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Invited Paper

Polarons as a Universal Source of Leakage Currents in Amorphous Oxides: A Multiscale Modeling Approach

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ABSTRACT

Gate leakage currents present a serious challenge for designing modern ultra-scaled metal-oxide-semiconductor (MOS) field effect transistors. While trap-assisted tunneling (TAT) has already been recognized as a major contribution to leakage currents in nanoelectronic devices, the microscopic nature of the traps acting as charge transition centers is still unclear. In this work we utilize a multi-scale modeling approach to link TAT to polaron states, which are acting similar to traps and are intrinsic to the amorphous gate dielectric. We first use density functional theory to study the electronic structure and the charge trapping dynamics of such polarons on an atomistic level in common gate dielectrics like SiO_2 or ZrO_2. From those calculations a nonradiative multiphonon model is derived to describe the charge hopping process between nearby polarons. Finally, the macroscopic gate leakage current is obtained from a Monte-Carlo device simulation, taking into account the stochastic distribution of trapping sites and their varying parameters due to the amorphous host material. By comparing the results of our simulation framework to experimental investigations on gate leakage currents for SiC/SiO_2 and TiN/ZrO_2 MOSCAPs, we provide compelling evidence that polarons are very likely the root cause for leakage currents in the studied devices. Our simulations further suggest that general features of these polarons, like the comparatively small relaxation energy, make them a universal source for steady-state leakage currents beyond the particular materials studied in this work.

Keywords: Trap-assisted tunneling, polarons, electron-phonon coupling, nonradiative transitions, charge transfer

1. INTRODUCTION

Charge trapping in oxide defects poses a significant reliability challenge in (nano)electronic devices like field-effect transistors. The charge accumulated in the oxide over the lifetime of the device causes a change in the device electrostatics and subsequently a drift of its threshold voltage. Due to its pronounced bias- and temperature dependence, this effect is commonly referred to as bias-temperature instability (BTI)[1] and can cause a failure of electronic systems at the circuit level. However, besides trapping charges in the oxide, defects can also mediate gate-leakage currents from the device channel to the gate contact.[2] Contrary to leakage currents caused by direct or Fowler-Nordheim (FN) tunneling (see Fig. 1), trap-assisted tunneling (TAT) through defects is strongly temperature dependent. These TAT currents have been observed at medium field strength in the range of $E_{\mathrm{ox}} \approx 4 - 8\,\mathrm{MV\,cm^{-1}}$ in SiC/SiO_2 based metal-oxide-semiconductor field-effect transistors (MOSFETs)[3] but also in devices with other dielectrics like HfO_2 and ZrO_2.[4]

The temperature dependence in both TAT and BTI indicates a nonradiative mechanism for charge transfer via electron-phonon coupling as the underlying cause.[1] Here, the defect involved in the charge transfer undergoes a pronounced structural relaxation upon capturing or emitting charges, which is associated with the exchange of multiple phonons with the surrounding heat bath. This process can be studied from first-principles for an individual defect within the framework of nonradiative multiphonon (NMP) theory, which was pioneered by Huang and Rhys[5] and was later formulated to be suitable for ab-initio calculations in density functional theory (DFT).[6] However, in order to link this microscopic description to experimental leakage currents in actual devices, a simplified model suitable for device simulations is required. Here we implement a Monte-Carlo sampling strategy

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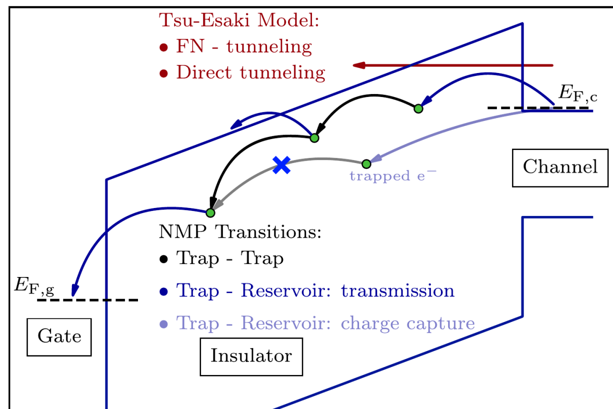

Figure 1. Different mechanisms for gate-leakage currents in a MOS gate stack. For direct and Fowler-Nordheim tunneling (red), an electron is injected into the oxide conduction band. This mechanism does not show a pronounced temperature dependence. On the contrary, for trap-assisted tunneling (black and blue) a defect state in the bandgap of the oxide serves as an intermediate step from which a charge can further "hop" to a different trap, the oxide conduction band or the gate electrode. Due to the coupling of the defect to the surrounding heat bath, this process shows a strong temperature activation in the form of an Arrhenius law. Reproduced from Ref. [10]

in our compact-physics device framework Comphy[7,8] to study the charge transfer over defects and the resulting gate-leakage currents. A stochastic approach is necessary here to efficiently account for the distribution of defect parameters due to the varying chemical environment in amorphous oxides.

By comparing the required parameters in our device model to reproduce the experimental gate-leakage currents with predictions from atomistic DFT calculations, we suggest that gate-leakage currents can be conducted over so-called electron polarons, i.e. states induced by self-trapped electrons. Our reasoning is based on the atypically low relaxation energies ($E_\mathrm{R} < 1.0\,\mathrm{eV}$) of the involved trapping sites required to explain the observed temperature-dependence of the TAT currents. Such low relaxation energies are uncommon for most defects in amorphous SiO_2 (a-SiO_2) but are a key signature of self-trapped electrons in this material.[9] The general energetic position of the "defect states" combined with the low relaxation energy further suggest that polarons could contribute significantly to leakage currents in most amorphous oxides.

2. *AB-INITIO* CALCULATIONS

In order to study defects or polarons in amorphous oxides, a credible atomistic model of the oxide has to be created first. This is usally done with the melt-quench procedure using classical molecular dynamics (MD) simulations. In order to create a-SiO_2 structures, a $3 \times 3 \times 3$ supercell of crystalline β-cristobalite containing 216 atoms was melted and quenched using the ReaxFF force field parameterized for silicon/silica interfaces[11] to describe the interactions in the SiO_2 system. Similarly, a Buckingham-type force field[12] was used to melt a $3 \times 3 \times 3$ supercell of cubic ZrO_2. In both cases, the crystal was melted at 5000K and subsqeuently equilibrated for 10 ps before it was quenched at a rate of $6\,\mathrm{K\,ps^{-1}}$ (a-SiO_2) and $5 - 20\,\mathrm{K\,ps^{-1}}$ (a-ZrO_2). The reason for the different quench rates used to generate a-ZrO_2 out of the crystalline phase is that, similar to other non-glass-forming oxides like HfO_2, it easily recrystallizes[13] and thus can show different degrees of crystallinity in experimental samples. We used different cooling rates to mimic this variation in our atomistic models.

Following the classical MD simulations, the resulting amorphous structures were further optimized using DFT. Both the atomic positions and the cell vectors were relaxed to residual atomic forces below $25\,\mathrm{meV\,Å^{-1}}$ and internal stress below 0.01 GPa. All DFT calculations were performed within the Gaussian plane wave method as implemented in the CP2K code[14] using the double-ζ Goedecker–Teter–Hutter (GTH)[15] basis set for expanding the electron density and wave functions. To obtain an accurate electronic structure of the models, we used the nonlocal hybrid exchange correlation (XC) functional PBE0_TC_LRC[16] with a Hartree-Fock (HF) mixing parameter of $\alpha = 0.25$, resulting in a single-particle bandgap of 8.1 eV (a-SiO_2) and 5.9 eV (a-ZrO_2)in good agreement with the experimental values of 8.9 eV (a-SiO_2) and 5.8 eV (a-ZrO_2).[17] To mitigate the high

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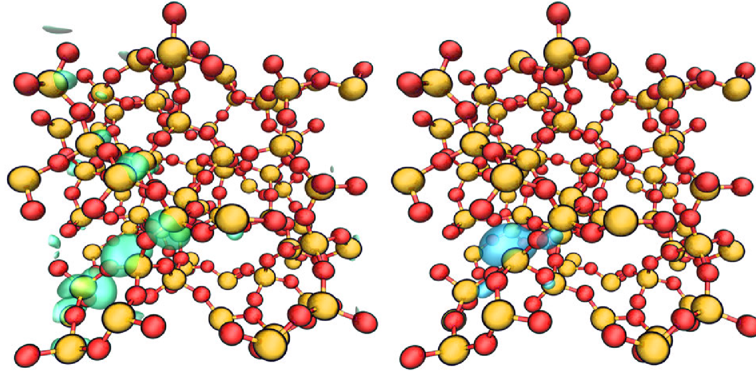

Figure 2. Spontaneous localization of an electron in a-SiO_2. The lowest unoccupied molecular orbital (left, green) in the structure is a semi-localized state. Upon capturing an electron, this state spontaneously localizes (right, blue) at a particular site, forming a self-trapped electron similar to small polarons known in crystalline materials. Reproduced from Ref. [21]

computational costs for the exact Hartree–Fock exchange integrals, the auxiliary density matrix Method[18] was used to approximate the exchange in a smaller auxiliary basis set.

With the amorphous oxide structures established, we then injected additional electrons into the conduction band of the oxide to study the formation of polarons. For a detailed description of the procedure, see Ref. [9] for the case of a-SiO_2. Relaxing the structure with fixed cell vectors after electron injection leads to a spontaneous localization of the additional electron at a precursor site as shown in Fig. 2. In a-SiO_2 these precursors are made up of strained O-Si-O bonds naturally occuring at a concentration of roughly $4.5 \times 10^{19}\,\mathrm{cm}^{-3}$ as has been determined by large-scale MD simulations.[19] In a-ZrO_2, however, self-trapping can occur at locally oxygen deficient sites, similar to what has been reported in previous works for HfO_2.[13] Note however, that these sites are distinct from true oxygen vacancies, which typically introduce defect states in the bandgap, whereas here, the “defect” state only forms after self-trapping of an electron. These calculations are used to extract the thermodynamic charge transition level (CTL) and the relaxation energy of the polaron state. These two quantities are key parameters for modeling the charge transfer rates in a device-level NMP model. For a detailed discussion on how to extract these parameters from ab-initio calculations, we refer to the literature.[20] The extracted parameters for electron polarons in both materials are collected in Tab. 1. Note that 50 different amorphous structures had to be analyzed in order to assess the statistical spread of the polaron charge trapping parameters.

3. DEVICE MODELING

As the basis for our device simulation, we use our previously developed 1D compact model in the Comphy package.[7,8] Within Comphy, a surface potential approach is used to obtain important quantities like the carrier concentration in the channel as a function of the gate bias and the temperature. Using this framework, the total gate-leakage current can be calculated as

$$I_{\mathrm{tot}} = I_{\mathrm{TAT}} + I_{\mathrm{direct/FN}} + I_{\mathrm{DP}}\,, \tag{1}$$

with the TAT current I_{TAT}, the direct tunneling current $I_{\mathrm{direct/FN}}$ described by a Tsu-Esaki model,[22] and the displacement current I_{DP}. The displacement current arises from transient currents required to change the voltage across the gate oxide capacitance. The displacement currents can be ignored for comparisons with gate leakage measurements, when these measurements are performed with a sufficiently low gate sweep rate.

The TAT current can be obtained from a generalized version of the Shockley-Ramo theorem and is given by[23]

$$I_{\mathrm{TAT}} = q_0 \sum_i k_{\mathrm{e},i,\mathrm{gate}} f_i + q_0 \sum_{i,j\neq i} k_{\mathrm{e},ij}(1 - f_j)\,, \tag{2}$$

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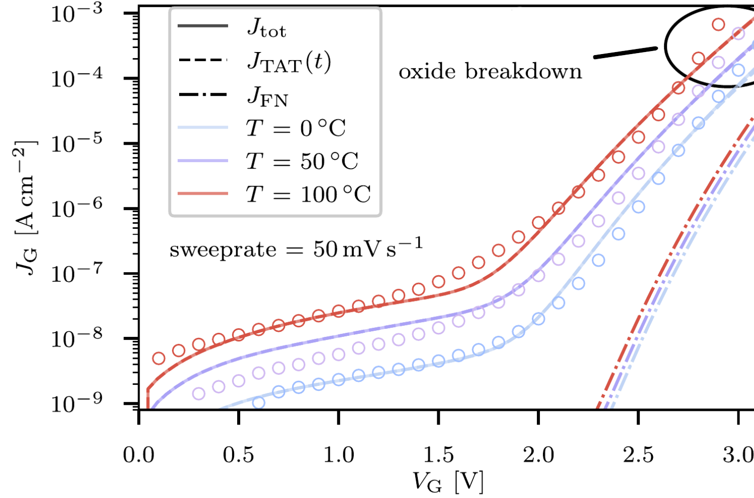

Figure 3. Experimental (dots) and simulated gate leakage currents for the studied MIM ZrO_2 capacitor at different temperatures. For lower electric fields ($V_G < 2.0\,V$) the currents are transient and change the occupancy of defects associated with BTI. At higher fields, however, the gate leakage is dominated by stationary TAT currents. Both currents show a pronounced temperature dependence, indicating a trap-assisted tunneling mechanism, whereas Fowler-Nordheim (FN) tunneling exhibits almost no temperature activation. Reproduced from Ref. [21]. The experimental data is taken from Ref. [24]

with $k_{e,i,\text{gate}}$ and $k_{e,ij}$ being the charge emission rates of defect i into the gate and into a different defect j respectively. The defect occupancies f_i obey a set of Master equations given by

$$\frac{\mathrm{d}f_i}{\mathrm{d}t} = (1 - f_i)R_{c,i} - f_i R_{e,i} \quad \text{with} \tag{3}$$

$$R_{c,i} = k_{c,\text{channel},i} + k_{c,\text{gate},i} + \sum_{j \neq i} k_{c,ij} f_j \tag{4a}$$

$$R_{e,i} = k_{e,i,\text{channel}} + k_{e,i,\text{gate}} + \sum_{j \neq i} k_{e,ij}(1 - f_j) \tag{4b}$$

The capture and emission rates, k_c and k_e respectively, depend on the location of the defects, the gate bias, the temperature, as well as the charge transfer parameters of the defects and are calculated within NMP theory.

In order to calculate the TAT currents efficiently, a certain number of defects is sampled from a distribution function, assuming normally distributed relaxation energies and charge trap levels together with uniformly distributed trap locations. Rejection sampling is used to avoid defects being unphysically close to each other, with a cutoff distance of 1.0 nm. Given a set of defects, the nonlinear set of equations 3 is solved using an implicit Euler scheme, resulting in the defect occupancies f_i from which the total TAT currents can be computed. Further details about the device simulation aspects of our work can be found in Refs. [10, 21].

4. RESULTS

We use our device modeling framework to fit the required parameters for charge trapping in defects to reported gate-leakage currents measured on two different gate stacks, namely a SiC MOSCAP with thermally grown SiO_2 and a metal–insulator–metal (MIM) capacitor using ZrO_2 as a high-κ dielectric. The experimental gate-leakage currents in the case of the ZrO_2 MIM devices together with the fit obtained from our device simulation are shown in Fig 3. As can be seen, there is a good agreement to the experiment over a wide range of gate biases and temperatures. The leakage current exhibits a pronounced temperature dependence indicating a charge transport via electron-phonon coupling. A more thorough investigation shows that at low biases ($V_G < 2.0\,V$) the currents are transient and change the occupancy of defects associated with BTI. At higher gate bias, the current becomes a stationary TAT current. For comparison, the calculated Fowler-Nordheim tunneling current with a significantly smaller temperature dependence is also plotted in Fig 3.

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		$\langle E_\mathrm{T}\rangle$ [eV]	σ_{E_T} [eV]	$\langle E_\mathrm{R}\rangle$ [eV]	σ_{E_R} [eV]	max x_T [nm]	N_T [cm^{-3}]
a-SiO_2	TAT (Exp.)	2.85	0.10	0.89	0.11	3.0	7.6×10^{18}
	Polarons (DFT)	2.53	0.23	1.06	0.23	–	–
a-ZrO_2	TAT (Exp.)	1.09	0.10	0.76	0.10	-	3.0×10^{18}
	Polarons (DFT)	1.24	0.20	0.70	0.15	–	–

Table 1. Summary of the used parameters (trap level E_T, relaxation energy E_R, trap positions x_T, trap density N_T) to explain the experimental data in our device model and the theoretical predictions for polarons from DFT for the two dielectrics studied in this work. The good agreement between predictions and experimental data indicates that polarons are a likely candidate for causing TAT in both materials.

As summarized in Tab. 1, in both gate stacks the relaxation energy of the required defects for TAT currents to occur are around $E_R \leq 1.0\,\mathrm{eV}$. However, typical oxide defects in a-SiO_2 like the oxygen vacancy, the hydrogen bridge or the hydroxyl-E$'$ center usually have relaxation energies in the range of $E_R = 2.0 - 4.0\,\mathrm{eV}$,[20,25] rendering them unable to contribute significantly to the TAT currents. On the other hand, our DFT calculations show that in both materials self-trapped electrons (polarons) are in good agreement with the parameters extracted from our device model.

5. CONCLUSIONS

By combining ab-initio calculations with physics-based device-level simulations for calculating gate-leakage current, we provided evidence for self-trapped electrons (polarons) playing a dominant role for trap-assisted tunneling currents in amorphous gate oxides. This conclusion is based on the unusually low relaxation energy of the trap states responsible for TAT, which are inconsistent with most defect candidates. However, electron polarons in amorphous oxides not only have such low relaxation energies, but also have a trap level generally located between the conduction bands of the oxide and the semiconductor, making them a likely source of TAT currents in amorphous oxides in general beyond the specific materials studied in this work.

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