Solid-State Electronics Vol. 27, No. 4, pp. 394–395, 1984
Printed in Great Britain.

0038-1101/84 $3.00 + .00
Pergamon Press Ltd.

TEMPERATURE DISTRIBUTION AND POWER DISSIPATION IN MOSFETs

(*Received* 27 *June* 1983; *in revised form* 22 *September* 1983)

Due to the rapid progress in the development of microelectronic circuits, many semiconductor simulation models have been published during the last year to offer a better understanding of device physics. Certain models concentrate on MOS-transistors because the most rapid advance is due to this kind of device. The number of functions per chip has been increased reducing the dimensions of the single transistor, e.g. channel length[3]. As a consequence, current density and electric field strength increase within the device and, therefore, the power dissipation per chip is also increased. Therefore, cooling problems become more important. In MOS-transistors, heat is produced only in a thin sheet near the semiconductor surface and the question for the peak temperature in the device may rise.

We have analyzed the temperature distribution in small scale MOS-transistors by solving the heat-flow equation in two dimensions.

$$\operatorname{div}[\kappa(T)\operatorname{grad} T] = -P. \tag{1}$$

The solution is carried out numerically by the finite difference method. The boundary conditions of the differential eqn (1) are determined by external thermal resistances. Mathematically they are of Dirichlet–Neumann mixed mode type[4, 6]. The thermal conductivity $\kappa(T)$ has been investigated over a wide temperature range and is given by e.g.[5]

$$\kappa(T) = \frac{1}{0.03 + 0.00156T + 1.65 \cdot 10^{-6T^2}} (\text{W/K cm}). \tag{2}$$

For 300K $\kappa(T)$ equals 1.55W/Kcm. For the gate oxid another formula applies which has been fitted to data found in[10].

After discretization into finite differences eqn (1) becomes a system of nonlinear algebraic equations which can be linearized according to Newton's method. Since eqns (1) and (2) are only weakly nonlinear good convergency behavior can be observed and usually two or three iterations suffice to obtain satisfactory results.

The heat generation term in eqn (1) is given by

$$P = \mathbf{E} \cdot \mathbf{J} - q \cdot U_G \cdot (G\text{–}R). \tag{3}$$

with U_G the band gap and $(G\text{–}R)$ the generation/recombination rate. This equation has been already proposed by Alder[1]. The first term at the right hand side is the power supplied by the electric field. The second term describes the power necessary for the generation of carriers. A different expression for the heat generation has been proposed by Chryssafis *et al.*[2], however, their formulation differs from eqn (3) and is not plausible from the physical point of view.

Equation (3) may be interpreted as follows: Heat is produced whenever an electron loses potential energy which may be due to electronic conduction or recombination. Energy storage in the hot electron gas is not considered in eqn (3). To account for this effect requires very time consuming Monte–Carlo techniques[7, 8], however, the influence of this effect can be considered to be very small. The thermal problem has been decoupled from the electrical problem[9] to reduce essentially the complexity of the solution algorithm. For the electrical problem constant temperature has been assumed which is a rather rigid approximation; it is justified only because of the small temperature variation within the device as will be shown in the following.

Figure 1 shows equithermal curves in an MOSFET operating in the pentode region. This operation mode has been chosen to show a worst case situation as the power dissipation is largest in this regime. Although the electric field is very high in the pinch-off region (250 kV/cm) with enormous power density, the peak temperature is only five degrees higher than the minimum temperature within this plot. Most of the temperature drop occurs within the deep substrate and across external thermal resistances. A similar result has been obtained for thyristors[1] and it is due to the very high thermal conductivity of silicon. The heat-flow equation has not been solved explicitly for two dimensions within the deep substrate. As the thickness of the substrate (d approx. 500 μm) is not small compared to the channel width, three-dimensional effects become important. Therefore, it is more useful to extend the two-dimensional simulation only for a thin layer near the surface (thickness d_s approx. 10 μm) and to simulate the deep bulk by an effective thermal resistor[9]

$$R_{th} = \frac{d - d_s}{\kappa(L + 2d)(L + 2d_s)}. \tag{4}$$

This parasitic resistor has to be added to any external thermal resistor. In our example a value of 400 K/W has been used for the effective (parasitic + external) substrate resistor. The thermal resistor at the gate electrode and the

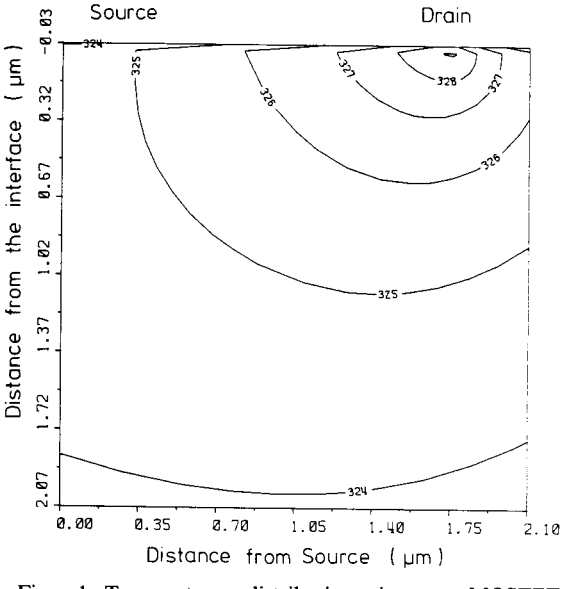

Fig. 1. Temperature distribution in an MOSFET (W = 100μm, $L_{\text{eff}} = 1.5\mu\text{m}$) operating at $U_{DS} = 6.5\text{V}$, $U_{GS} = 3\text{V}$, $I_D = 13.7\text{mA}$. The horizontal axis is parallel to the channel and is calibrated in μm distance from the source. The vertical axis points into the substrate and indicates the distance from the Si–SiO_2 interface. The equithermal curves exhibit a sharp bend at the interface which is due to the different $\kappa(T)$ in both materials.

external temperature have been set to 600K/W and 300K, respectively.

We conclude from Fig. 1 that heat problems in VLSI-MOSFETs can be overcome by reducing the parasitic thermal resistances of the basic device (e.g. reduction of the substrate thickness) and by improving the external heat. This statement is justified because of the small temperature variation within the intrinsic device.

Acknowledgements—This work was supported by the "Fonds zur Förderung der wissenschaftlichen Forschung" under project S 22/11. The authors would like to thank the "Interuniversitäres Rechenzentrum der T.U. Wien" for providing a generous amount of computer resources.

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Printed in Great Britain.

0038-1101/84 $3.00 + .00
Pergamon Press Ltd.

METHOD FOR REDUCTION OF HYSTERESIS EFFECTS IN MIS MEASUREMENTS

(*Received* 2 *May* 1983; *in revised form* 7 *September* 1983)

Application of a voltage U_F varying with time to an MIS system may lead to pronounced hysteresis. This is used in MNOS memory devices[1], but may lead to ambiguity in the evaluation of energetic distributions $D_{it}(E)$ of interface traps. If for that purpose a method is used which is based upon the variation of the surface potential ψ_s as a function of U_F in thermodynamic equilibrium, the equation

$$q^2 D_{it} = C_i\left(\frac{dU_F}{d\psi_s} - 1\right) + \frac{dQ_{sc}}{d\psi_s} \qquad (1)$$

(where C_i is the insulator capacitance and Q_{sc} the total charge in the space charge layer, both per area) is generally used[2]. The function $\psi_s(U_F)$ may be determined e.g. by $C(V)$ data, field effect measurements, or, as in the measurements presented below, by large-signal photovoltage pulses according to[3, 4]. Here we address also (but not exclusively) MIS structures which are composed of 3 detachable parts (M, I and S, the latter e.g. with "real" surfaces[5]) as used in many classical field effect experiments[5]. In any case, it is clear from (1) that only single-valued functions $dU_F/d\psi_s$ and $dQ_{sc}/d\psi_s$ will lead to unambiguous values for $D_{it}(E)$. Hysteresis may even appear in MIS systems with an ideal insulator (see (2) and (3) below) and is often quite disturbing when optimizing non-silicon MIS structures. Examples of $C(V)$ curves with (unwanted) hysteresis are to be found e.g. in[6–8].

A method to reduce hysteresis effects, using small regions of sweep with an otherwise classical $C(V)$ method[9] seems, as the examples quoted last indicate, not to have found widespread application.

We consider now three causes of hysteresis and the means used in this work to reduce it.

(1) Drift of carriers in or into the insulator (one example is drift of ions during voltage stress[10]) often occurs. By applying U_F in the form of (rectangular, duration 0.4 s) pulses (see. Fig. 1b) the time for drift may be reduced as compared to the mode used in Fig. 1(a) and, consequently, the hysteresis becomes smaller. Adding voltage pulses of opposed polarity (see Fig. 1c) can help to cause a shift of carriers back into their original position, thereby further reducing hysteresis.

(2) Non-equilibrium in the space charge layer of the semiconductor[11] may lead to hysteresis, which in many

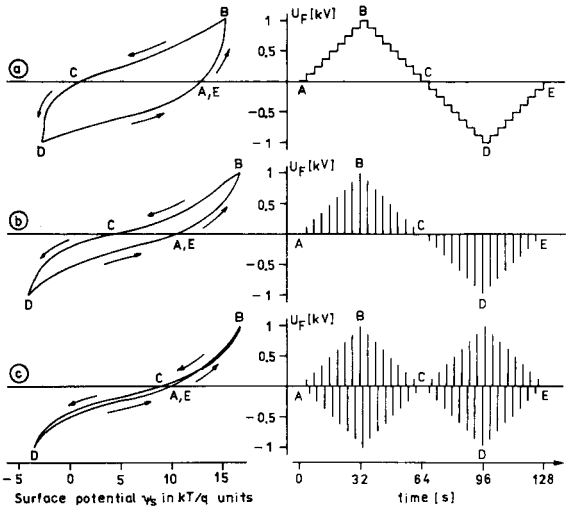

Fig. 1. Field modulation mode (right) and corresponding experimental results (left). The individual points $\psi_s(U_F)$ have been omitted because they do not show visible deviations from the smooth curve drawn through them. Si-sample prepared (see text) and measured at room temperature.

cases is caused by insufficient minority carrier generation. In[12] additional carriers were produced by continuous illumination. The simple eqn (1), however, then no longer holds. In our experiments strong flashes of light, which coincide with the centre of the field voltage pulses scetched in Fig. 1(b), are used for the determination of ψ_s from the resulting photovoltages[3, 4]. The optical pulses have a length of $\approx 1\mu s$, each generates a maximum excess pair concentration of $2 \cdot 10^{16}\,cm^{-3}$. This value is larger than even that of the majority carrier concentration of the Si-samples we investigated. We did, therefore, neither expect nor observe problems with insufficient minority carrier generation.

(3) Non-equilibrium between interface states and the semiconductor may be a further cause of hysteresis[7, 8]. In[13] illumination (constant during a sweep) was used to reduce the amount of this type of non-equilibrium. Similarly, pulsed illumination—often used in photovoltage experiments—is thought to give a contribution to the reduction of hysteresis in our investigations. Because the time of non-equilibrium produced by the optical pulses is considerably shorter than the length of the field voltage pulses the application of (1) seems justified. We have made measurements at Si samples with a wide range of surface properties, resulting in D_{it}-values between $(6 \cdot 10^{10} \ldots 3 \cdot 10^{14})\ eV^{-1}\,cm^{-2}$. All of these measurements could be evaluated using (1) without any serious doubt concerning hysteresis, if the mode indicated in Fig. 1c was used. As an example we present (left part of Fig. 1 and Fig. 2) results which were obtained at a Si sample with (111) surface, which was—after the usual mechchem polishing to mirror finish—cleaned in methanol and then treated with NH_4OH (10%) for 10 min at room temperature, rinsed for 15 min in deionized water, spun dry and kept in dry clean air. ("Real" surface). For details about measuring apparatus and evaluation of the photovoltage pulses cf.[3, 4]. The appearance of hysteresis was responsible for the significantly different results for $D_{it}(E)$ in Fig. 2 (cf. legend). In curve 3 of Fig. 2 the influence of hysteresis is negligible. This allowed reliable comparisons with Flietner's model calculations[14] without the explicit consideration of insulator-polarization effects discussed in[15].

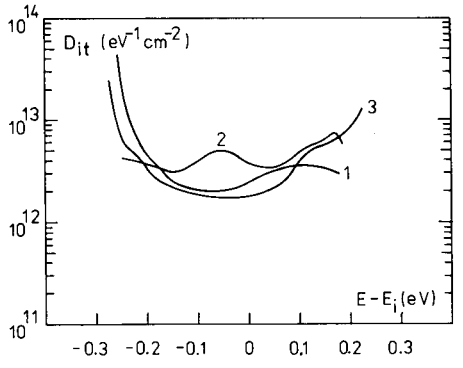

Fig. 2. Energetic distributions of surface states, determined from the results prepared in Fig. 1. Curve 1 obtained from the upper branch of *a*, curve 2 from the averaged ψ_s-values of *a*, curve 3 from the averaged values of *c*.

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