The sensitivity of short channel MOSFET's on technological tolerances

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Very Large Scale Integration is based on the miniaturization of the single transistor device. To shrink just the physical device dimensions usually will yield serious problems concerning the device behaviour. As it is commonly known all device parameters have to be "scaled" (p.e. /1/) together with the device geometry according to certain rules. In general, lower voltages, heavier doping, shallower junctions and thinner oxides help to maintain applicable device characteristics as channel length is reduced. Down to about two microns channel length the device behaviour can be controlled excellently by the relevant technological steps (implantation, diffusion, oxidation). However, as often observed by experimental investigations, the same process control is no longer ensured for devices with a further reduced channel length. In order to achieve more transparency for this fact a process sensitivity analysis has been performed. As a representative technology an n-channel silicon gate process on an 8 Ωcm has been chosen. This process is used by Siemens AG, Munich. A proper channel profile originates by a double boron implantation (35 keV, $3\cdot10^{11}cm^{-2}$ and 160 keV, $10^{11}cm^{-2}$ respectively) followed by a low temperature anneal treatment. Transistors with a gate oxide of 500 Å and arsenic source and drain junctions with a depth of about 3000 Å were fabricated with varying channel lengths down to the submicron range. These devices have first been measured accurately to extract the relevant device parameters like threshold voltage, subthreshold slope and breakdown voltage. Secondly, two-dimensional numerical simulations /2/,/3/,/4/ of this kind of devices have been made, to get a relation between experimental and theoretical results and so, to verify both measurement and calculation.

Usually in papers on submicron MOS transistors comparisons between theoretical curves and selected experimental points are given. But with respect to the inherent dependence of most parameters on the dispersion of the geometrical and technological parameters, it seems to be necessary to analyse and present these dependences directly. Numerical investigations in feedback with experiment have been carried out to extract the most interesting values, which are the partial derivatives of the threshold voltage and the breakdown voltage with regard to the channel length, the drain voltage, the oxide thickness and depth and peak concentration of the channel implant. As just one particular result, which is easy to discuss, the sensitivity of the threshold voltage on channel length variation is given in this abstract for the transistors specified above (Fig. 1). The dashed line denotes a drain bias of 0.5 Volt, the solid line a drain bias of 5 Volt. To interprete these curves assume a transistor with an effective channel length of one micron with an uncertainty of ten percent; that is a possible absolute dispersion in channel length of just 1000 Å. For a drain voltage of 0.5 Volt one can read out of Fig. 1 an uncertainty of the threshold voltage of ± 25 millivolts,which, in general, is not dramatic. For a drain bias of 5 Volt one has already an uncertainty of ± 58 millivolts, which will cause quite a few circuits to fail in operation. Displeasing in this discussion are the facts that an uncertainty of the channel length of only ten percent is a very good value for short channel devices. On top of that the chosen device design is realistic and does not especially pronounce the outlined effects. Further should be noted that for these curves all the other technological parameters are assumed to have the correct value (partial derivatives). For application to reality all the worst possible tolerances have to be taken into account to get a sensitivity estimate. As a conclusion one should be afraid that the enormous increase of process sensitivity with shrinking device geometries might probably be a practical limit of miniaturization.

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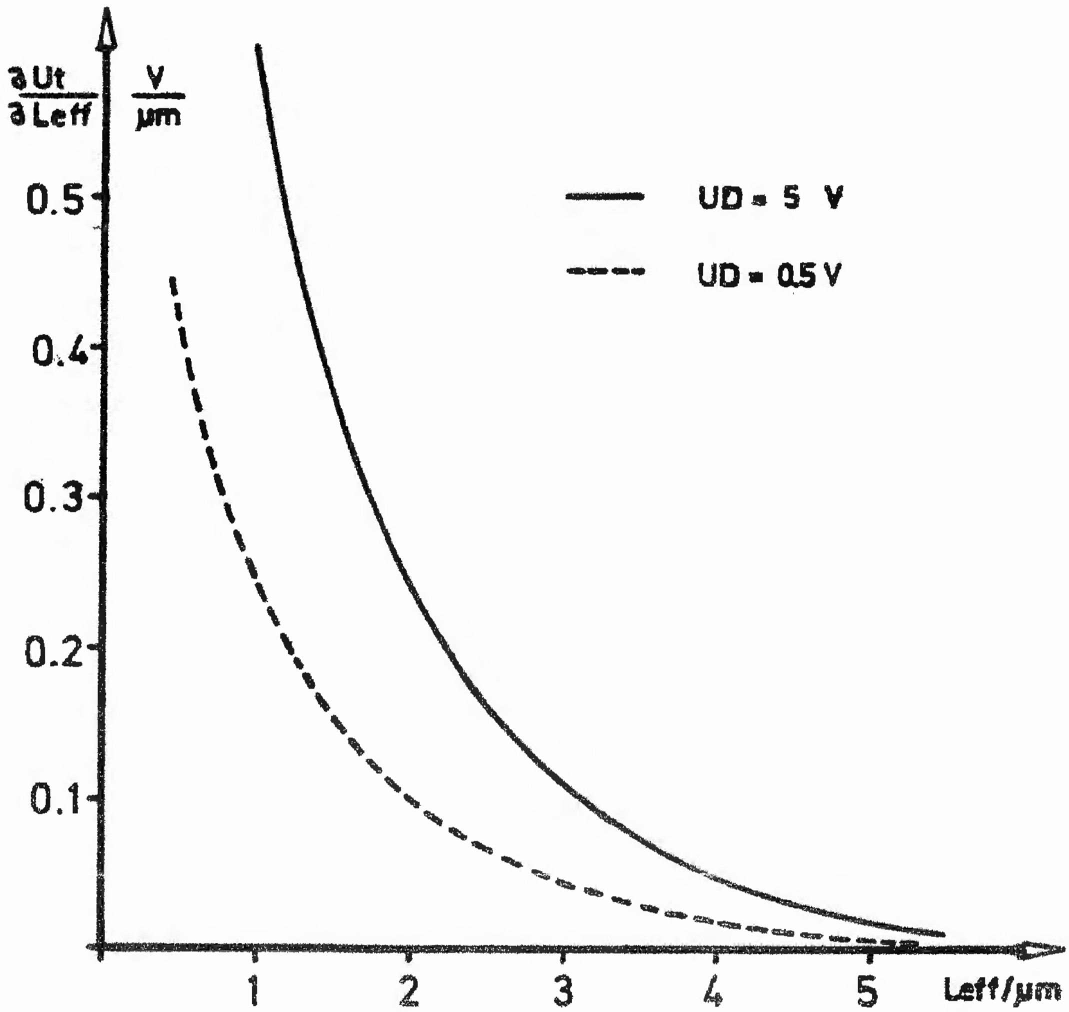

Fig. 1