NUMERICAL ANALYSIS OF BREAKDOWN PHENOMENA IN MOSFET's

A. SCHÜTZ, S. SELBERHERR, and H.W. PÖTZL

Institut für Physikalische Elektronik
Technische Universität Wien
Gußhausstr. 27, 1040 VIENNA, AUSTRIA
and Ludwig Boltzmann Institut für Festkörperphysik

Abstract

An accurate two dimensional self consistent numerical model for MOS transistors which is able to predict avalanche behaviour is presented. This model is directed towards better understanding of the physical processes arising from the avalanche effect and leading to breakdown. The system of the basic semiconductor equations is solved with respect to several generation recombination mechanisms representing an inhomogeneity term in both carrier continuity equations. To improve the description of the ionization process correction terms are introduced to account for the fact that the gate induced field does not cause ionization.

1. Introduction

Two-dimensional numerical simulation of semiconductor devices has become a rapidly growing, interesting field in semiconductor physics. However, most of the models published so far neglect impact ionization to simplify the numerical problem. To the authors knowledge only one paper has been published on two-dimensional avalanche simulation in MOSFET's /1/. That model, however, is not fully consistent as the continuity equation for majorities is not solved. Thus the majority carrier distribution is not consistently calculated which, in strong avalanche, will influence the electrical potential solution. This simplification is only valid in the case of weak avalanche.

In our model impact ionization is treated as inhomogeneity in both carrier continuity equations which are solved consistently with Poisson's equation. In the following the physical model and typical results of our analysis will be presented.

2. Model description

The present model is based on the two dimensional self consistent solution of Poisson's equation and both continuity equations including generation recombination mechanisms. The partial differential equations are solved with the finite difference method. For more details about the discretisation, the numerical method, and the program structure see /2/, /3/, and /4/.

$$\operatorname{div} \varepsilon \operatorname{grad} \Psi = -q\,(p - n + N_D - N_A) \qquad (1)$$

$$\mathrm{div}\ \vec{J}_n = -q\ (G - R) \tag{2}$$

$$\mathrm{div}\ \vec{J}_p = q\ (G - R) \tag{3}$$

Within this model the avalanche is included in the (G - R) terms in eq. 2 and eq. 3. These terms include generation of electron hole pairs by impact ionization but also recombination processes which are described by Shockley-Read-Hall terms for the surface and the bulk and an Auger recombination term.

$$(G-R) = (G-R)_s + (G-R)_b + (G-R)_{Aug} + G_{ion} \tag{4}$$

Avalanche generation G_{ion} is described by Chynoweth's law. A correction is introduced to account for the fact that the gate induced field does cause ionization as it is usually perpendicular to the motion of the carriers. The ionization coefficients used in (7) are obtained from /5/.

$$(G-R)_{Aug} = (p \cdot n - n_i^2)\ (C_n \cdot n + C_p \cdot p) \tag{5}$$

$$G_{ion} = \frac{|\vec{J}_n|}{q} \alpha_n(E) + \frac{|\vec{J}_p|}{q} \alpha_p(E) \tag{6}$$

$$\alpha_n(E) = A_n \exp\left(\frac{-B_n |\vec{J}_n|}{|\vec{E} \cdot \vec{J}_n|}\right) \tag{7a}$$

$$\alpha_p(E) = A_p \exp\left(\frac{-B_p |\vec{J}_p|}{|\vec{E} \cdot \vec{J}_p|}\right) \tag{7b}$$

Although the recombination effects usually are negligible for MOSFET's in the normal mode of operation, they may become important in the avalanche region because of the drastic increase in carrier densities all over the device. Especially Auger recombination will become important as it is a cubic function of the carrier densities.

As impact ionization is very sensitive to the electric field, Poisson's equation has to be solved very carefully. Thus the finite difference mesh is adjusted to the doping profile and to the potential distribution to limit the potential increments. Furthermore it is checked during the iteration process and modified if necessary.

3. Results

A power of the present model lies in the prediction of the internal physical processes in MOSFET's occurring in the avalanche region. This offers better principal understanding than the mere calculation of avalanche currents. In the following we shall analyse the snap back behaviour of n- channel MOSFET's which is a rather interesting phenomenon. Fig. 1 shows calculated drain and bulk current vs. drain voltage characteristics for a 1 micron MOSFET. Because of the larger drain to gate voltage, the electric field distribution at the same V_{DS} shows a slightly higher peak value for V_{GS}=0V than for V_{GS}=1V resulting in a somewhat larger avalanche multiplication factor. From that point of view it seems to be paradox that the breakdown voltage is higher for V_{GS}=0V. However, this characteristic shows snap back behaviour, i.e. negative resistance occurs. In this branch of the curve the drain voltage decreases with rising current and finally approaches a value which is called sustain voltage.

In this chapter it will be shown that the electrical behavior of the MOSFET near breakdown is mainly determined by the internal hole distribution. This distribution is shown in fig. 2 and fig. 3 for two different operating points V_{DS}=5.6V, V_{GS}=1V and V_{DS}=8V, V_{GS}=0V, respectively. Holes are generated by impact ionization in the pinch- off region as indicated by the peaks at the surface. These excess holes have to recombine with electrons or have to leave the device through the bulk contact giving rise to bulk current according to

$$I_B = \int_{Device} (G - R) \, dV. \tag{8}$$

A further increase of impact ionization increases the hole density especially near the source junction due to the lower electrical potential. The space charge of this hole density lowers the source to bulk barrier thus increasing the electron current. If the gain of the corresponding feedback mechanism (larger hole density - larger electron current - more impact ionization causing even larger hole density) is equal to or larger than 1, an unlimited increase of the node currents is started. This usually occurs at much smaller drain voltages as would be necessary for an infinite avalanche multiplication factor. The barrier lowering which indicates the feedback mechanism is dependent on the voltage drop due to the bulk current and the parasitic resistance of the deep bulk. Thus for given substrate doping a critical bulk current level exists.

Now we can analyze the paradoxon mentioned above. At the lower gate voltage (0V) the electron current density near the surface is very much lower than for the higher gate voltage (1V). Therefore fewer holes are generated by the avalanche in spite of the slightly higher field values. This implies that the critical bulk current level is reached at a considerably higher drain voltage for the lower gate voltage. This can be seen in fig. 1. A more negative substrate bias increases the critical substrate current, thus increasing the breakdown voltage too.

Now we would like to discuss the phenomenon of the negative resistance and the physical process leading to the sustain voltage. The critical bulk current level yielding unity feedback gain corresponds to a vertical slope of the drain current characteristic. Beyond that point, at further increasing current level, the ionization rates α_n, α_p must decrease to keep the avalanche generation G_{ion} at an approximately constant level. Therefore V_{DS} decreases yielding negative resistance which is commonly denoted as snap back. By this process an electron hole plasma is built up. With increasing plasma density the recombination increases nonlinearly because of the Auger process thus consuming most of the holes generated by avalanche. The avalanche generation must remain sufficiently large to feed this dramatically increasing recombination. Furthermore the large plasma density smoothes the electric field distribution reducing impact ionization. Consequently, no further decrease of the drain voltage is possible without the plasma and the breakdown phenomenon vanishing. In this region of operation the internal quantities are dependent on the drain current rather than on the gate voltage. Therefore a unique sustain voltage will be reached at high current levels.

It has been reported that short channel devices show scarcely snap back behavior /6/. The same can be observed at higher gate voltages. This phenomenon can be easily explained on the lines of the last paragraph: Because of the large source current which can be due to a large gate voltage as well as to a small channel length, the critical substrate current is reached below sustain voltage. Thus snap back cannot occur.

4. Conclusion

In this contribution we have shown a numerical method to analyze MOS transistor avalanche. It is based on the consistent solution of the basic semiconductor equations. In this way reliable values for the node currents can be calculated. The main power of our algorithm, however, lies in the prediction of the internal quantities thus allowing for better principal understanding of breakdown phenomena. The hole density is shown to play an important role in the description of breakdown effects. The voltage drop of the bulk current at the parasitic resistance of the deep bulk causes an internal feedback phenomenon similar to the role of the base resistance in bipolar transistor breakdown. A negative resistance branch of the characteristic can arise in this way which is usually denoted as snap back. High currents due to high gate voltage and/or short channel length and the resulting strong recombination tend to cover the snap back effect.

Owing to the lack of space and to avoid confusion only results for an n- channel transistor have been presented. However, p- channel devices can be analyzed in the same way.

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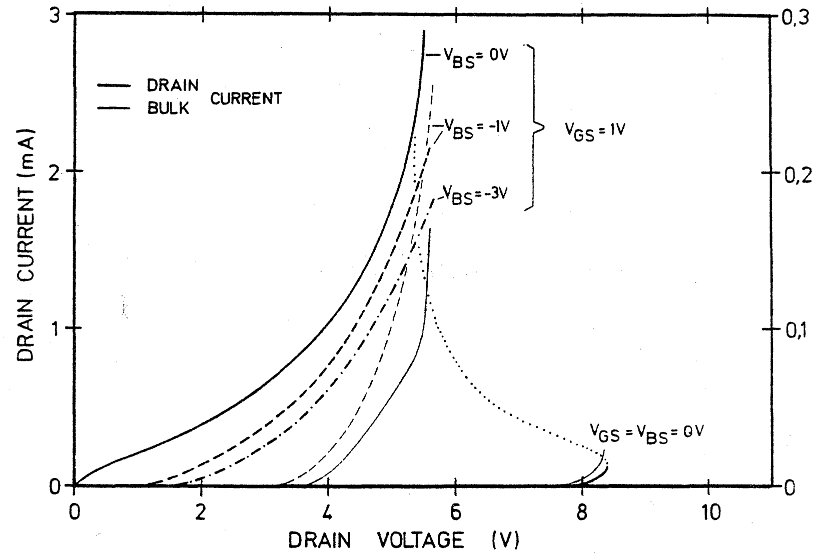

Fig. 1

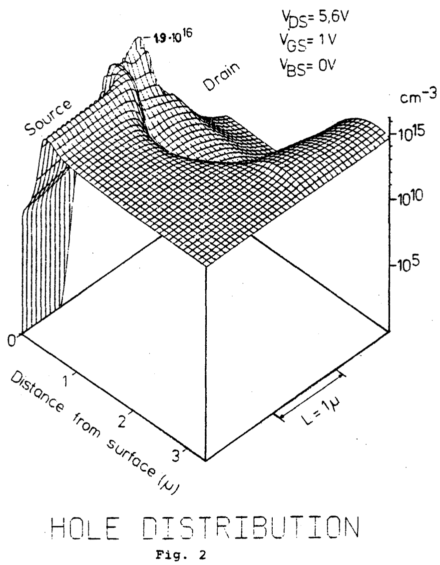

Fig. 2

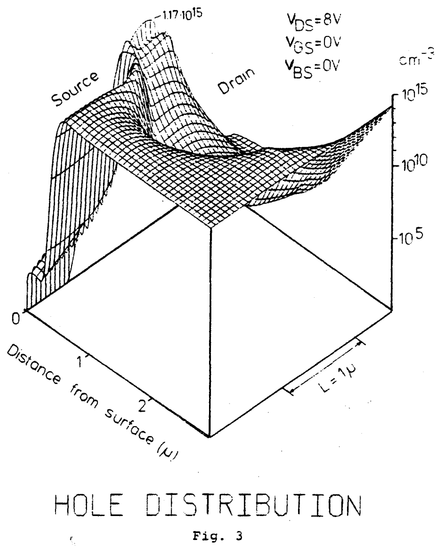

Fig. 3