

MINIMOS—A Two-Dimensional MOS Transistor Analyzer

SIEGFRIED SELBERHERR, MEMBER, IEEE, ALFRED SCHÜTZ, AND HANS WOLFGANG PÖTZL, MEMBER, IEEE

Abstract—We describe a user-oriented software tool—MINIMOS—for the two-dimensional numerical simulation of planar MOS transistors. The fundamental semiconductor equations are solved with sophisticated programming techniques to allow very low computer costs. The program is able to calculate the doping profiles from the technological parameters specified by the user. A new mobility model has been implemented which takes into account the dependence on the impurity concentration, electric field, temperature, and especially the distance to the Si-SiO₂ interface. The power of the program is shown by calculating the two-dimensional internal behavior of three MOST's with 1- μ m gate length differing in respect to the ion-implantation steps. In this way, the threshold voltage shift by a shallow implantation and the suppression of punchthrough by a deep implantation are demonstrated. By calculating the output characteristics without and with mobility reduction, the essential influence of this effect is shown. From the sub-threshold characteristics, the suppression of short-channel effects by ion implantation becomes apparent. The MINIMOS program is available for everyone for just the handling costs.

I. INTRODUCTION

VERY-LARGE-SCALE INTEGRATION (VLSI) of MOS circuits made computer-aided simulation an urgent necessity in modern MOS transistor design, particularly, as experimental investigations are very time consuming, often too expensive, and sometimes not at all feasible. All the analytic models published use certain assumptions and regional approximations, which are often so restrictive that only a very limited predictability of MOS performance is achievable. Especially as the structures have been more and more miniaturized, the applicability of those simple models turned out to be insufficient. In order to characterize modern devices in a reasonable way, the designer is forced to apply higher order numerical models.

In the last decade, several attempts have been made to develop computer-simulation programs based on two-dimensional models without too restrictive assumptions according to physical constraints [1]–[10]. But in almost every case, a wider application of these programs was frustrated either by limited performance due to missing numerical stability or by the necessity of too large an amount of computer operating cost.

We have developed MINIMOS, a highly user-oriented program package for the two-dimensional simulation of planar

Manuscript received November 26, 1979; revised February 22, 1980. This work was sponsored by the "Fonds zur Förderung der wissenschaftlichen Forschung" under Projekt 3358. The MOS transistors were provided by Siemens AG, Munich, Germany.

The authors are with the Institut für Physikalische Elektronik, Technische Universität Wien, Vienna, Austria, and the Ludwig Boltzmann-Institut für Festkörperphysik, Vienna, Austria.

MOS transistors. Modern programming methods ensure a maximum of flexibility and the required low computing costs. Dynamic memory management feasibility has been included to adjust automatically the actual memory requirement. The main parts of the solution routines are assembly coded to allow a very fast execution. The syntax of the input language is easy to remember and fully compatible with a recently published proposal for a unified input syntax for CAD programs [11]. In Section II of this paper the physical model which is implemented in MINIMOS is described; the numerical treatment is discussed in Section III, and some typical results are shown in Section IV.

II. MODEL DESCRIPTION

In order to accurately analyze an arbitrary semiconductor structure under all kinds of operating conditions, the basic carrier transport equations in the classical case as first given by van Roosbroeck [12] must be solved.

$$\text{div } \epsilon \text{ grad } \psi = -q(p - n + N_D^+ - N_A^-) \quad (\text{Poisson's equation}) \quad (1)$$

$$\left. \begin{aligned} \text{div } J_n - q \frac{\partial n}{\partial t} &= qR \\ \text{div } J_p + q \frac{\partial p}{\partial t} &= -qR \end{aligned} \right\} \quad (\text{continuity equations}) \quad (2)$$

$$\left. \begin{aligned} J_n &= -q(\mu_n n \text{ grad } \psi - D_n \text{ grad } n) \\ J_p &= -q(\mu_p p \text{ grad } \psi + D_p \text{ grad } p) \end{aligned} \right\} \quad (\text{current relations}). \quad (3)$$

These given equations can be solved for steady-state operation by an iterative scheme given first by Gummel [13]. Normalizing (1)–(5) in the same way as de Mari [14] did, the steady-state equations become

$$\begin{aligned} \text{div grad } \psi &= n - p - C \\ \text{div } J_n &= R \\ \text{div } J_p &= -R \\ J_n &= -\mu_n (n \text{ grad } \psi - \text{grad } n) \\ J_p &= -\mu_p (p \text{ grad } \psi + \text{grad } p). \end{aligned} \quad (4)$$

The assumptions, which have to be made to obtain these equations are

$$\begin{aligned} &\text{homogeneity of the permittivity} \\ \epsilon_{\text{SEM}} &= \text{const} \quad \epsilon_{\text{OXID}} = \text{const} \end{aligned} \quad (5)$$

total ionization of all impurities

$$C = N_D - N_A = N_D^+ - N_A^- \quad (8)$$

The model implemented in the MINIMOS program assumes some additional simplifications, which are good approximations in most MOS-transistor simulations:

no bandgap narrowing

$$n_i = \text{const} \quad (9)$$

no recombination and generation

$$R = \phi \quad (10)$$

only channel carriers contribute to current flow

$$\text{if n-channel device: } J_p = \phi$$

$$\text{if p-channel device: } J_n = \phi \quad (11)$$

homogeneous temperature distribution all over the device

$$T = \text{const.} \quad (12)$$

The device temperature is kept constant, but can be varied within the range of 250–450 K.

Thus the model is reduced to the following nonlinear system of partial differential equations:

For n-channel devices:

$$\text{div grad } \psi = \exp(\psi - \phi_n) - \exp(\phi_p - \psi) - C$$

$$\text{div } J_n = \phi$$

$$J_n = -\mu_n n \text{ grad } \phi_n$$

$$\phi_p = \text{const (that is: } J_p = \phi). \quad (13a)$$

For p-channel devices:

$$\text{div grad } \psi = \exp(\psi - \phi_n) - \exp(\phi_p - \psi) - C$$

$$\text{div } J_p = \phi$$

$$J_p = -\mu_p p \text{ grad } \phi_p$$

$$\phi_n = \text{const (that is: } J_n = \phi). \quad (13b)$$

It should be noted that substrate currents cannot be calculated with this model directly, because recombination and generation are neglected and the quasi-Fermi level of the bulk majority carriers is assumed to be constant. However, a fairly satisfying estimation is obtainable in calculating the ionization integral over the whole device [15]. The reasonability of the simplifications introduced thus follows.

The most important input parameter is, without any doubt, the doping profile. As two-dimensional doping profiles have not been analyzed in detail, as far as we know, the MINIMOS program offers several possibilities for the definition of the doping profile [16]. First an approximation, which is satisfactorily accurate in many cases, can be calculated by MINIMOS itself with analytic expressions in closed form [17]–[19]. Secondly SUPREM, the Stanford University Process Engineering Models program [20], may be used to calculate specific vertical profile shapes very accurately, which are fitted in the lateral direction. The third way is to define a doping profile point by point, which of course is the most complicated

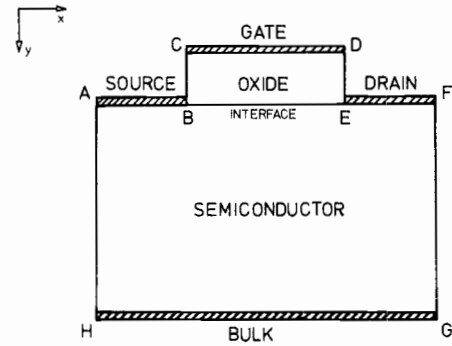


Fig. 1. The basic simulation geometry.

way, but offers the practicability to simulate DIMOS structures, for example, and even more complex structures.

The physical parameters, which have to be modeled are the thermo voltage (U_T), the intrinsic number (n_i), and the carrier mobilities (μ_n, μ_p).

$$U_T = U_T(T) = \frac{kT}{q} \quad (\text{V})$$

$$n_i = n_i(T) = 3.88 \times 10^{16} T^{3/2} \exp(-7000/T) \text{ (cm}^{-3}\text{)},$$

$$\mu_n = \mu_n(T, E_p, E_T, y, C, n) \text{ (cm}^2/\text{V} \cdot \text{s)}$$

$$\mu_p = \mu_p(T, E_p, E_T, y, C, p) \text{ (cm}^2/\text{V} \cdot \text{s}). \quad (14)$$

Since published mobility models [21]–[23] do not seem to be satisfactory, a completely new mobility model has been developed [24]. We assume mobility to be a function of temperature (T), the electric-field component parallel to the direction of current flow (E_p), the electric-field component perpendicular to the Si-SiO₂ interface (E_T), the distance to this interface (y), the concentration of impurities (C), and the mobile carrier density (n or p), respectively. The implemented formulas are given in detail in Appendix I.

III. NUMERICAL TREATMENT

In the following explanations only n-channel devices are considered, as the only difference in p-channel devices is in the change of some signs and constants.

The set of equations determined in [13] with the electric potential (ψ) and the quasi-Fermi level of the electrons (ϕ_n) can be linearized and solved either iteratively [13] or simultaneously. The simultaneous solution is quite a numerical job and offers major advantages only under special conditions [10]; thus we conclude that the iterative way is preferable [16]. To solve the partial differential equations, we have chosen the method of finite differences. The basic geometry we use for simulation is given in Fig. 1.

A. Poisson's Equation

If we linearize the first of the equations in (13a) we obtain

$$\psi_{\text{EXACT}} = \psi + \delta$$

$$\text{div grad } \delta - \delta(n + p) = n - p - C - \text{div grad } \psi + 0(\delta^2).$$

(15)

Equation (15) is an elliptic differential equation, a so-called

"Helmholtz" equation. The discretization of this equation to finite differences can be done with standard methods [25], [26] without any difficulty. Care has to be taken only with the discretization of the interface (line *BE* in Fig. 1), because of the discontinuity of the space charge. In the oxide region, Poisson's equation reduces to the simpler Laplacian equation

$$\text{div grad } \psi = \phi. \quad (16)$$

B. Boundary Conditions for the Electric Potential

At the contacts (*AB*: Source, *CD*: Gate, *EF*: Drain, *GH*: Bulk), which are assumed to be ohmic, the potential is kept constant to the applied voltage plus the appropriate built-in voltage caused by the doping.

At the interface, the electric potential has to obey the law of Gauss (17), which is the guiding principle for the discretization

$$\left(\epsilon_{OX} \frac{\partial \psi}{\partial y} \right)_{OX} = \left(\epsilon_{SEM} \frac{\partial \psi}{\partial y} \right)_{SEM}. \quad (17)$$

At the vertical boundaries (*AH*, *CB*, *DE*, *FG*), the lateral electric field has to vanish. This can easily be implemented by mirroring the electric potential at the boundary [25].

C. Continuity Equation

For the solution of the continuity equation the efficient difference approximations, which have been proposed by Scharfetter and Gummel [23], are extended to two dimensions.

Because of the large validity range of these difference approximations, which was one of the main reasons for our decision, only a few mesh points are required for accurate calculations. However, it should be noted that various other methods have been published, e.g., [2], [4].

D. Boundary Conditions for the Continuity Equation

At the source contact (*AB*) and the drain contact (*EF*) the carrier density is kept constant to the value of the doping concentration.

At the interface (*BE*) no current component in the *y* direction is allowed.

At the vertical boundaries (*AH*, *FG*) the lateral current component has to vanish. At the bulk contact (*HG*) no current components are allowed.

Some detail on the difference approximations are given in Appendix II. For a basic background see [25]–[27].

E. Mesh and Initial Guess

The mesh is nonuniform and generated automatically to account for bias values and the doping profile. It is made such as to keep the potential drop between neighboring mesh points to less than 10 thermo-voltages. The minimum mesh size is 25 times 25 nodes; the maximum size is 60 times 60 nodes. As the actual number of mesh points contributes significantly to the necessary computer time and computer memory, the estimation of the optimal mesh size has to be performed very carefully. With similar extensive care an initial solution has to be calculated. We use one-dimensional fits based on the standard semiconductor theory followed by a simultaneous solution of a system consisting of the two-dimensional Poisson

equation and the one-dimensional continuity equation. If the potential drop between neighboring mesh points is too large after this simulation step, the actual mesh is refined and the initial solution is recalculated, until a desirable configuration is obtained.

F. Solution

The SIP method of Stone [28] turned out to work best for both the Poisson's equation and the continuity equation. The relaxation methods [20], [22] do not converge as fast as desired. The method of Dupont, Kendall, and Rachford [29] is probably comparable to the SIP method concerning solution time, but the overhead computing seems to be more complex. Thus the SIP method has been preferred.

A geometrically spaced set of six or nine cyclically varied iteration parameters is used with the SIP method, similar to Stone's idea. In case of Poisson's equation, the maximum iteration parameter can easily and directly be estimated as explained in [28]. In case of the continuity equation, a fairly small value (0.25) has to be chosen as the maximum iteration parameter. An accurate theoretical explanation of this fact was not obtainable. It can be found in the rather poor condition (non-Hermitian) of the continuity equation.

Local iteration parameters, as proposed by Jesshope [30], have been tried, but no real improvement could be observed. The stopping criterion for the iteration process is an absolute error in the electric potential of 10^{-4} thermo-voltages. This small error can be obtained within 3 to 100 linearization cycles at the most, depending mainly on bias values. The total simulation time for one operating point is within 5 to 60 s central processor time on a CDC Cyber 74 computer depending on bias values and doping profile.

IV. RESULTS

In this section we want to present some typical applications. It is not easy to provide interesting results for the experienced reader, which are also impressive and easy to understand for readers with general interest in modeling but without specific knowledge of MOS devices. We have chosen the effects of ion implantation on short-channel devices for the purpose of demonstrating the use of MINIMOS. Three devices are calculated whose properties become apparent from the original simulation input decks presented in Fig. 2. The following discussion of Fig. 2 shall also demonstrate the ease of using the MINIMOS program.

The first line is a title line, which is used only to identify the output pages. The input syntax is totally based on a master key, key, and value structure. The next input line, which is the "DEVICE" statement, characterizes the device. Specified is an n-channel device (CHANNEL=N) with an aluminum gate (GATE=AL), an oxide thickness of 500 Å (TOX=500.E-8), a channel width of 10 μm (W=10.E-4) and a channel length of 1 μm (L=1.E-4). The "BIAS" statement specifies the operating point. We choose a drain voltage of 2 V (UD=2.) and a gate voltage of 0 V (UG=φ). The substrate voltage is assumed to be zero by MINIMOS, if not specified explicitly. The "PROFILE" statement specifies the substrate doping and the source-drain diffusion. In the examples presented here we used the simplest

```

ONE - MICRON ANALYSIS (DEVICE 1)
DEVICE CHANNEL=N GATE=AL TOX=500.E-8 W=10.E-4 L=1.E-4
BIAS UD=2. UG=0.
PROFILE NB=1.E15 ELEM=PH DOSE=1.E15 AKEV=40 TOX=500.E-8
+ TEMP=1000 TIME=900
END

```

```

ONE - MICRON ANALYSIS (DEVICE 2)
DEVICE CHANNEL=N GATE=AL TOX=500.E-8 W=10.E-4 L=1.E-4
BIAS UD=2. UG=0.
PROFILE NB=1.E15 ELEM=PH DOSE=1.E15 AKEV=40 TOX=500.E-8
+ TEMP=1000 TIME=900
IMPLANT ELEM=B DOSE=3.E11 AKEV=20 TEMP=900 TIME=900
END

```

```

ONE - MICRON ANALYSIS (DEVICE 3)
DEVICE CHANNEL=N GATE=AL TOX=500.E-8 W=10.E-4 L=1.E-4
BIAS UD=2. UG=0.
PROFILE NB=1.E15 ELEM=PH DOSE=1.E15 AKEV=40 TOX=500.E-8
+ TEMP=1000 TIME=900
IMPLANT ELEM=B DOSE=3.E11 AKEV=20 TEMP=900 TIME=900
IMPLANT ELEM=B DOSE=2.E11 AKEV=120
END

```

Fig. 2. Some typical input decks.

way of defining a doping profile, which is the direct calculation by MINIMOS. The other possibilities have been explained above. A substrate doping of 10^{15} cm^{-3} ($\text{NB}=1.\text{E}15$) and a source-drain implantation with phosphorus ($\text{ELEM}=\text{PH}$), an implantation dose of 10^{15} cm^{-2} ($\text{DOSE}=1.\text{E}15$) and an implantation energy of 40 keV ($\text{AKEV}=40$) is specified. The implantation is done through an isolation oxide of 500 Å ($\text{TOX}=500.\text{E}-8$) and an annealing step is performed at 1000°C ($\text{TEMP}=1000$) for 900 s ($\text{TIME}=900$). The second input deck has an "IMPLANT" statement, which defines a channel implantation with boron ($\text{ELEM}=\text{B}$), a dose of $3 \times 10^{11} \text{ cm}^{-2}$ ($\text{DOSE}=3.\text{E}11$), an energy of 20 keV ($\text{AKEV}=20$), annealed at 900°C ($\text{TEMP}=900$) for 900 s ($\text{TIME}=900$). The third input deck has an additional "IMPLANT" statement specifying a second, deeper channel implantation with boron ($\text{ELEM}=\text{B}$), a dose of $2 \times 10^{11} \text{ cm}^{-2}$ ($\text{DOSE}=2.\text{E}11$), and an energy of 120 keV ($\text{AKEV}=120$). It is assumed that both channel implantation steps are annealed at the same time. It is fairly well known that the first of our three model devices is "normally-on" and that the shallow implantation of device 2 is needed to obtain a "normally-off" device with positive threshold voltage. Furthermore, the deep implantation of device 3 is necessary to avoid punchthrough. These effects will now be demonstrated by two-dimensional plots of the physically relevant quantities in the interior of the three model devices.

The calculated doping density distributions are shown in Figs. 3-5. From these figures one can read the depth of the p-n junctions under source and drain being approximately 3000 Å. The surface concentration of the source and drain regions is $5 \times 10^{19} \text{ cm}^{-3}$. The effective channel length is reduced by the lateral subdiffusion to about $0.6 \mu\text{m}$. The shallow channel implantation for adjusting the threshold voltage is to be seen in Figs. 4, 5. Additionally, Fig. 5 shows the deep implantation for punchthrough suppression. The threshold voltage was barely affected by the deep implantation.

Fig. 6 shows the distribution of the electric potential for the

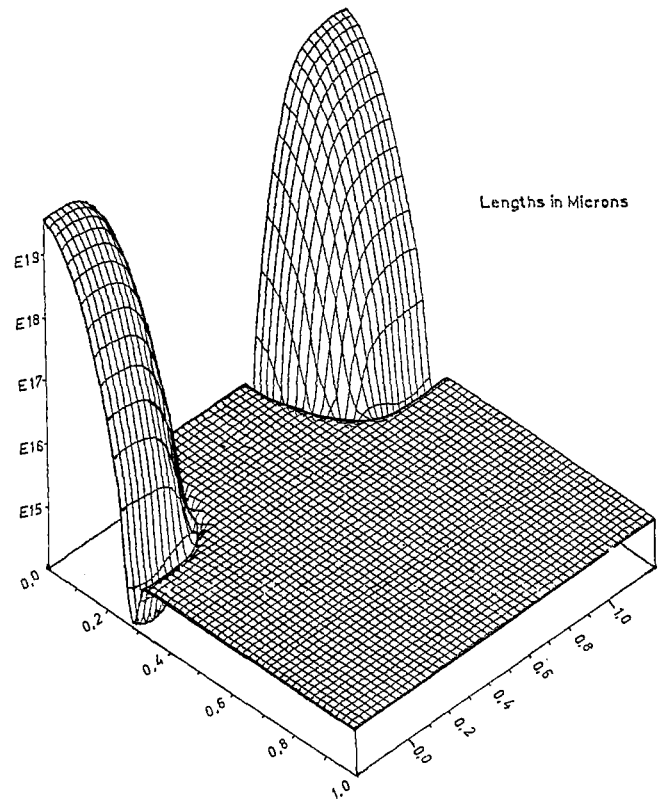


Fig. 3. Doping concentration for device 1 (cm^{-3}).

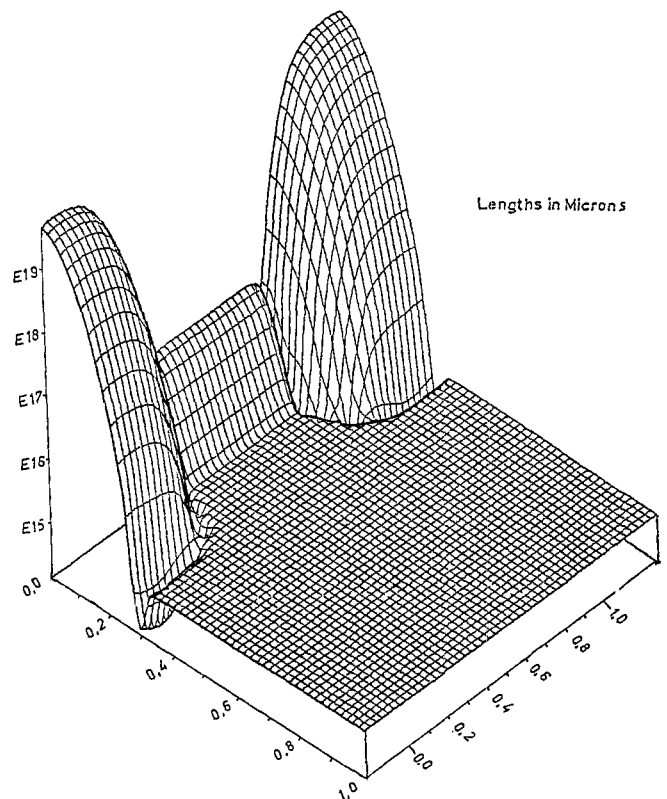
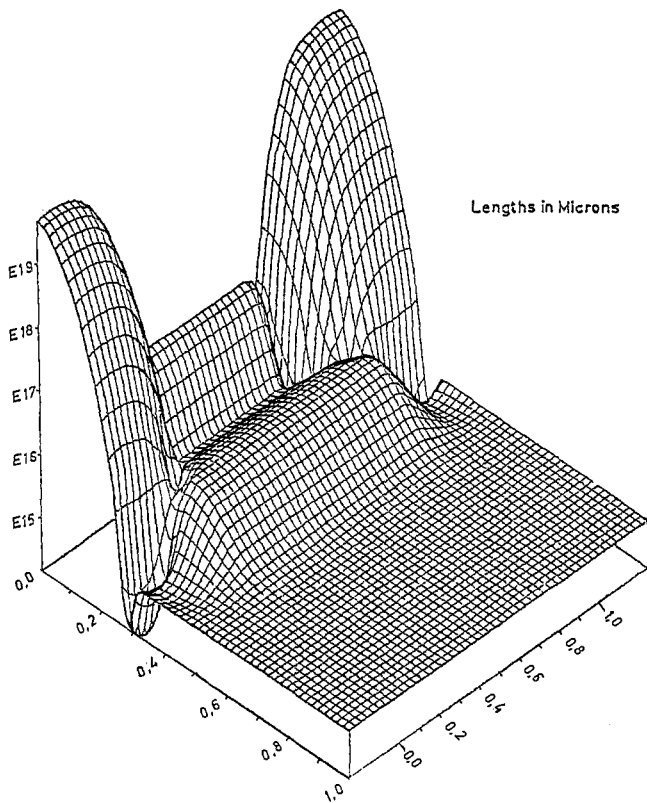
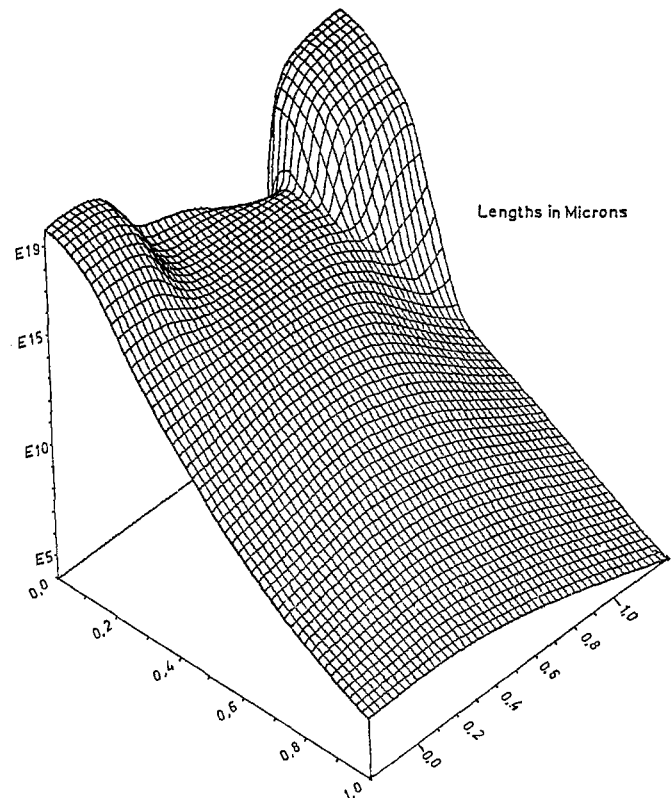
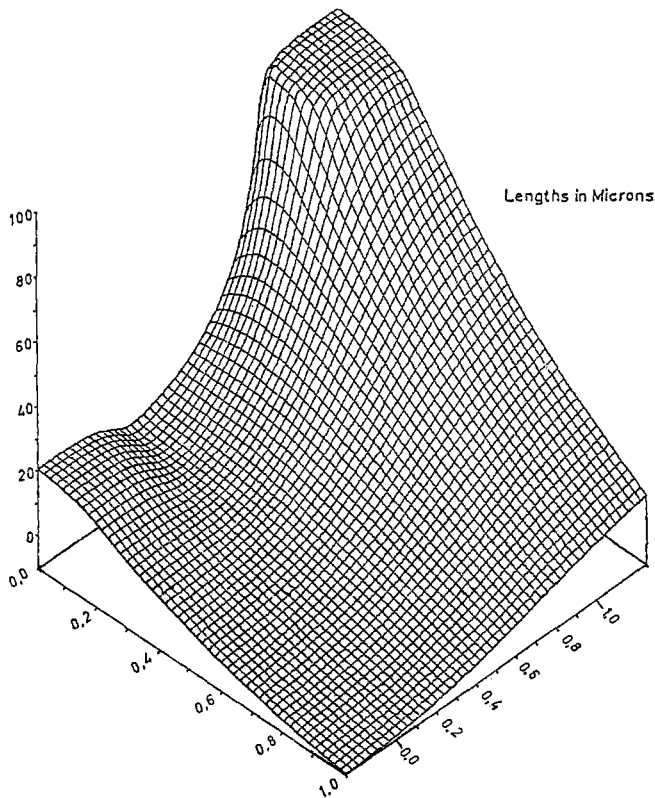


Fig. 4. Doping concentration for device 2 (cm^{-3}).

Fig. 5. Doping concentration for device 3 (cm^{-3}).Fig. 7. Concentration of electrons for device 1 (cm^{-3}).Fig. 6. Electric potential for device 1 (U_T).

first device. The drain contact is on the right-hand side. In the depletion regions of the reverse-biased drain bulk diode, the potential decreases approximately linearly and it is nearly constant in the highly doped source and drain regions. A slight barrier is visible at the source-channel diode. The potential distribution for devices 2 and 3 are not shown here, because there are hardly any differences.

Fig. 7 shows the electron distribution for the first device. The surface concentration in the channel is fairly high due to the fact of operating in the strong inversion region. As noted before, the threshold voltage for this nonchannel-implanted device is slightly negative. One also can see the carrier minimum near the drain contact representing the pinchoff region.

Fig. 8 shows the concentration of electrons in the second device. The surface concentration has decreased in the channel area by the channel implantation, as expected. In spite of this, there occurs somewhat of a carrier channel at a depth of about 2000 Å. This is caused by punchthrough as will become clearly apparent from the current-density distributions.

Fig. 9 shows the electron distribution in the third device. The second implantation results in a monotonic decrease of the carrier density from the transistor surface into bulk, which indicates the suppression of punchthrough.

Fig. 10 shows the lateral current density distribution in the first device. For better visibility, the plot on the right-hand side shows the complement of the current density. In the channel near the source side the current is forced to flow at

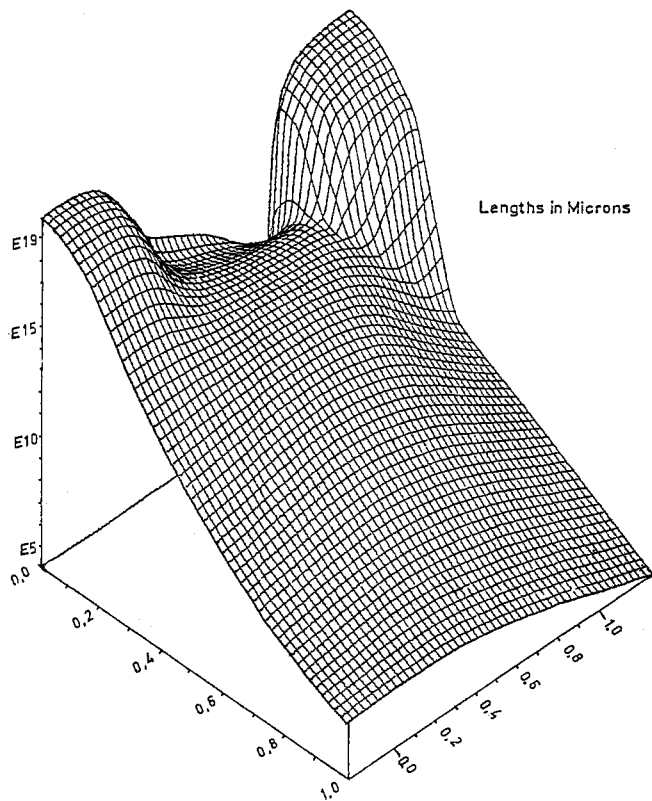


Fig. 8. Concentration of electrons for device 2 (cm^{-3}).

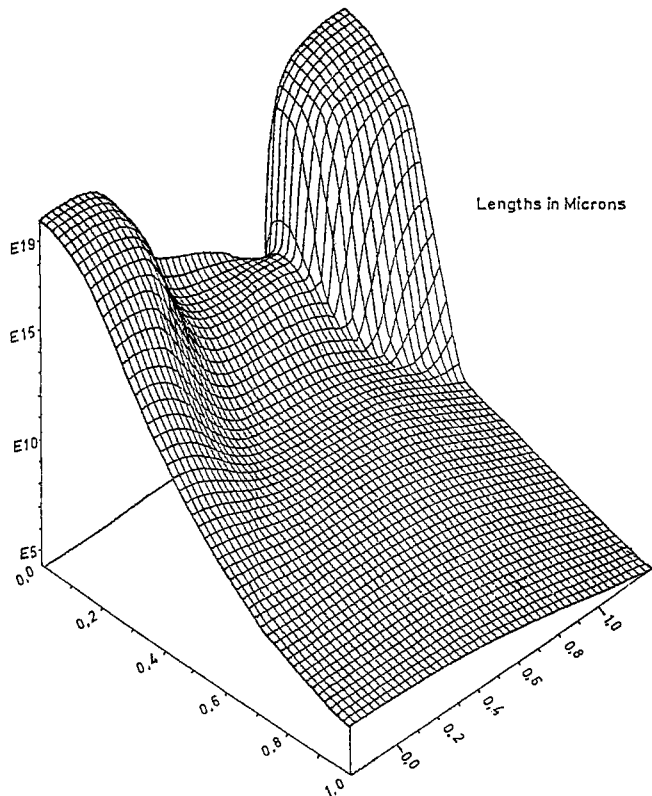


Fig. 9. Concentration of electrons for device 3 (cm^{-3}).

the surface by the transversal component of the field. But already in the middle of the channel, a typical short-channel effect, one can watch current spreading caused by the drain influence. It also should be noted that the current channel is fairly wide. The reason for this phenomenon is to be found in a kind of punchthrough mode which is partially suppressed by the high inversion condition.

The lateral current distribution and complement for the second transistor are shown in Fig. 11. As one can see, this device is operating in the punchthrough mode. The current flow takes place in a wide channel in the bulk. An additional thin current sheet at the surface is also apparent.

Fig. 12 shows the lateral current distribution and complement for the third device. The second channel implantation results in a suppression of punchthrough in this operating point. The entire current flows at the semiconductor surface. The two small additional peaks in these plots are not at all arbitrary. They may easily be understood by physical reasoning: the current starts to flow in a thin area below the source contact. It spreads out in the n-doped source region first and is forced to a thin current sheet in the channel afterwards. The influence of the drain region widens this channel again in the pinchoff area. Below the drain contact, the current flows again in a thin area because it has to pass through the contact.

The output characteristics for a gate voltage of 1 V are shown in Fig. 13. For comparison, the simulation results without mobility reduction are shown as dashed curves. A decisive influence of this effect can be seen. It is most pronounced for device 1 which hardly shows any saturation without mobility reduction.

Fig. 14 shows the subthreshold characteristics for two different drain voltages. The full drawn lines denote 2 V, the dashed lines 100 mV. The slope is the same for all three devices at a drain voltage of 100 mV. It is decreased at 2-V drain voltage for devices 1 and 2 by an additional punchthrough current. The shift of the characteristics for different drain voltages, which is caused by the short-channel effect, is also a minimum for device 3.

Comparison of MINIMOS simulation results with experimental data has shown that good agreement can be obtained [16]. We do not repeat this comparison here because a real proof of the validity of a simulation program like MINIMOS is only possible in comparing a wide range of different devices by various users. Therefore, we invite every interested reader to check MINIMOS himself, as it is available to everybody for just the handling costs.

V. CONCLUSION

In this paper we describe a user-oriented program package for the two-dimensional numerical simulation of planar MOS transistors. Sophisticated programming techniques and optimal numerical algorithms allow very low computer costs. Our motivation for the development of this program was

to gain more principle physical understanding of MOS transistors,

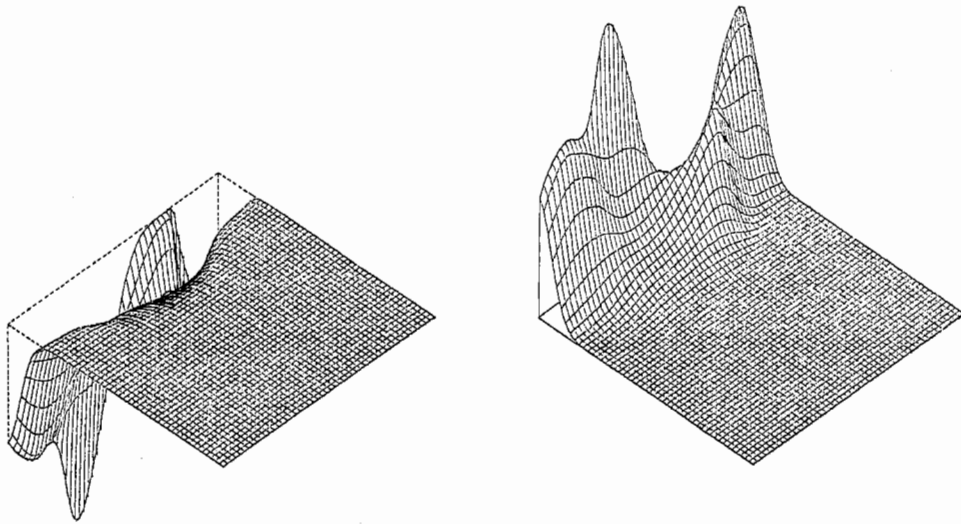


Fig. 10. Lateral current density for device 1.

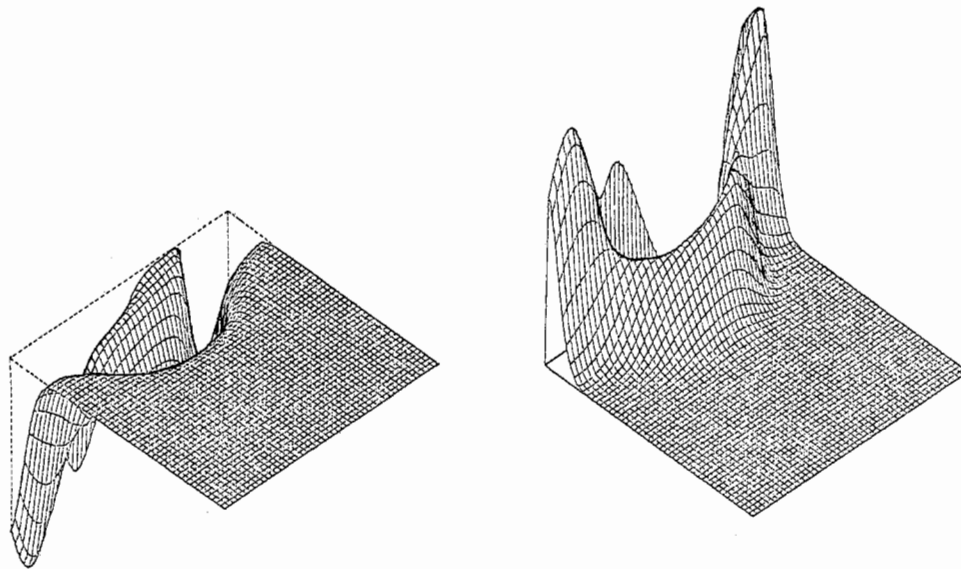


Fig. 11. Lateral current density for device 2.

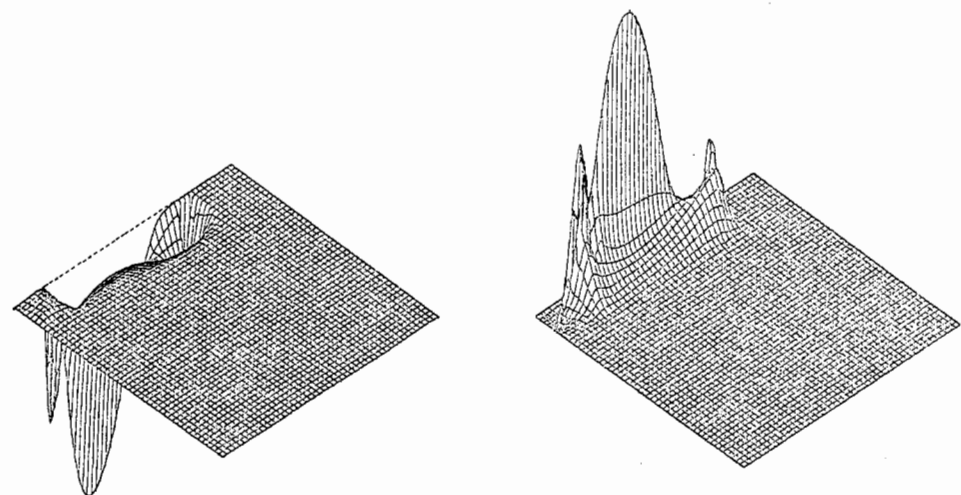
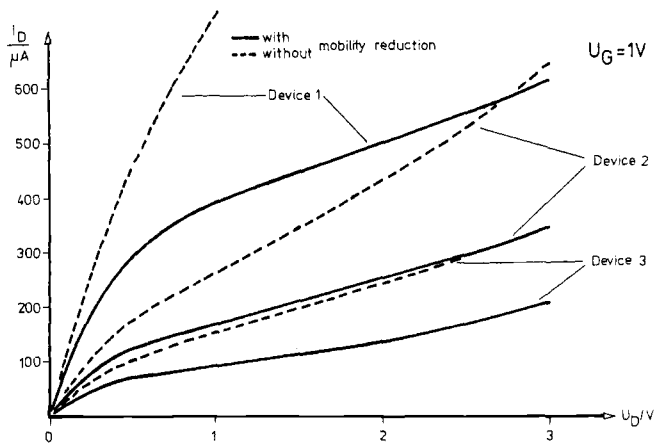
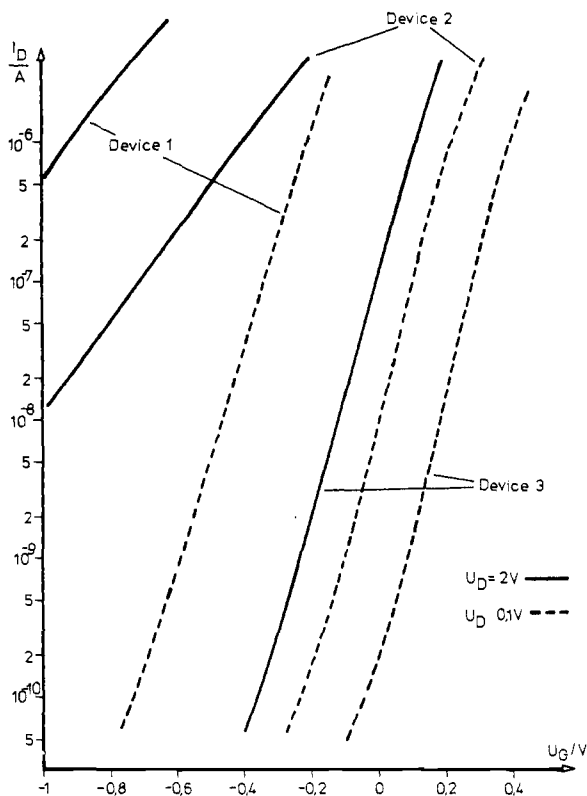


Fig. 12. Lateral current density for device 3.


 Fig. 13. Output characteristics with $U_G = 1$ V.

 Fig. 14. Subthreshold characteristics with $U_D = 0.1$ V (dashed lines) and $U_D = 2$ V (full drawn lines).

to bridge the gap between technology modeling and circuit design,
to provide both designers and technologists with an easy usable but yet accurate MOS simulation program.

It has been shown in this paper that these goals have been achieved by the program. This has been demonstrated by calculating the two-dimensional shapes of the relevant physical quantities and the current-voltage characteristics of 1- μm gate length MOST's differing in the ion implantation steps. Many features become apparent, which are not accessible to measurement such as the carrier density and current density distributions within the devices. The same holds true for the influence of mobility reduction effects, which is directly seen

from two sets of output characteristics. It is hoped that MINIMOS will be broadly used as it is available to everyone and keeps the computer costs uniquely low.

APPENDIX I

In this section the formulas for electron and hole mobility are given. The detailed derivation with all references will be published separately [24].

A. Electron Mobility

The mobility is merged out of two components mainly

$$\mu_n(T, E_P, E_T, y, C, n) = (1/\mu LI^\beta + 1/\mu EPET^\beta)^{-1/\beta}.$$

The merging function is a type of Mathiessens rule with a temperature dependent weight [32]

$$\beta = 2.57 \times 10^{-2} T^{0.66}.$$

μLI describes the influence of lattice scattering, impurity scattering, and screening as a function of temperature. Thus $\mu LI = \mu LI(T, C, n)$.

$\mu EPET$ describes the influence of velocity saturation and surface scattering as a function of temperature and the distance to the Si-SiO₂ interface. Thus

$$\mu EPET = \mu EPET(T, E_P, E_T, y).$$

μLI is also constructed from two components; where μL denotes the pure lattice mobility as a function of temperature and μI denotes the impurity scattering mobility after Brooks [33]

$$\mu L = 7.12 \times 10^8 T^{-2.3} \quad (\text{cm}^2/\text{V} \cdot \text{s})$$

$$\mu I = \frac{7.3 \times 10^{17} T^{1.5}}{C \cdot f \left(\frac{1.52 \times 10^{15} T^2}{n} \right)} \quad (\text{cm}^2/\text{V} \cdot \text{s})$$

with $f(x) = \ln(1+x) - x/(1+x)$.

These two mobility components are merged by a formula given first by Debye [34]

$$\mu LI = \mu L \left(1 + g \left(\left(\frac{6\mu L}{\mu I} \right)^{1/2} \right) \right)$$

with

$$g(x) = x^2 \left(Ci(x) \cos(x) + \sin(x) \left(Si(x) - \frac{\pi}{2} \right) \right).$$

$\mu EPET$ is also built up from two parts, where μEP describes the influence of velocity saturation (hot-electron effect) and μET models surface scattering

$$\mu EP = \frac{1.53 \times 10^9 T^{-0.87}}{-E_P} \cdot \left(\frac{y + 10^{-7}}{y + 2 \times 10^{-7}} \right)^{1/2} \quad (\text{cm}^2/\text{V} \cdot \text{s})$$

$$\mu ET = 10^8 \cdot (y + 2 \times 10^{-7})^{1/2} \cdot h(E_T)^{-1/2} \quad (\text{cm}^2/\text{V} \cdot \text{s})$$

with $h(x) = x + (x^2)^{1/2}$.

These two parts are combined empirically with a Mathiessens rule with the weight 2

$$\mu EPET = (1/\mu EP^2 + 1/\mu ET^2)^{-1/2}.$$

Some of the constants given in this survey are certainly debatable and will probably be updated after modeling a wide range of different types of devices. However, using these values we have obtained so far excellent quantitative agreement of simulation and measurement in our studies.

B. Hole Mobility

As the formulas for hole mobility are identical according to the mathematical structure with the formulas for electron mobility, they are just summarized in this section in a straightforward manner to show the relevant constants.

Let

$$\mu L = 1.35 \times 10^8 T^{-2.2} \quad (\text{cm}^2/\text{V} \cdot \text{s})$$

and

$$\mu I = \frac{5.6 \times 10^{17} T^{1.5}}{C \cdot f \left(\frac{2.5 \times 10^{15} T^2}{p} \right)} \quad (\text{cm}^2/\text{V} \cdot \text{s})$$

then

$$\mu LI = \mu L \left(1 + g \left(\left(\frac{6\mu L}{\mu I} \right)^{1/2} \right) \right).$$

Let

$$\mu EP = \frac{1.62 \times 10^8 T^{-0.52}}{E_P} \cdot \left(\frac{y + 2 \times 10^{-7}}{y + 4 \times 10^{-7}} \right)^{1/2} \quad (\text{cm}^2/\text{V} \cdot \text{s})$$

and

$$\mu ET = 2.6 \times 10^8 \cdot (y + 4 \times 10^{-7})^{1/2} \cdot h(-E_T)^{-1/2} \quad (\text{cm}^2/\text{V} \cdot \text{s})$$

then

$$\mu EPET = (1/\mu EP^2 + 1/\mu ET^2)^{-1/2}.$$

Let

$$\beta = 0.46 T^{0.17}$$

then

$$\mu_p(T, E_P, E_T, y, C, p) = (1/\mu LI^\beta + 1/\mu EPET^\beta)^{-1/\beta}.$$

The functions f , g , h are identical for electron mobility and hole mobility.

APPENDIX II

In this section some formulas for the discretized Poisson equation and the discretized continuity equation are given. Fig. 15 shows a typical finite-difference node scheme to which we refer in the following formulas.

A. Poisson's Equation in the Semiconductor Region

Let

$$e_{ij} = 0.5 (x_i + x_{i-1}) (y_j + y_{j-1})$$

and

$$f_{ij} = (y_j + y_{j-1})/x_i$$

$$g_{ij} = (x_i + x_{i-1})/y_j$$

$$r_{ij} = 1/(e_{ij}(n_{ij} + \exp(\phi_p - \psi_{ij})) + f_{ij} + f_{i-1j} + g_{ij} + g_{ij-1})$$

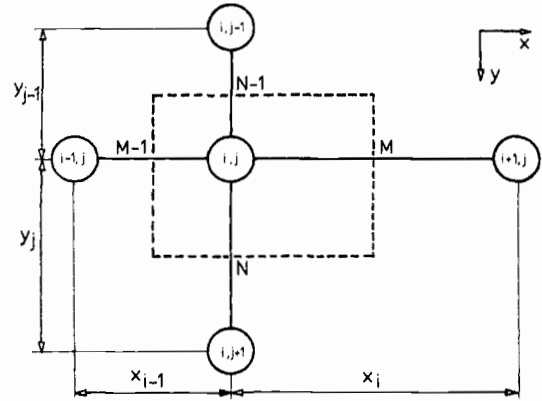


Fig. 15. Typical node for finite differences.

$$a_{ij} = f_{ij} r_{ij}$$

$$b_{ij} = f_{i-1j} r_{ij}$$

$$c_{ij} = g_{ij} r_{ij}$$

$$d_{ij} = g_{ij-1} r_{ij}$$

then

$$\begin{aligned} \delta_{ij} = & a_{ij}(\delta_{i+1j} + \psi_{i+1j} - \psi_{ij}) + b_{ij}(\delta_{i-1j} + \psi_{i-1j} - \psi_{ij}) \\ & + c_{ij}(\delta_{ij+1} + \psi_{ij+1} - \psi_{ij}) + d_{ij}(\delta_{ij-1} + \psi_{ij-1} - \psi_{ij}) \\ & + e_{ij} r_{ij} (C_{ij} - n_{ij} + \exp(\phi_p - \psi_{ij})). \end{aligned}$$

B. Poisson's Equation at the Interface

Let

$$j = k \text{ denote the interface line}$$

$$\gamma = \epsilon_{\text{OXID}}/\epsilon_{\text{SEM}}$$

$$e_{ik} = 0.5 (x_i + x_{i-1}) y_k$$

$$f_{ik} = (y_k + \gamma y_{k-1})/x_i$$

$$g_{ik} = (x_i + x_{i-1})/y_k$$

$$r_{ik} = 1/(e_{ik}(n_{ik} + \exp(\phi_p - \psi_{ik})) + f_{ik} + f_{i-1k} + g_{ik} + \gamma g_{ik-1})$$

$$a_{ik} = f_{ik} r_{ik}$$

$$b_{ik} = f_{i-1k} r_{ik}$$

$$c_{ik} = g_{ik} r_{ik}$$

$$d_{ik} = \gamma g_{ik-1} r_{ik}$$

then

$$\begin{aligned} \delta_{ik} = & a_{ik}(\delta_{i+1k} + \psi_{i+1k} - \psi_{ik}) + b_{ik}(\delta_{i-1k} + \psi_{i-1k} - \psi_{ik}) \\ & + c_{ik}(\delta_{ik+1} + \psi_{ik+1} - \psi_{ik}) + d_{ik}(\delta_{ik-1} + \psi_{ik-1} - \psi_{ik}) \\ & + e_{ik} r_{ik} (C_{ik} - n_{ik} + \exp(\phi_p - \psi_{ik})). \end{aligned}$$

C. Continuity Equation in the Semiconductor region

Let

$$\xi(x) = \frac{x}{\exp(x) - 1} \quad (\text{Bernoulli function})$$

$$e_{ij} = \frac{\mu_M \xi(\psi_{ij} - \psi_{i+1j})}{x_i(x_i + x_{i-1})}$$

$$f_{ij} = \frac{\mu_{M-1} \xi(\psi_{ij} - \psi_{i-1j})}{x_{i-1}(x_i + x_{i-1})}$$

$$g_{ij} = \frac{\mu_N \xi(\psi_{ij} - \psi_{ij+1})}{y_j(y_j + y_{j-1})}$$

$$h_{ij} = \frac{\mu_{N-1} \xi(\psi_{ij} - \psi_{ij-1})}{y_{j-1}(y_j + y_{j-1})}$$

$$r_{ij} = \frac{1}{e_{ij} + f_{ij} + g_{ij} + h_{ij}}$$

$$a_{ij} = e_{ij} r_{ij} \exp(\psi_{ij} - \psi_{i+1j})$$

$$b_{ij} = f_{ij} r_{ij} \exp(\psi_{ij} - \psi_{i-1j})$$

$$c_{ij} = g_{ij} r_{ij} \exp(\psi_{ij} - \psi_{ij+1})$$

$$d_{ij} = h_{ij} r_{ij} \exp(\psi_{ij} - \psi_{ij-1})$$

then

$$n_{ij} = a_{ij} n_{i+1j} + b_{ij} n_{i-1j} + c_{ij} n_{ij+1} + d_{ij} n_{ij-1}.$$

D. Continuity Equation at the Interface

Let

$j = k$ denote the interface line

$$\xi(x) = \frac{x}{\exp(x) - 1}$$

$$e_{ik} = \frac{\mu_M \xi(\psi_{ik} - \psi_{i+1k})}{x_i(x_i + x_{i-1})}$$

$$f_{ik} = \frac{\mu_{M-1} \xi(\psi_{ik} - \psi_{i-1k})}{x_{i-1}(x_i + x_{i-1})}$$

$$g_{ik} = \frac{\mu_N \xi(\psi_{ik} - \psi_{ik+1})}{y_k^2}$$

$$r_{ik} = \frac{1}{e_{ik} + f_{ik} + g_{ik}}$$

$$a_{ik} = e_{ik} r_{ik} \exp(\psi_{ik} - \psi_{i+1k})$$

$$b_{ik} = f_{ik} r_{ik} \exp(\psi_{ik} - \psi_{i-1k})$$

$$c_{ik} = g_{ik} r_{ik} \exp(\psi_{ik} - \psi_{ik+1})$$

then

$$n_{ik} = a_{ik} n_{i+1k} + b_{ik} n_{i-1k} + c_{ik} n_{ik+1}.$$

The Bernoulli function $\xi(x)$ must be evaluated very carefully for maximum accuracy [31].

ACKNOWLEDGMENT

The authors wish to thank Dr. D. Schornböck and the whole staff of the computer center for the excellent computer access and Prof. Dr. E. Bonek for critically reading our manuscript.

REFERENCES

- [1] D. P. Kennedy and R. R. O'Brien, "Two dimensional analysis of J.F.E.T. structures containing a low conductivity substrate," *Electron. Lett.*, vol. 7, pp. 714-716, 1971.
- [2] D. Vadorpe, J. Borel, G. Merckel, and P. Saintot, "An accurate two-dimensional numerical analysis of the MOS transistor," *Solid-State Electron.*, vol. 15, pp. 547-557, 1972.

- [3] J. W. Slotboom, "Computer aided two-dimensional analysis of bipolar transistors," *IEEE Trans. Electron Devices*, vol. ED-20, pp. 669-679, 1973.
- [4] M. S. Mock, "A two-dimensional mathematical model of the insulated gate field effect transistor," *Solid-State Electron.*, vol. 16, pp. 601-609, 1973.
- [5] H. H. Heimeier, "A two-dimensional numerical analysis of bipolar transistors," *IEEE Trans. Electron Devices*, vol. ED-20, pp. 708-714, 1973.
- [6] O. Manck, H. H. Heimeier, and W. L. Engl, "High injection in a two-dimensional transistor," *IEEE Trans. Electron Devices*, vol. ED-21, pp. 403-409, 1974.
- [7] S. P. Gaur and D. H. Navon, "Two-dimensional carrier flow in a transistor structure under non isothermal conditions," *IEEE Trans. Electron Devices*, vol. ED-23, pp. 50-57, 1976.
- [8] N. Kotani and S. Kawazu, "Computer analysis of punch through in MOSFETs," *Solid-State Electron.*, vol. 22, pp. 63-70, 1979.
- [9] T. Toyabe and S. Asai, "Analytical models of threshold voltage and breakdown voltage of short-channel MOSFET's derived from two-dimensional analysis," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 453-461, 1979.
- [10] P. E. Cotrell and E. M. Buturla, "Two-dimensional static and transient simulation of mobile carrier transport in a semiconductor," in *Proc. NASECODE I Conf.*, pp. 31-64, 1979.
- [11] A. R. Newton, J. D. Crawford, and D. O. Pederson, "Computer aids to LSI and digital systems design," presented at the Katholieke Universiteit Leuven, Belgium, Summer Course 1978.
- [12] W. V. Van Roosbroeck, "Theory of flow of electrons and holes in germanium and other semiconductors," *Bell Syst. Tech. J.*, vol. 29, pp. 560-607, 1950.
- [13] H. K. Gummel, "A self consistent iterative scheme for one-dimensional steady state transistor calculations," *IEEE Trans. Electron Devices*, vol. ED-11, pp. 445-465, 1964.
- [14] A. De Mari, "An accurate numerical steady state one-dimensional solution of the pn-junction," *Solid-State Electron.*, vol. 11, pp. 38-58, 1968.
- [15] T. Toyabe, K. Yamaguchi, S. Asai, and M. Mock, "A numerical model of avalanche breakdown in MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 825-832, 1978.
- [16] S. Selberherr, W. Fichtner, and H. W. Pötzl, "MINIMOS—A program package to facilitate MOS device design and analysis," in *Proc. NASECODE I Conf.*, pp. 275-279, 1979.
- [17] D. P. Kennedy and R. R. O'Brien, "Analysis of the impurity atom distribution near the diffusion mask for a planar pn-junction," *IBM J. Res. Develop.*, pp. 179-186, 1965.
- [18] H. G. Lee, J. D. Sansbury, R. W. Dutton, and J. L. Moll, "Modeling and measurement of surface impurity profiles of lateral diffused regions," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 455-461, 1978.
- [19] H. Ryssel and I. Ruge, *Ionimplantation*. Stuttgart, Germany: Teubner, 1978.
- [20] D. Antoniadis, S. Hansen, and R. Dutton, "Suprem II—A program for IC process modeling and simulation," Stanford Electron. Lab., Stanford, CA, Tech. Rep. 5019-2, 1978.
- [21] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, pp. 2192-2193, 1957.
- [22] K. Yamaguchi, "Field-dependent mobility model for two-dimensional numerical analysis of MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 1068-1074, 1979.
- [23] D. L. Scharfetter and H. K. Gummel, "Large-signal analysis of a silicon Read diode oscillator," *IEEE Trans. Electron Devices*, vol. ED-16, pp. 64-77, 1969.
- [24] S. Selberherr, A. Schütz, and H. W. Pötzl, "A new mobility model for the two-dimensional MOS device simulation," to be published.
- [25] G. E. Forsythe and W. R. Wasow, *Finite Difference Methods for Partial Differential Equations*. New York: Wiley, 1960.
- [26] R. S. Varga, *Matrix Iterative Analysis*. Englewood Cliffs, NJ: Prentice-Hall, 1962.
- [27] D. Marsal, *Die Numerische Lösung Partieller Differentialgleichungen*. Mannheim, Germany: Bibliographisches Institut, 1976.
- [28] H. L. Stone, "Iterative solution of implicit approximations of multidimensional partial differential equations," *SIAM J. Num. Anal.*, vol. 5, pp. 530-558, 1968.
- [29] T. Dupont, R. D. Kendall, and H. H. Rachford, "An approximate factorization procedure for solving self-adjoint elliptic difference equations," *SIAM J. Num. Anal.*, vol. 5, pp. 559-573, 1968.
- [30] C. Jesshope, "Bipolar transistor modeling with numerical solu-

tions to the two-dimensional dc and transient problems," Ph.D. dissertation, University of Southampton, Southampton, England, 1976.

- [31] J. F. Hart, E. W. Cheney, C. L. Lawson, H. J. Maehly, *et al.*, *Computer Approximations*. New York: Wiley, 1968.
- [32] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical re-

lation to electric field and temperature," *IEEE Trans. Electron Devices*, vol. ED-22, pp. 1045-1047, 1975.

- [33] H. Brooks, "Theory of the electrical properties of germanium and silicon," in *Advances in Electronics and Electron Physics*, vol. 7, 1955, pp. 85-182.
- [34] P. P. Debye and E. M. Conwell, "Electrical properties of n-type germanium," *Phys. Rev.*, vol. 93, pp. 693-706, 1954.

Interactive Two-Dimensional Design of Barrier-Controlled MOS Transistors

SALLY LIU, BERNARD HOFFLINGER, MEMBER, IEEE, AND DONALD O. PEDERSON, FELLOW, IEEE

Abstract—An interactive program has been developed for the graphic generation and the solution of two-dimensional impurity, carrier, potential, and field distributions in small-geometry MOS transistor configurations. Emphasis is placed on conversational operation and three-dimensional display on a graphics terminal with a generation rate, for any self-consistent two-dimensional solution, of less than few minutes for each computation and drawing. Although this limited the approach to a solution of the potential problem only, the barrier-controlled characteristics in weak inversion and weak injection (punch-through) are produced efficiently and provide quantitative data for slopes, threshold voltages, and punchthrough voltages, as well as their two-dimensional dependence on device geometry, doping, and terminal voltages. Examples are presented for NMOS transistors with various enhancement and buried channel implants. The program is useful both as a pre-selector for structures to be simulated with a more elaborate two-dimensional potential and transport program and as a generator of parameters for a device model in a circuit simulator.

I. INTRODUCTION

WITH DECREASING transistor dimensions, it has become more difficult to describe MOS transistors with equations that are simple enough for hand calculations or programmable calculators and yet retain sufficient accuracy to provide useful information about the device characteristics [1]. Since transistor models are used widely in circuit simulators, device models compatible with these simulators have

Manuscript received December 5, 1979; revised March 27, 1980. This work was supported in part by Nixdorf Computer, Pederborn, and the Bundesministerium für Forschung und Technologie, Bonn, Germany, and by Hewlett-Packard Company and Signetics Corporation.

S. Liu and D. O. Pederson are with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720.

B. Hoefflinger is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720, on leave from the University of Dortmund, Dortmund, Germany.

received widespread attention. Current-charge-voltage equations with sets of "device parameters" are often used [2], [3]. Look-up tables for current, capacitance, and voltage have become a feasible alternative when dealing with large circuits [4], [5]. Both types of transistor representations require either available device data with parameters extracted from them [6], [7], or parameter estimates obtained from one-dimensional or pseudo-one-dimensional physical models of the transistors [1].

For the design of a new generation of transistors, an improved form of computer-oriented modeling is required. The numerical solution of the two-dimensional potential and transport equations can describe integrated field-effect transistors, and significant contributions to this problem have evolved over the past ten years [8]-[10]. In this activity, initially, idealized impurity distributions and boundaries have been assumed to facilitate solutions. However, with very small device geometries, modern process simulators show extremely inhomogeneous two-dimensional impurity distribution and shaped boundaries, which must then be considered in the potential and transport solution.

One way in attacking this complex problem is the use of very capable maxicomputers, selecting a sample situation, and developing a solution with every possible effect included. Yet what is needed even here is a more limited computer program which is efficient enough to offer quick solutions at the designer's desk. In particular, a rapid interactive design capacity needs to be established including two-dimensional device geometries, impurity distributions, and solutions for at least the most important device characteristics.

In the work reported here, program TWIST (Two-dimensional Interactive Simulation of MOS Transistors) is developed based on a minicomputer together with a graphics terminals.