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# DESIGN OF INTEGRATED CIRCUITS: DEVICE MODELING

**ABSTRACT** - The advent of Very Large Scale Integration has been an incentive to concentrate persistently on device modeling. The fundamental properties which represent the basis for all device modeling activities are summarized. The sensible use of physical and technological parameters is discussed and the most important physical phenomena which are required to be taken into account are scrutinized. The assumptions necessary to find a reasonable trade-off between efficiency and effort for a model synthesis are recollected and their thus induced limitations are explained. Modifications to bypass these limitations are pin-pointed. Simple and easy to use formulae for the physical parameters of major importance, which one has to deal with when designing a model are presented. The necessity of a careful parameter-selection, based on physical information, is shown. Various effects are documented which are of critical importance when a model for special purposes is demanded. Since different objectives for the simulation require different models, a rough classification of types of models to achieve a desired accuracy with minimal complexity is sketched. Some results of a two dimensional model are discussed with typical applications of interest for miniaturized MOS devices. Much emphasis is laid on the didactic potential of such a complex high order model. This paper cannot intend to be any more than a review. The reader with a specific interest in any one subject will find the references useful for further detail.

# 1. INTRODUCTION

The first integrated circuits which just contained a few devices became commercially available in the early 1960's. Since that time an evolution has taken place place so that today the manufacture of integrated circuits with over 400.000 transistors per single chip is possible. This advent of the so-called Very-Large-Scale-Integration (VLSI) certainly revealed the need of a better understanding of the basic device physics. The miniaturization of the single transistor, which is one of the inseparable preconditions of VLSI, brought about a collapse of the classical device models, because totally new phenomena became visible and even dominated the device behaviour. One consequence of this evidence led to an unimaginable number of suggestions of how to modify the classical models to incorporate various of the new phenomena. Additionally new activities have been initiated to explore the physical principles which make a device operationable. The number of scientific publications which utilize the terms "device analysis", "device simulation" and "device modeling" (c.f./1/) grew in an incredible manner.

At first it seems necessary to clarify these frequently used terms to facilitate the intelligibility of the subsequent chapters. Consulting a dicitionary one will find among many more the following interpretations:

Analysis
- separation of a whole into its component parts, possibly with comment and judgement
- examination of a complex, its elements, and their relations in order to learn about

Simulation
- imitative representation of the functioning of one system or process by means of the functioning of another
- examination of a problem not subject to experimentation

Modeling
- to produce a representation or simulation of a problem or process
- to make a description or analogy used to help visualize something that cannot be directly observed

Therefore, analysis is at least intended to mean "Exact Analysis" and simulation must inferentially mean "Approximate Simulation" using only to some extent physically motivated models. Modeling is necessary for analysis and simulation, but with a different objective. However, any model should at least reflect the underlying physics.

In the next section the fundamental properties which are the basis fo all device models are summarized. Much effort is laid on the documentation of various physical effects which possibly have to be taken into account when synthezising a device model for some special application. The assumptions which are usually made in order to ease modeling are presented and their validity is, at least qualitatively discussed. Simple and easy to use formulae are presented which allow to phenomenologically simulate the most important physical parameters with which the modelist has to deal. In the third section the hierarchy and objective of different types of device models is sketched. It is not our intention to simply list the details of different models, which have been published. This task has been accomplished already by excellent review papers /22/, /26/, /30/, /41/, /52/, /61/. We have tried to concentrate more on the motivation which leads to different types of models. A didactic example which should make transparent the applicability of a high order model for the analysis of device behaviour is given in the fourth section. For that purpose the influence of ion implantation in the channel region of a very small scale MOSFET on threshold voltage and punch through property has been chosen. A sophisticated application of a high order model is shown in the fifth section to demonstrate that it is possible to comprehend some complex interaction of different physical phenomena with device modeling. This is accomplished by explaining the reasons for the snap-back effect in the characteristics of a miniaturized MOSFET.

Throughout this paper all constants and quantities are given in the following units, if not specified differently: lengths in cm, times in s, temperature in K, voltages in V, currents in A. The units are often omitted to gain better a transparency of the formulae.

## 2. SOME FUNDAMENTAL PROPERTIES

In order to accurately analyze an arbitrary semiconductor structure which is intended as a self-contained device under various operating conditions, a mathematical model has to be given. The equations which form this mathematical model are often called the fundamental semiconductor equations; these will be discussed in the first chapter of this section.

The second chapter will deal with assumptions which have to be made for special applications additionally to those which have already been used in the derivation of the equations and which are beyond the scope of this presentation. Furthermore, all quantities which are involved in the basic equations will be outlined more or less qualitatively.

It will become apparent that the fundamental equations employ a set of physical and technological parameters. An in-depth analysis of all those parameters has not been finished until now - or the results of such an analysis are of overwhelming complexity - because of inherent methodical difficulties. The topic of the third chapter of this section will contain some suggestions for a heuristic simulation of the most important parameters based as it were on physical principles.

### 2.1 THE FUNDAMENTAL SEMICONDUCTOR EQUATIONS

The most familiar model of carrier transport in a semiconductor device has been proposed by Van Roosbroeck /80/. It consists of Poisson's equation (2.1-1), the current continuity equations for electrons (2.1-2) and holes (2.1-3) and the current relations for electrons (2.1-4) and holes (2.1-5)

$$\operatorname{div} \varepsilon \operatorname{grad} \psi = -q \, ( p - n + C ) \qquad (2.1\text{-}1)$$

$$\operatorname{div} \vec{J}_n = -q \, ( G - R ) \qquad (2.1\text{-}2)$$

$$\operatorname{div} \vec{J}_p = q \, ( G - R ) \qquad (2.1\text{-}3)$$

$$\vec{J}_n = -q \, ( \mu_n \, n \operatorname{grad} \psi - D_n \operatorname{grad} n ) \qquad (2.1\text{-}4)$$

$$\vec{J}_p = -q \, ( \mu_p \, p \operatorname{grad} \psi + D_p \operatorname{grad} p ) \qquad (2.1\text{-}5)$$

These relations form a system of coupled partial differential equations. Poisson's equation, which is one of Maxwell's laws, describes the charge distribution in the interior of a semiconductor device. The balance of sinks and sources for electron- and hole currents is characterized by the continuity equations. The current relations describe the absolute value, direction and orientation of electron- and hole currents. The continuity equations and the current relations can be derived from Boltzmann's equation by not at all trivial means. The ideas behind these considerations cannot be presented here due to limited space. The interested reader should refer to /80/ and its secondary literature or text books on semiconductor physics.

However, it is of prime importance to note that the equations (2.1-4) and (2.1-5) do not characterize effects which are caused by degenerate semiconductors (e.g. heavy doping). /49/, /51/, /55/, /79/, /82/ discuss some modifications of the current relations, which partially take into account the consequences introduced by degenerate semiconductors (e.g. invalidity of Boltzmann's statistics, bandgap narrowing). These modifications are not at all simple and lead to problems especially for the formulation of boundary conditions /59/, /81/. In case of modeling MOS devices, degeneracy is, owing to the relatively low doping in the channel region, practically irrelevant. For modern bipolar devices, though, bearing in mind shallow and extraordinarily heavily doped emitters, it is an absolute necessity to account for local degeneracy of the semiconductor.

Furthermore (2.1-4) and (2.1-5) do not describe velocity overshoot phenomena which become apparent at feature lengths of 0.1$\mu$m for silicon and 1$\mu$m for gallium-arsenide /27/; and certainly no effects which are due to ballistic transport the existence of which is still questionable are included. The latter start to become important for feature sizes below 0.01$\mu$m for silicon and 0.1$\mu$m for gallium-arsenide /28/. Considering the state of the art of device miniaturization neither effect does bother much the modelists of silicon devices. For gallium-arsenide devices new ideas are mandatory for the near future /27/, /56/, /57/.

## 2.2 ASSUMPTIONS AND DISCUSSION OF PARAMETERS

It is imperative to discuss the parameters of the semiconductor equations in order to get some insight into the compexity of that mathematical model and the difficulty of a more or less rigorous solution.

The permittivity $\varepsilon$ in Poisson's equation in the most general case is a rank one tensor. Because all common semiconductor materials grow in cubic crystal structure and because silicon-dioxide is amorphus no anisotropy exists and the permittivity can be treated as a scalar quantity. Furthermore, one can savely assume that the permittivity is homogenous with sufficient accuracy for even degenerate semiconductors.

The electrically active net doping concentration C in Poisson's equation is the most important technological parameter. To obtain this quantity by mathematical analysis /21/ is at least as cumbersome as to accurately analyze some semiconductor device, because the physics of the technological processes which determine the doping concentration lacks still basic understanding. The need of modeling in this area is drastically increasing in view of VLSI devices. One-dimensional process modeling is fairly well established nowadays, but two-dimensional simulations is just appearing. Some glimpses of modeling doping profiles with handy analytical expressions will be given in the next chapter. One assumption which is usually made with fairly satisfactory success is the total ionization of all dopants (2.2-1).

$$C = N_D - N_A = N_D^+ - N_A^- \qquad (2.2\text{-}1)$$

As long as the Fermi level is separated several thermal voltages from the impurity level this assumption holds quite nicely. For modern bipolar transistors, however, it certainly becomes questionable for the emitter region (degenerate material).

The electron density n and the hole density p are commonly assumed to obey Boltzmann's statistics (2.2-2).

$$n = n_i \cdot e^{(\Psi - \Phi_n)/U_T} \qquad p = n_i \cdot e^{(\Phi_p - \Psi)/U_T} \qquad (2.2\text{-}2)$$

This assumption principally neglects degeneracy; but moderate

degeneracy can be included /24/ by introducing an effective, doping dependent intrinsic number (2.2-3).

$$n_i = n_i(T,N) \qquad (2.2\text{-}3)$$

$$n_i(T,N) = n_i(T)\; e^{52.7\left(\ln(N/10^{17})+\sqrt{(\ln(N/10^{17}))^2+0.5}\right)/T}$$

$$n_i(T) = 3.88\cdot 10^{16}\cdot T^{1.5}\cdot e^{-7000/T}$$

$$N = N_D + N_A$$

The temperature dependence of the intrinsic number is based on the influence of the effective carrier masses and the bandgap. More elaborate formulae for these effects which might be imperative for low temperature applications can be found in /29/. The formula for bandgap narrowing in (2.2-3) was first suggested by Slotboom /73/. For a doping concentration of $1.3\cdot 10^{17}$ $cm^{-3}$ the intrinsic number is already increased by twenty percent.

The mobility for electrons $\mu_n$ and holes $\mu_p$ is in principal a rank one tensor function of many arguments. One ends up with a "so called" mobility after averaging and combining various physical mechanisms which are still not analyzed thouroghly enough to be modeled satisfactorily /39/. Some formulae for a mobility model for silicon will be summarized in the next chapter.

Another assumption which is unfortunately not at all free of doubts is the validity of the Einstein-Nernst relations (2.2-4).

$$D_n = \mu_n \cdot U_T \qquad D_p = \mu_p \cdot U_T \qquad (2.2\text{-}4)$$

Some guidelines on how to extend these relations for degenerate material are given in e.g. /3/. It is important to remember that the current relations (2.1-4) and (2.1-5) do not differentiate between lattice temperature and electron temperature. Therefore, if one has to deal with hot electrons in a precise manner, the current relations have to be updated; in particular the mathematical structure of the diffusion current term has to be refined.

The last parameter which remains to be dealt with for a qualitative characterization is the net generation/recombination rate (G-R) in (2.1-2) and (2.1-3). This quantity has to describe a number of physical processes which are responsible for

generation/recombination of electron-hole pairs. These processes and their interactions are also not analyzed to a satisfactory level so that one has to use heuristic expressions for a model which is at least plausible in the underlying physics. Some suggestions for these formulae will be given in the next chapter.

## 2.3 MODELS OF PHYSICAL PARAMETERS

### a) Formulae for modeling doping profiles

A one dimensional doping profile which can be calculated fairly accurately with a process simulation program (e.g. /2/) may be heuristically converted to two dimensions for a structure with an ideal oxide mask as shown in Fig. 2-1 using (2.3-1).

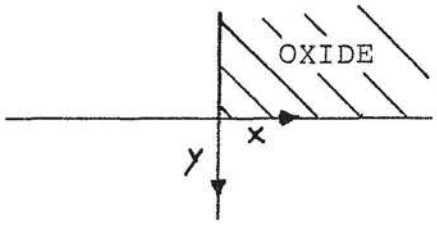


Fig. 2-1 Coordinate nomenclature for an ideal oxide mask

$$C(x,y) = C\left(\sqrt{y^2+\max(x/f,0)^2}\right) \qquad (2.3\text{-}1)$$

This formula is extraordinarily simple to use and needs only one fitting parameter: f which controls the amount of lateral diffusion. For most applications f lies in the range of 0.5 to 0.9. An elliptic rotation at x=0 (c.f. Fig. 2-1) of the one-dimensional profile is performed to obtain the doping concentration below the oxide mask. Out-diffusion effects which occur near the mask edge are not at all taken into account.

Lee /47/, /48/ recently published expressions which are still fairly simple to use, but which are based on more physical reasoning. (2.3-2) can be used for the simulation of a predeposition step. Ld denotes the diffusion length; D: diffusion constant, t: diffusion time, Ns: desired surface concentration.

$$Ld = 2\cdot\sqrt{D\cdot t} \qquad (2.3\text{-}2)$$

$$C_p(x,y) = 0.5\cdot N_s \cdot e^{-(y/Ld)^2} \cdot \mathrm{erfc}(x/Ld)$$

The formulae (2.3-3) allow to simulate diffusion with an initial ion-implantation. Rp denotes the projected range, $\Delta$Rp: projected standard deviation, Dose: implantation dose.

$$a = (2 + (Ld/\Delta Rp)^2)^{-1/2} \qquad (2.3\text{-}3)$$

$$K(y) = e^{-(a\cdot(Rp-y)/\Delta Rp)^2} \cdot \operatorname{erfc}(-a\cdot((Rp/\Delta Rp)+\sqrt{2\cdot y/Ld}))$$

$$C_i(x,y) = (a/(4\cdot\Delta Rp\cdot\sqrt{\pi}))\cdot Dose \cdot (K(y)+K(-y)) \cdot \operatorname{erfc}(x/Ld)$$

In the derivation of (2.3-2) and (2.3-3) it is assumed that the diffusion "constant" is really constant. This limits the application to relatively low peak values of the implanted profile. For high peak values one might fit the diffusion lengths Ld to obtain a desired junction depth.

The diffusion constant D can be estimated, again for fairly low concentrations, with the classical exponential law (2.3-4).

$$D = D_0\cdot e^{T_a/T} \qquad (2.3\text{-}4)$$

| Element | $D_0/(cm^2s^{-1})$ | $T_a/(K)$ |
|---|---|---|
| B | 0.5554 | $-3.975\cdot10^4$ |
| P | 3.85 | $-4.247\cdot10^4$ |
| Sb | 12.9 | $-4.619\cdot10^4$ |
| As | 24. | $-4.735\cdot10^4$ |

The projected range parameters Rp and $\Delta$Rp which are nonlinear functions of the implantation energy can be looked up in standard tables /31/. These tables are principally tedious to implement in computer programs, so that one might prefer some polynomial fit (3.2-5); x denotes here the implantation energy.

$$Rp = \sum_{i=1}^{n} a_i\cdot x^i \quad (\mu m) \qquad (2.3\text{-}5)$$

$$\Delta Rp = \sum_{i=1}^{n} b_i\cdot x^i \quad (\mu m)$$

The coefficients for such polynomials are given in Fig. 2-2 for Rp in silicon, in Fig. 2-3 for $\Delta$Rp in silicon and in Fig. 2-4 for Rp in silicon-dioxide.

| Element | B | P | Sb | As |
|---|---|---|---|---|
| $a_1$ | $3.338 \cdot 10^{-3}$ | $1.259 \cdot 10^{-3}$ | $8.887 \cdot 10^{-4}$ | $9.818 \cdot 10^{-4}$ |
| $a_2$ | $-3.308 \cdot 10^{-6}$ | $-2.743 \cdot 10^{-7}$ | $-1.013 \cdot 10^{-5}$ | $-1.022 \cdot 10^{-5}$ |
| $a_3$ | | $1.290 \cdot 10^{-9}$ | $8.372 \cdot 10^{-8}$ | $9.067 \cdot 10^{-8}$ |
| $a_4$ | | | $-3.056 \cdot 10^{-10}$ | $-3.442 \cdot 10^{-10}$ |
| $a_5$ | | | $4.028 \cdot 10^{-13}$ | $4.608 \cdot 10^{-13}$ |

Fig. 2-2 Coefficients for Rp in silicon

| Element | B | P | Sb | As |
|---|---|---|---|---|
| $b_1$ | $1.781 \cdot 10^{-3}$ | $6.542 \cdot 10^{-4}$ | $2.674 \cdot 10^{-4}$ | $3.652 \cdot 10^{-4}$ |
| $b_2$ | $-2.086 \cdot 10^{-5}$ | $-3.161 \cdot 10^{-6}$ | $-2.885 \cdot 10^{-6}$ | $-3.820 \cdot 10^{-6}$ |
| $b_3$ | $1.403 \cdot 10^{-7}$ | $1.371 \cdot 10^{-8}$ | $2.311 \cdot 10^{-8}$ | $3.235 \cdot 10^{-8}$ |
| $b_4$ | $-4.545 \cdot 10^{-10}$ | $-2.252 \cdot 10^{-11}$ | $-8.310 \cdot 11^{-10}$ | $-1.202 \cdot 10^{-10}$ |
| $b_5$ | $5.525 \cdot 10^{-13}$ | | $1.084 \cdot 10^{-13}$ | $1.601 \cdot 10^{-13}$ |

Fig. 2-3 Coefficients for $\Delta$Rp in silicon:

| Element | B | P | Sb | As |
|---|---|---|---|---|
| $a_1$ | $3.258 \cdot 10^{-3}$ | $9.842 \cdot 10^{-4}$ | $7.200 \cdot 10^{-4}$ | $7.806 \cdot 10^{-4}$ |
| $a_2$ | $-2.113 \cdot 10^{-6}$ | $-2.240 \cdot 10^{-7}$ | $-8.054 \cdot 10^{-6}$ | $-7.899 \cdot 10^{-6}$ |
| $a_3$ | | | $6.641 \cdot 10^{-8}$ | $7.029 \cdot 10^{-8}$ |
| $a_4$ | | | $-2.422 \cdot 10^{-10}$ | $-2.653 \cdot 10^{-10}$ |
| $a_5$ | | | $3.191 \cdot 10^{-13}$ | $3.573 \cdot 10^{-13}$ |

Fig. 2-4 Coefficients for Rp in silicon-dioxide

The maximum error of the projected range parameters calculated with these coefficients and (2.2-5) is in the energy range of 5keV to 300keV only a few percent compared to /31/. More data are given in /71/.

If an implantation is performed through an oxide, the projected range in the semiconductor has to be reduced /62/ e.g. with (2.3-6).

$$Rp = Rp_{se} \cdot (1 - T_{iox}/Rp_{ox}) \qquad (2.3\text{-}6)$$

$T_{iox}$ denotes the thickness of the oxide, $Rp_{se}/Rp_{ox}$: projected range in semiconductor/oxide.

b) Formulae for mobility modeling.

The mobility of carriers is, as already mentioned, an eminently complex quantity. Additionally it is an important parameter, because all errors in the mobility produce through the multiplicative dependence, a proportional error of the current which certainly is one of the primary results any model should yield reliably. The formulae which will be given below describe phenomenologically the mobility in silicon; the subscripts n and p will denote electrons holes, respectively.

To model mobility at least plausibly several scattering mechanisms have to be taken into account, the basis of which is lattice scattering. This effect can be described with a simple power law /39/ in dependence of temperature (2.3-7).

$$\mu_L(T) = A \cdot T^{-g} \quad (cm^2/Vs) \tag{2.3-7}$$

$A_n = 7.12 \cdot 10^8$ $\qquad$ $A_p = 1.35 \cdot 10^8$
$g_n = 2.3$ $\qquad$ $g_p = 2.2$

The pure lattice mobility is reduced through the scattering processes at ionized impurities. (2.3-8) is a well established formula which models temperature dependent ionized impurity scattering /9/ and electron-hole scattering /50/. The latter is extremely important in low doped regions where high injection takes place.

$$\mu_{LI}(N,T) = \mu_L(T) \cdot a + \mu_{min} \cdot (1 - a) \quad (cm^2/Vs) \tag{2.3-8}$$

$$a = \frac{1}{1 + (T/300)^b \cdot (N/N_0)^c}$$

$$N = 0.67 \cdot (N_D^+ + N_A^-) + 0.33 \cdot (n + p)$$

$\mu_{minn} = 55.24$ $\qquad$ $\mu_{minp} = 49.7$
$b_n = -3.8$ $\qquad$ $b_p = -3.7$
$c_n = 0.73$ $\qquad$ $c_p = 0.7$
$N_{0n} = 1.072 \cdot 10^{17}$ $\qquad$ $N_{0p} = 1.606 \cdot 10^{17}$

Similar expressions have been presented in /20/, /64/.

For simulating properly the mobility in MOS transistors one has to deal with surface roughness and field dependent surface scattering. /13/, /63/ presented interesting measured results on

inversion layer mobility; /75/ gave some excellent ideas on how to treat theoretically this and other scattering mechanisms; /85/ suggested a heuristc formula for field dependent surface scattering which is applicable for two-dimensional simulations, but whose adequacy is questioned in /75/. However, we have developed (2.3-9) which models phenomenologically with best fit to measurement surface roughness as well as field dependent surface scattering /72/.

$$\mu_{LIS}(y,E_p,E_t,N,T) = \mu_{LI}(N,T)\cdot\frac{y+y_r}{y+b\cdot y_r} \quad (cm^2/Vs) \qquad (2.3\text{-}9)$$

$$y_r = y_0/(1+E_p/E_{p0})$$

$$b = 2+E_t/E_{t0}$$

$$E_p = \max(0,(E_x\cdot J_x+E_y\cdot J_y)/(J_x^{\,2}+J_y^{\,2})^{1/2})$$

$$E_t = \max(0,(E_x\cdot J_y-E_y\cdot J_x)\cdot J_x/(J_x^{\,2}+J_y^{\,2}))$$

$$y_{0n} = 5\cdot10^{-7} \qquad y_{0p} = 4\cdot10^{-7}$$

$$E_{p0n} = 10^4 \qquad E_{p0p} = 8\cdot10^3$$

$$E_{t0n} = 1.8\cdot10^5 \qquad E_{t0p} = 3.8\cdot10^5$$

In regions with a high electric field component parallel to current flow, the drift velocity saturation phenomenon has to be taken into account. (2.3-10) combines, also phenomenologically, this physical effect and the lattice-impurity-surface mobility using a Mathiessen-type rule with a weakly temperature dependent saturation velocity /8/, /39/.

$$\mu_{tot}(y,E_p,E_t,N,T) = (\mu_{LIS}(...)^{\beta}+(v_s/E_p)^{\beta})^{1/\beta} \qquad (2.3\text{-}10)$$

$$v_{sn} = 1.53\cdot10^9\cdot T^{-0.87} \qquad v_{sp} = 1.62\cdot10^8\cdot T^{-0.52}$$

$$\beta_n = -2 \qquad \beta_p = -1$$

c) Formulae for modeling generation/recombination

To simulate satisfactorily transfer phenomena of majority carrier current and minority carrier current in just a simple diode, it is an absolute necessity to model carrier recombination and generation as carefully as possible. (2.3-11) represents the well known Shockley-Read-Hall term for modeling thermal generation/recombination. The carrier lifetimes can be simulated as being doping dependent /15/.

$$(G-R)_{th} = \frac{n_i^2 - p\cdot n}{\tau_n(p+n_1)+\tau_p(n+n_1)} \qquad (1/cm^3s) \qquad (2.3\text{-}11)$$

$$\tau_n = 3.95\cdot10^{-5}/(1+N/7.1\cdot10^{15}) \qquad \tau_p = 3.52\cdot10^{-5}/(1+N/7.1\cdot10^{15})$$

Surface generation/recombination can be treated in a fairly similar manner with (2.3-12).

$$(G-R)_s = \frac{n_i^2 - p\cdot n}{(p+n_1)/s_n+(n+n_1)/s_p}\cdot\delta(y) \qquad (1/cm^3s) \qquad (2.3\text{-}12)$$

$\delta(y)$ : Dirac-Delta function, y=0 denotes an interface

$$s_n = 100 \qquad s_p = 100$$

Impact ionization can be modeled by an exponentially field dependent generation term /11/, /12/. The constants in (2.3-13) are essentially taken from /78/.

$$G_a = \frac{\vec{J}_n}{q} A_n \exp\left(-\frac{B_n \vec{J}_n}{\vec{E}\cdot\vec{J}_n}\right) + \frac{\vec{J}_p}{q} A_p \exp\left(-\frac{B_p \vec{J}_p}{\vec{E}\cdot\vec{J}_p}\right) \qquad (1/cm^3s) \qquad (2.3\text{-}13)$$

$$A_n = 7\cdot10^5 \qquad A_p = 1.588\cdot10^6$$
$$B_n = 1.23\cdot10^6 \qquad B_p = 2.036\cdot10^6$$

It should be noted that this form of simulating avalanche is relatively crude compared to more exact considerations, but the underlying physical principles are so complex that a trade-off in accuracy and complexity leads to that type of formula.

To analyze high injection conditions, Auger recombination has to be included as an antagonism to avalanche generation. Already the use of a simple formula like (2.3-14) gives in general satisfactory results /5/, /15/, /24/.

$$(G-R)_{Aug} = (n_i^2 - p\cdot n)(C_n\cdot n + C_p\cdot p) \qquad (1/cm^3s) \qquad (2.3\text{-}14)$$

$$C_n = 2.8\cdot10^{-31} \qquad C_p = 9.9\cdot10^{-32}$$

Finally, all generation/recombination phenomena have to be combined to one total quantity. The usual way to do so is to simply sum up all terms (2.3-15). However, that means that no interaction of the different phenomena does exist.

$$(G-R)_{tot} = (G-R)_{th} + (G-R)_s + (G-R)_{Aug} + G_a \qquad (2.3\text{-}15)$$

## 3. THE HIERACHY OF MODELS

Device models are principally used for two different forms of applications, namely device analysis and circuit simulation. For the former a highly accurate model which is imperatively based on physical considerations is needed. For the latter - since for this application the interaction of different devices is of primary importance - models which just simulate the device behaviour within some given accuracy are requested. It is evident that for the same device a set of different models is required in order to analyze or simulate efficiently. Obviously, one must have simpler models to simulate the global interaction of 100.000 devices than to analyze detailed effects in a circuit containing some 10 devices /58/. The pervasive problem in device modeling is to achieve a required accuracy with minimal model complexity. The model used should certainly not be more accurate than needed to be for the purposes of a desired simulation. Therefore, it is of paramount importance to understand the trade-off between efficiency and accuracy of a model.

Basically a device model can be classified as being:

- analytical
- semi numerical
- numerical
- artificial

Analytical models can be derived only if one makes rigorous assumptions and regional approximations prior to integrating the basic equations (2.1-1)-(2.1-5). An analytical solution of the partial differential equations without additional assumptions is impossible. One has to admit, however, that many analytic models have been applied and are still applied and produce absolutely satisfactory results. In case of circuit simulation analytic models are the best established type of models. Owing to limited space, it is unfortunately impossible to present the variety of ideas of many scientists, which led to analytic models with high reputation. The interested reader should consult e.g. /30/, /61/ for bipolar transistor modeling and e.g. /26/, /43/, /52/, /83/ for MOSFET modeling.

Semi-numerical models can be qualitatively separated into two categories, one of which utilizes relatively complicated equivalent-circuits /46/. Models of the second class try to reduce the number of assumptions which are necessary for a fully analytic solution by solving Poisson's equation with classical numerical methods and the other equations by an analytical calculus /16/, /25/, /32/, /33/. This type of models is to some extent capable to analyze device performance and not only to simulate device behaviour. Analytical models usually lack, owing to too many assumptions, the capability of prediction.

Gummel /34/ was the very first who suggested to solve the semiconductor equations fully numerically for the analysis of a bipolar transistor. He and many early successors e.g. /17/, /18/, /64/ contributed basic methods and ideas for numerical device analysis and simulation. The urgent need of better device models for integrated circuits produced an improvement of these early activities; the first papers on modeling devices in two space dimensions were published e.g. /42/. Many theses on device modeling have been finished since that time e.g. /38/, /40/, /50/, /60/, /72/, /74/, and many valuable papers have been published /6/, /14/, /35/, /36/, /37/, /53/, /54/. Today the first activities in modeling devices in even three space dimensions can be observed /7/, /10/, /86/. A few examples of the power of one particular two dimensional model will be given in the next chapters. However, one should bear in mind that these high order numerical models are relatively expensive and slow and, therefore, should be applied thoughtfully. Much work has still to be done to make these models more broadly applicable; not just when experimental device investigations are not feasable /68/ or too time consuming.

In recent days some activities on totally artificial models for application in circuit simulation programs can be seen, as the utilization of numerical models is only possible for very small circuits /23/. These models are designed to fit best given characteristics which e.g. are obtained by measurement with minimal mathematical complexity. Therefore no connection to physics does exist. Very recent ideas are based on nested one dimensional table look up /58/ which certainly minimizes the time needed for model evaluation, but consumes more computer-memory.

## 4. A DIDACTIC EXAMPLE

It is rather difficult to provide an interesting example for the experienced reader, which is also impressive and easy to understand for readers with general interest in modeling but without specific knowledge of device physics. We have chosen the effects of ion implantation on short channel MOS transistors for the purpose of demonstrating the use of two dimensional simulation. Three devices are calculated whose properties become apparent from the original simulation input decks presented in Fig. 4-1. The following discussion of Fig. 4-1 shall also demonstrate the ease of using MINIMOS /69/, /70/, our simulation program.

The first line is a title line, which is used only to identify the output of the program. The input syntax is totally based on a master key, key and value structure. The next input line which is the "DEVICE" statement, characterizes the device. Specified is an n-channel device (CHANNEL=N) with an n-doped polysilicon gate (GATE=NPOLY), an oxide thickness of 35 nanometers (TOX=350.E-8), a channel width of 10 micrometers (W=10.E-4) and a channel length of one micrometer (L=1.E-4). The "BIAS" statement specifies the operating point. A drain voltage of 3 volts (UD=3.) and a gate voltage of zero volts (UG=0.) has been chosen. The substrate voltage is assumed to be zero by MINIMOS, if not specified otherwise. The "PROFILE" statement is used to specify the substrate doping and the source/drain diffusion. In the examples presented here we used the simplest way of defining a doping profile, that is the direct calculation by MINIMOS. Another possibility would be to make use of a technology simulation program like SUPREM, the **S**tanford **U**niversity **PR**ocess **E**ngineering **M**odels program /2/, for the more accurate calculation of vertical profile shapes which are fitted in the lateral direction. For our simulation a substrate doping of $10^{15}cm^{-3}$ (NB=1.E15) and a source/drain implantation with phosphorus (ELEM=PH), an implantation dose of $10^{15}cm^{-2}$ (DOSE=1.E15) and an implantation energy of 40keV (AKEV=40) is specified. The implantation is performed through an isolation oxide of 35 nanometers (TOX=350.E-8) and followed by an annealing step at 1000 centigrades (TEMP=1000) for 1200 seconds (TIME=1200).

```
ONE-MICRON ANALYSIS (DEVICE 1)
DEVICE    CHANNEL=N  GATE=NPOLY  TOX=350.E-8 W=10.E-4 L=1.E-4
BIAS      UD=3.  UG=0.
PROFILE   NB=1.E15  ELEM=PH  DOSE=1.E15  AKEV=40  TOX=350.E-8
+         TEMP=1000  TIME=1200
END


ONE-MICRON ANALYSIS (DEVICE 2)
DEVICE    CHANNEL=N  GATE=NPOLY  TOX=350.E-8 W=10.E-4 L=1.E-4
BIAS      UD=3.  UG=0.
PROFILE   NB=1.E15  ELEM=PH  DOSE=1.E15  AKEV=40  TOX=350.E-8
+         TEMP=1000  TIME=1200
IMPLANT   ELEM=B  DOSE=3.5E11  AKEV=25  TEMP=925  TIME=1800
END


ONE-MICRON ANALYSIS (DEVICE 3)
DEVICE    CHANNEL=N  GATE=NPOLY  TOX=350.E-8 W=10.E-4 L=1.E-4
BIAS      UD=3.  UG=0.
PROFILE   NB=1.E15  ELEM=PH  DOSE=1.E15  AKEV=40  TOX=350.E-8
+         TEMP=1000  TIME=1200
IMPLANT   ELEM=B  DOSE=3.5E11  AKEV=25  TEMP=925  TIME=1200
IMPLANT   ELEM=B  DOSE=1.5E11  AKEV=100
END
```

Fig. 4-1: Some typical input decks for MINIMOS

The second input deck further includes an "IMPLANT" statement which defines a channel implantation with boron (ELEM=B), a dose of $3.5 \cdot 10^{11} cm^{-2}$ (DOSE=3.5E11), an energy of 25keV (AKEV=25), annealed at 925 centigrades (TEMP=925) for 1800 seconds (TIME=1800). The third input deck has an additional "IMPLANT" statement specifying a second, deeper channel implantation with boron (ELEM=B), a dose of $1.5 \cdot 10^{11} cm^{-2}$ (DOSE=1.5E11) and an energy of 100keV (AKEV=100). It is assumed that both channel implantation steps are annealed at the same time. It is fairly well known that the first of these three devices is, owing to the short channel effect, "normally-on" and that the shallow implantation of device 2 utilizes threshold shift to obtain a "normally-off" device. Furthermore, the deep implantation of device 3 is necessary to avoid punch through. These effects will now be demonstrated by birds-eye-view- and contour-plots of physically relevant quantities in the interiour of the three model devices.

The calculated doping density distributions for our devices are shown in Figs. 4-2, 4-3, 4-4.

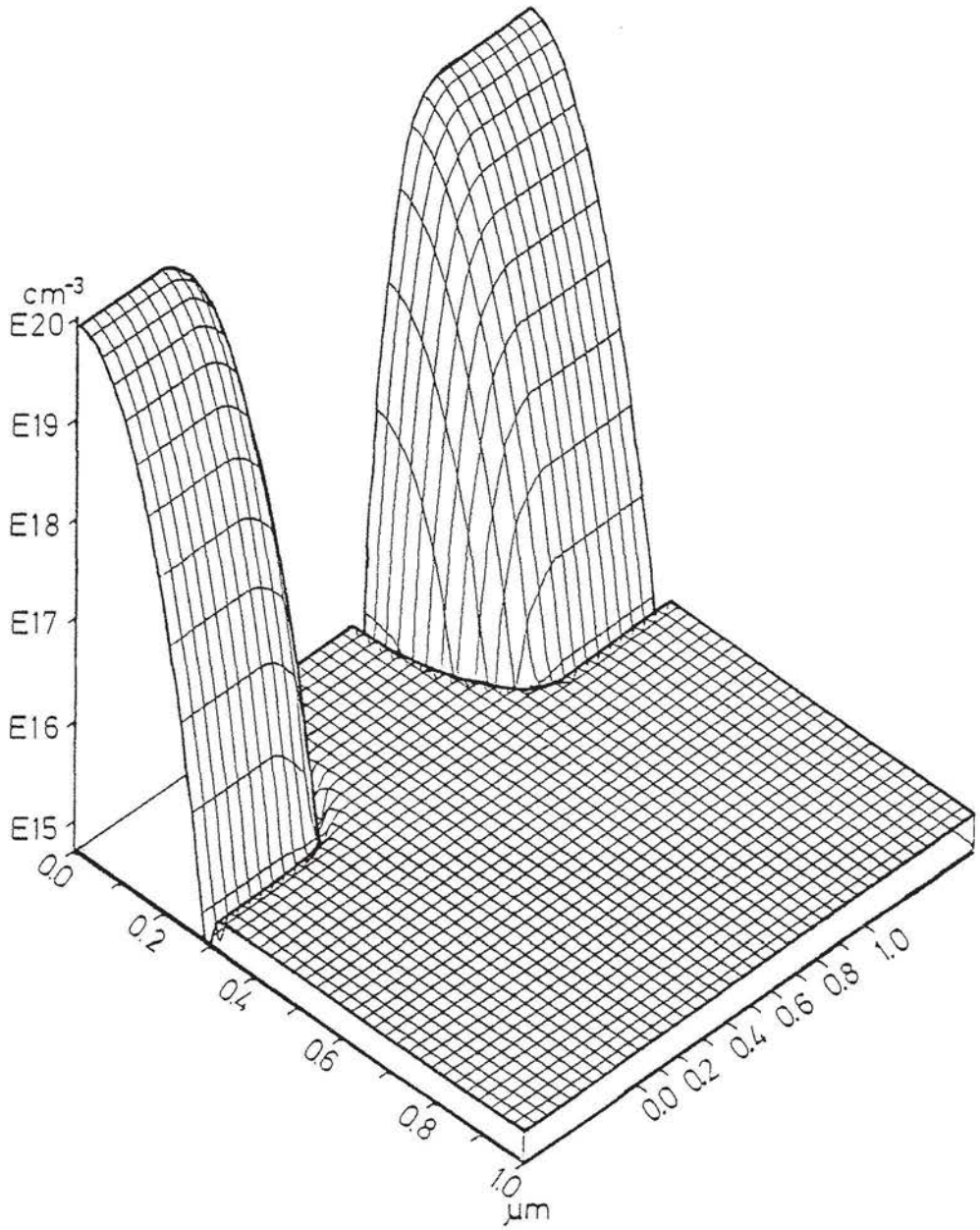


Fig. 4-2: Doping profile for device 1

From these figures one can read off the depth of the pn-junctions under source and drain being approximately 300 nanometers. The surface concentration of the source and drain regions is about $10^{20}cm^{-3}$. The effective channel length is reduced by the lateral subdiffusion to about 0.6 micrometers. The shallow channel implantation for threshold tailoring can be seen in Figs. 4-3, 4-4. Additionaly, Fig. 4-4 shows the deep implantation for punch through suppression. The threshold voltage is only marginally affected by the deep implantation.

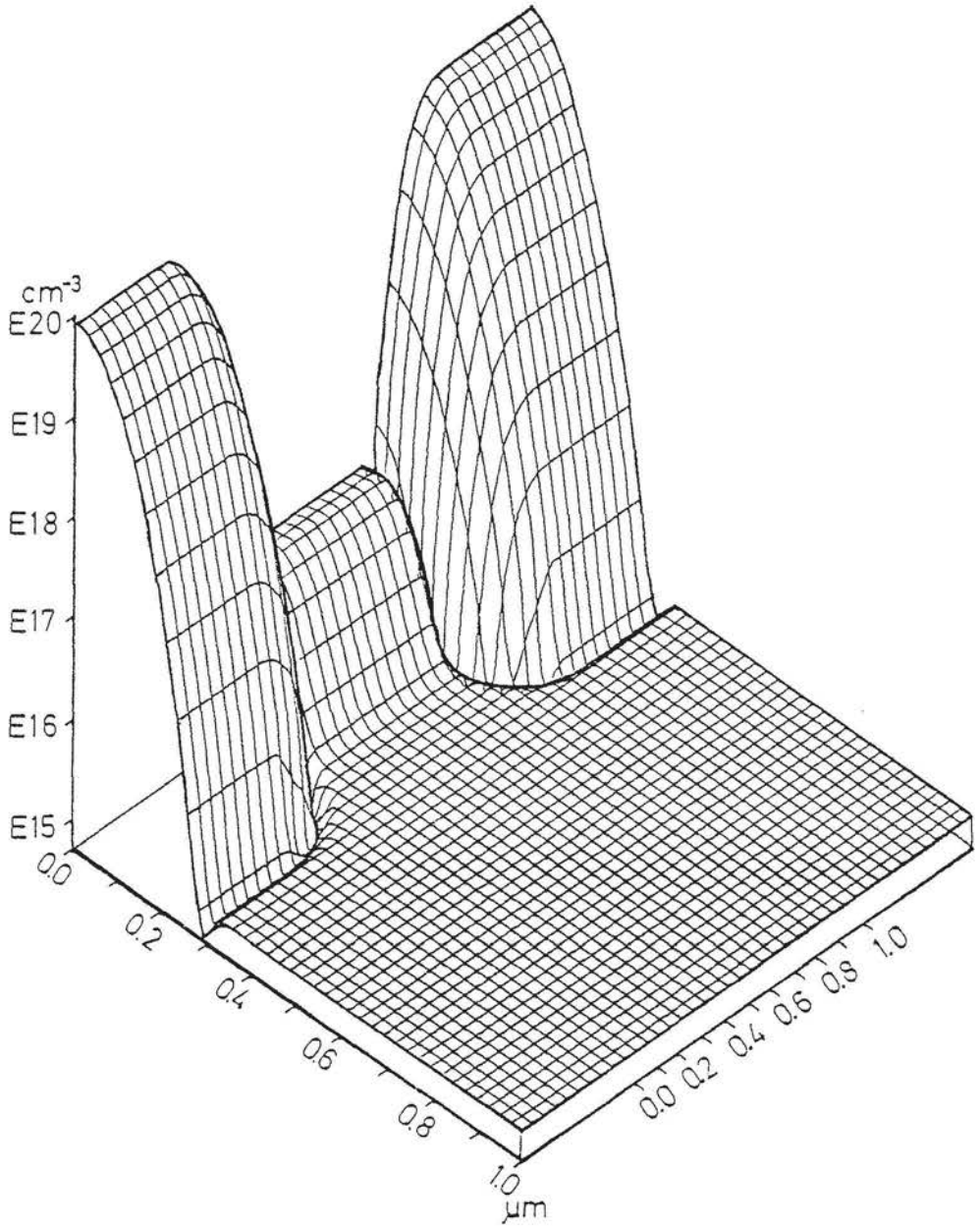


Fig. 4-3: Doping profile for device 2

Fig. 4-5 shows the distribution of the electric potential for the first device. The drain contact is on the right. In the depletion region of the reverse biased drain-bulk diode the potential decreases monotonously and it is more or less constant in the highly doped source and drain regions. The barrier at the source channel diode is relatively small /77/. Fig. 4-6 shows the potential distribution in the second device. The birds-eye-view plot looks very similar to the plot in Fig. 4-5.

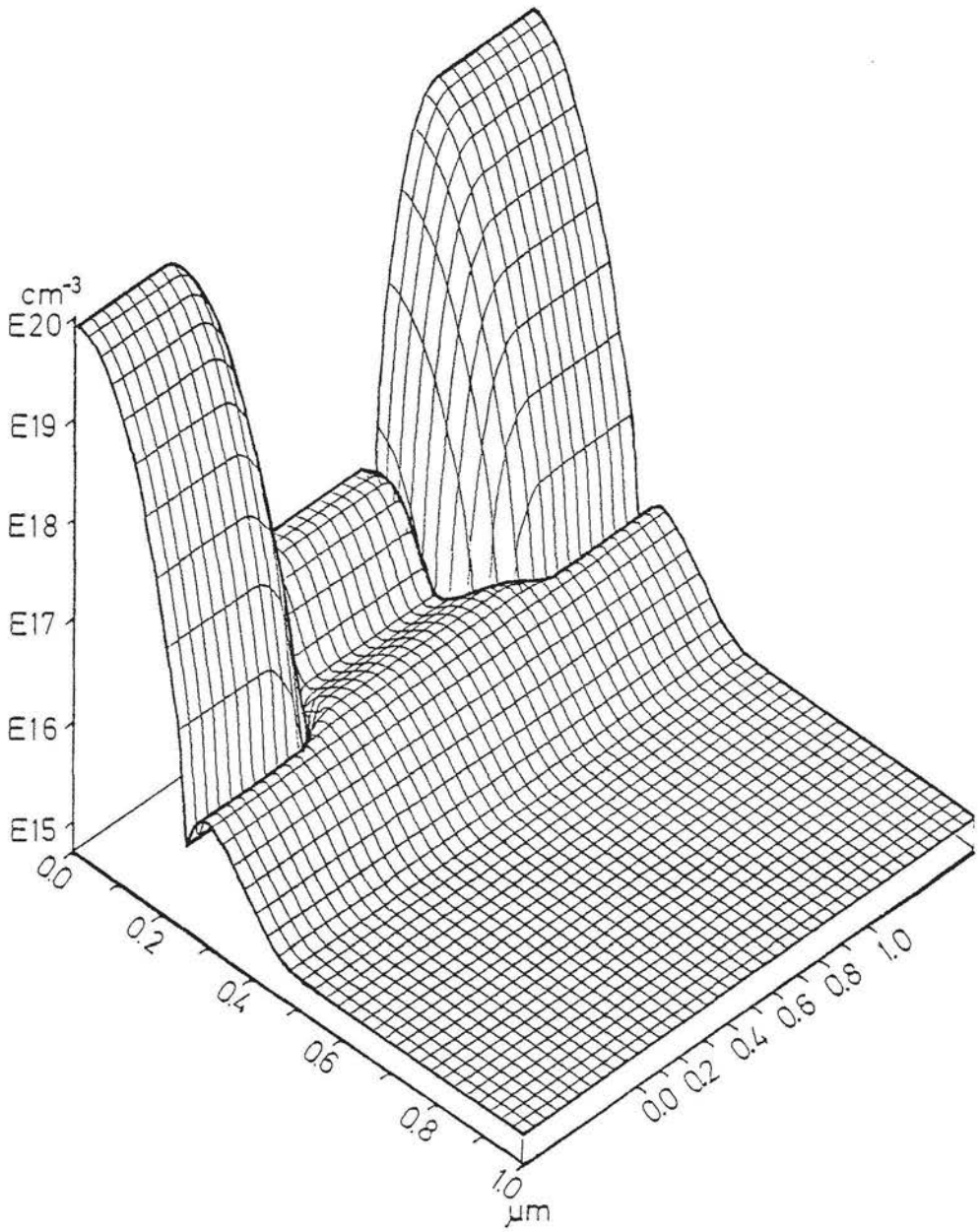


Fig. 4-4: Doping profile for device 3

The contour-plot, however, shows quite a pronounced potential basin directly below the interface. Of even greater importance than this basin itself is the saddlepoint below the basin. At this saddlepoint the electric field vanishes and current only can flow by carrier diffusion. This sort of saddlepoint is, following the proposition of many authors (e.g. /4/, /45/), a typical indication of the punch-through effect. The electric field which is induced by the gate is unable to separate the depletion regions of source and drain.

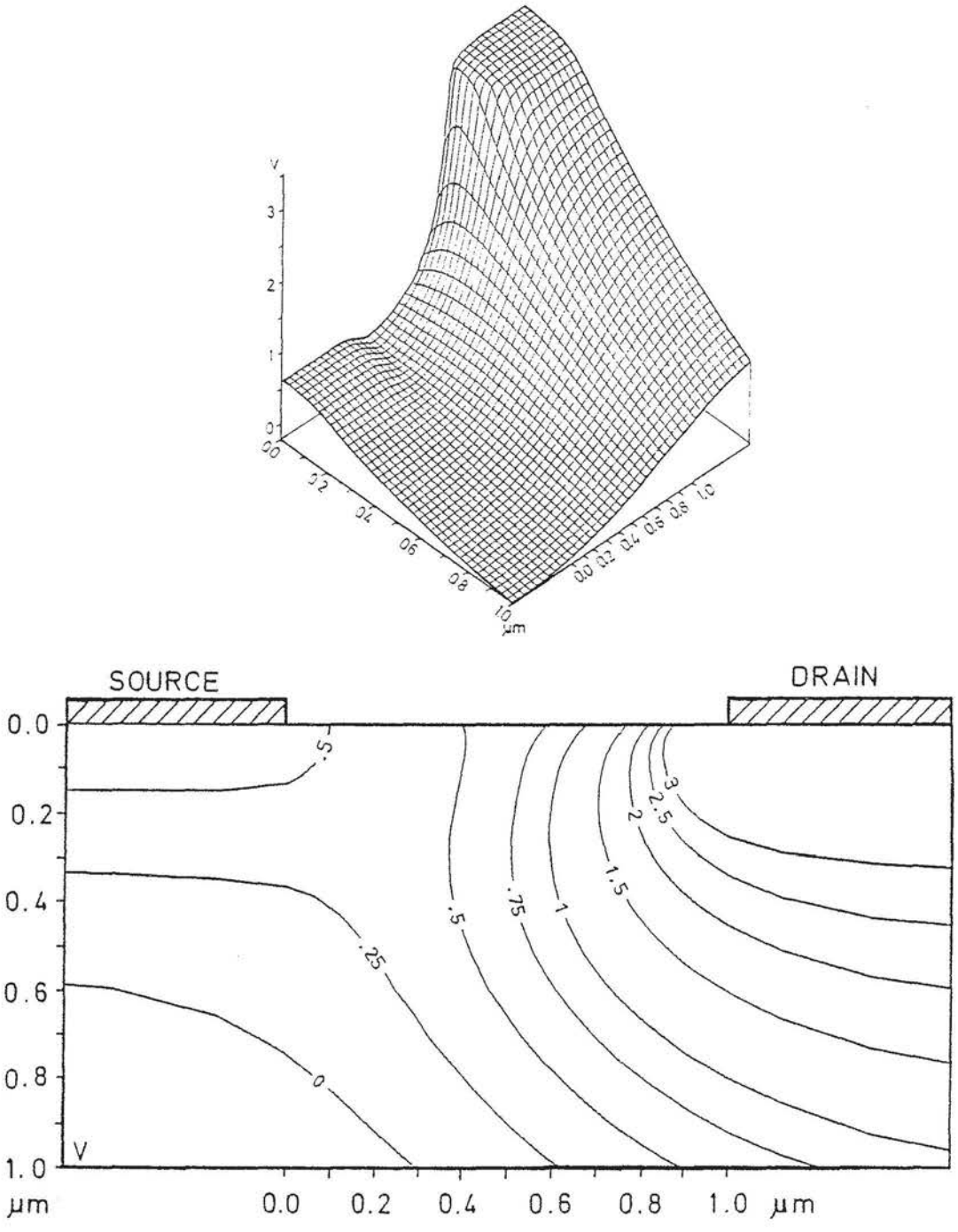


Fig. 4-5: Electric potential for device 1

These depletion regions are in contact below the region of control by the gate. As it will become visible later on, the saddlepoint is a reliable indication of the punch-through effect, but it does not need to exist.

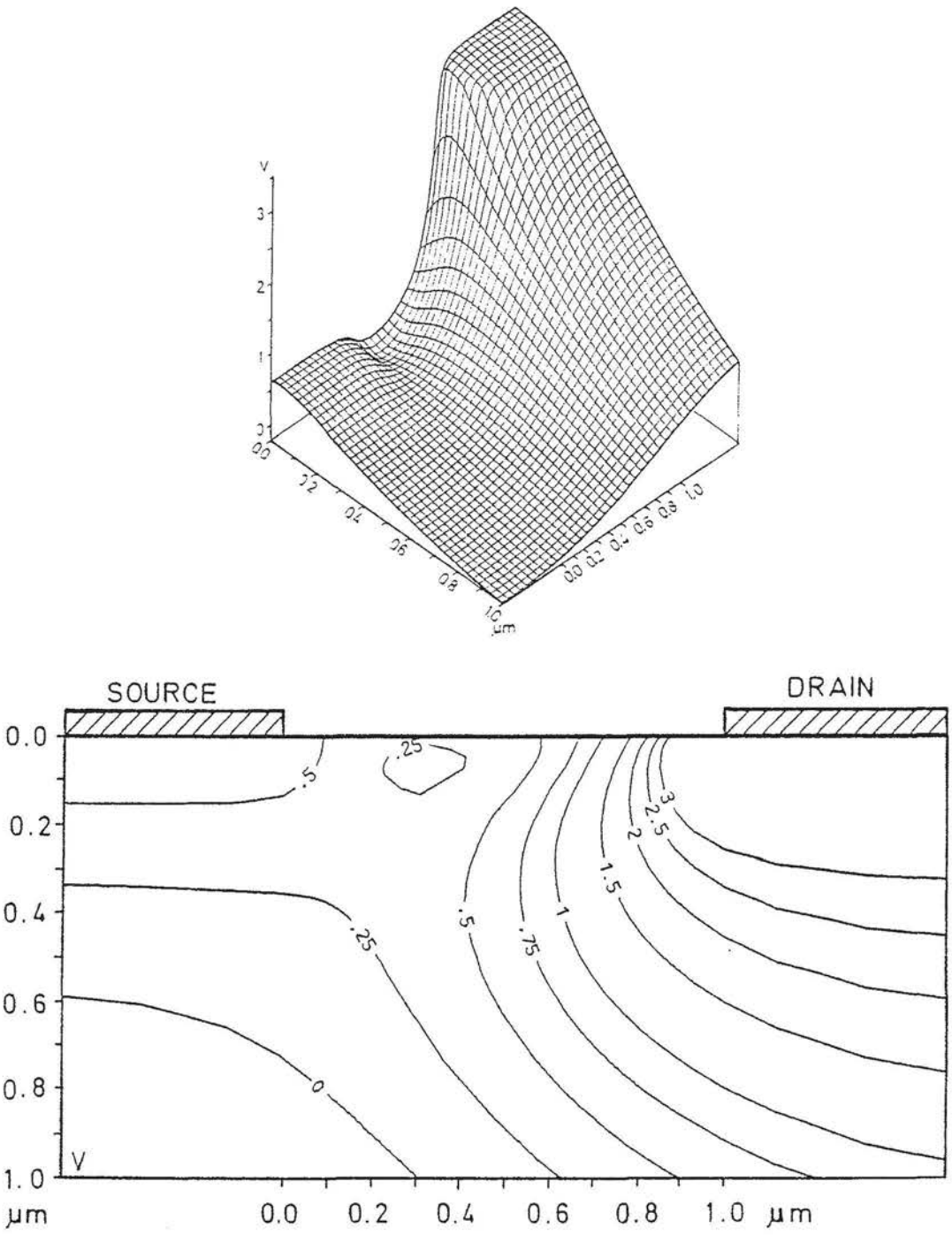


Fig. 4-6: Electric potential for device 2

Fig. 4-7 shows the potential distribution in the third device. The birds-eye-view plot differs just marginally from the plot in Fig. 4-6. But from the contour plot one can see a well pronounced barrier between source and channel which guarantees the "normally-off" behaviour.

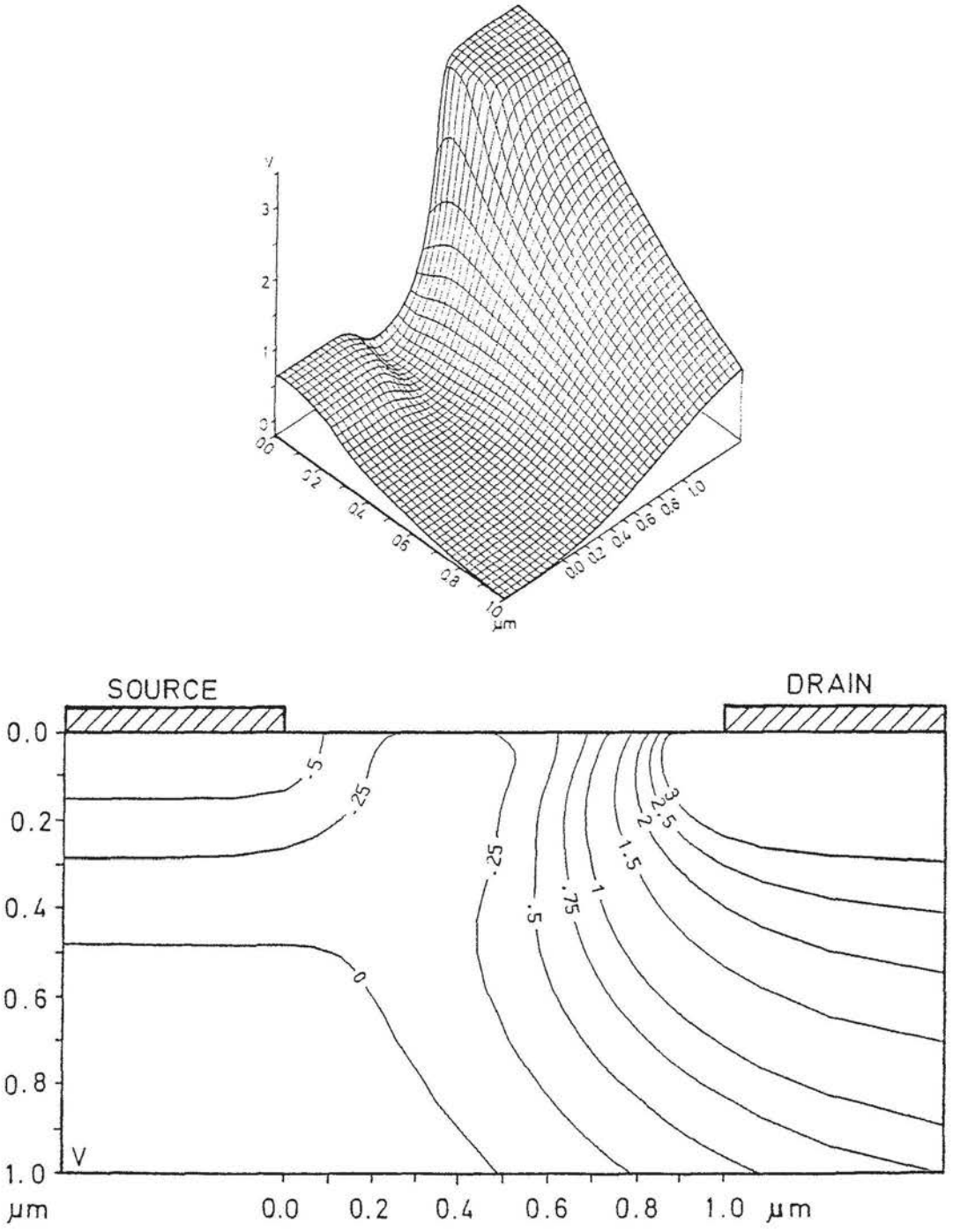


Fig. 4-7: Electric potential for device 3

Fig. 4-8 shows the lateral current density distribution in the first device. For better visibility, the plot on the right shows the mirror image to give better insight into the channel region. In the channel near the source side the current is forced to flow at the surface by the transversal component of the field.

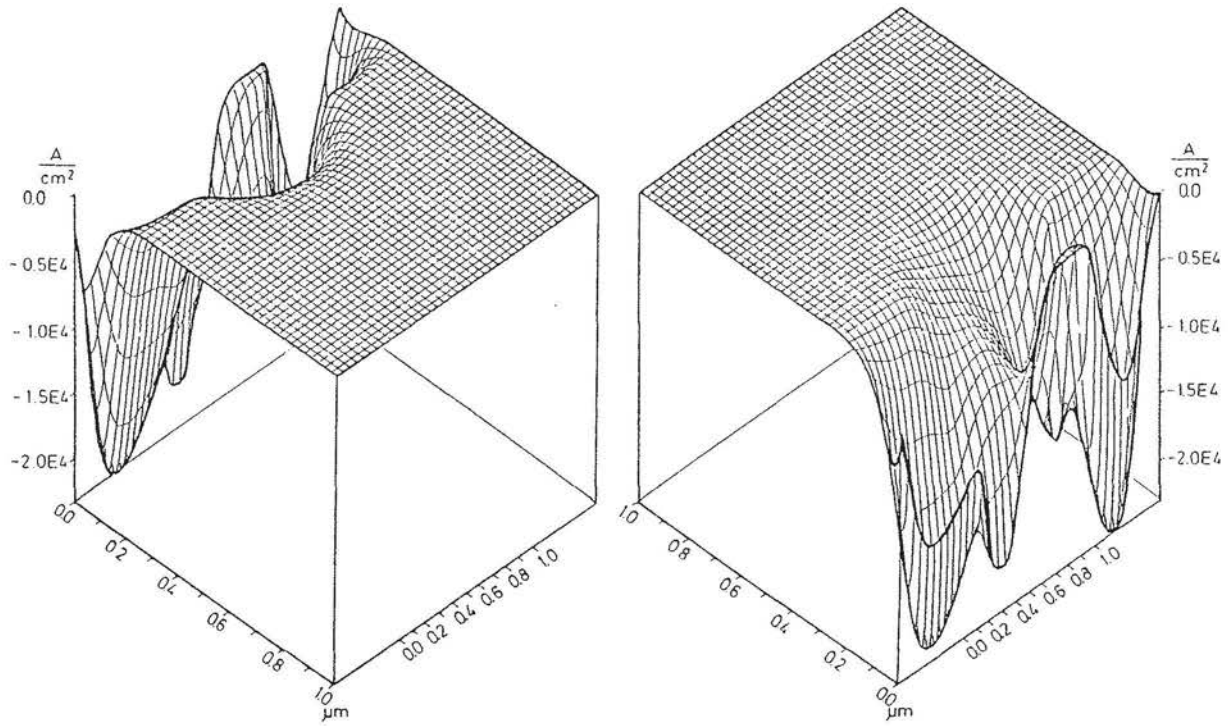


Fig. 4-8: Lateral current density for device 1

But already in the middle of the channel, a typical short channel effect, one can watch current spreading caused by the drain influence.

It also should be noted that the current channel is fairly wide. The reason for this phenomenon is to be found in a superposition of an inversion channel and a punch through channel. The maximum of the lateral current density surprisingly lies below the contacts. This fact becomes clear when we consider current continuity. Current can only pass through the contact in transversal direction. Current flow in the semiconductor, however, takes place globally in the lateral direction from source to drain. As current flow is continuous, the lateral current component has to be large below the contacts, because the flux in the channel, which is relatively wide, as mentioned, is large too. The lateral current distribution for the second device is shown in Fig. 4-9. As one can see, this device is operating in the punch through mode. The current flow takes place in a wide channel in the bulk. Surface current does effectively not exist. Furthermore, the maximum of the current density has decreased more than an order of magnitude compared to the first device.

Fig. 4-10 shows the lateral current density distribution for

the third device. The second channel implantation results in a total suppression of punch through in this operating point. The entire current flows at the semiconductor surface, but the peak value of the current density is about a factor of 200 lower than in the second device.

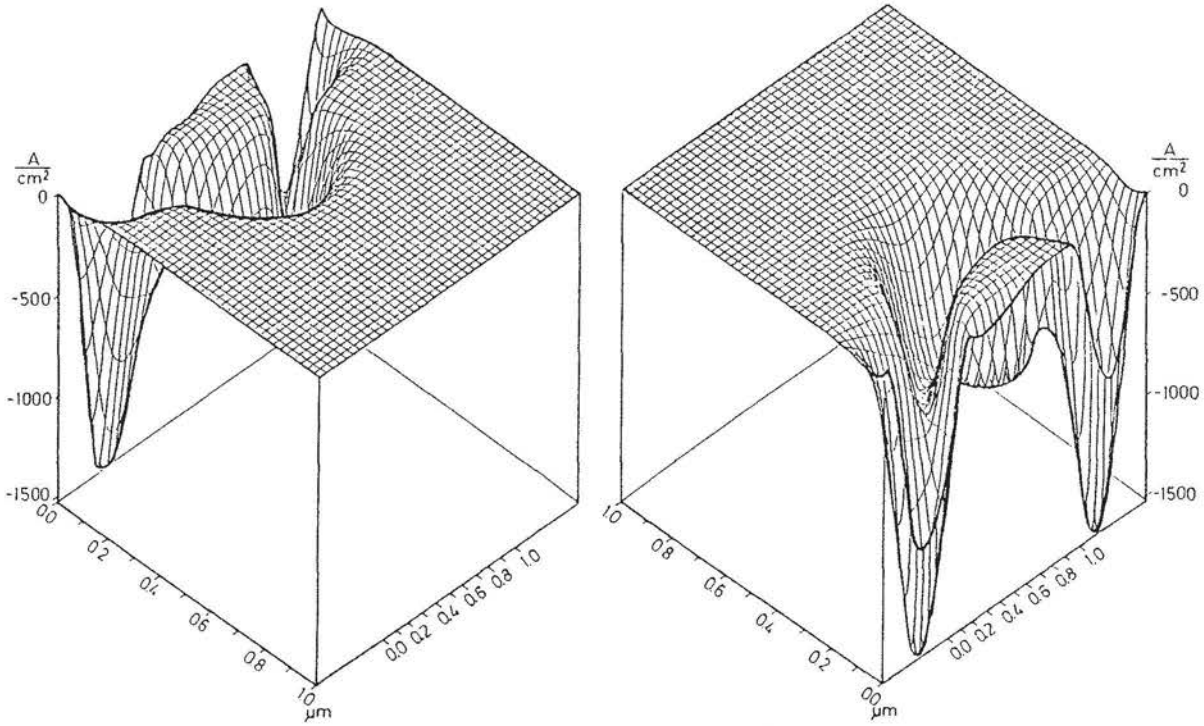


Fig. 4-9: Lateral current density for device 2

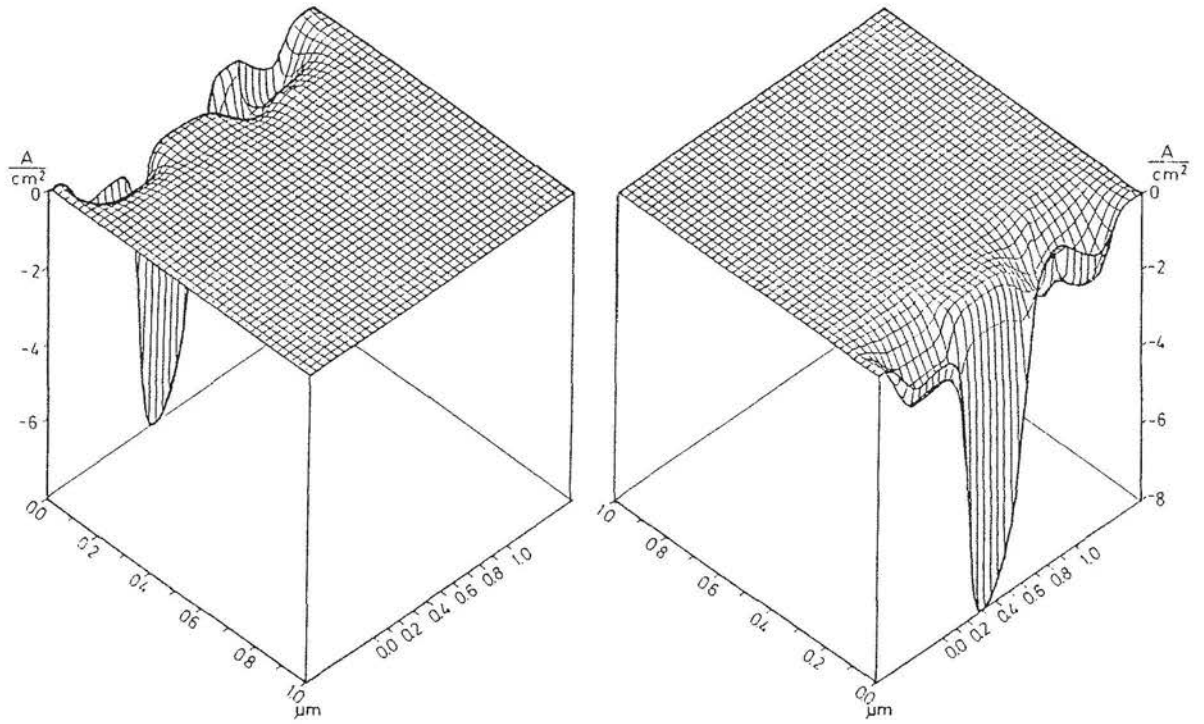


Fig. 4-10: Lateral current density for device 3

Current density distributions of this shape are typical for regularly operating transistors in subthreshold and can be used as criterion for valuation.

Fig. 4-11 shows the subthreshold characteristics for two different drain voltages. The fully drawn lines denote 100mV, the dashed lines 3V drain bias. The slope is the same for all three devices at a drain voltage of 100mV. It is dramatically decreased at 3V drain bias for devices 1 and 2 by the punch through current. The shift of the characteristics for different drain voltages, which is caused by the short channel effect, is a minimum for the third transistor thus verifying the success of the channel implantation steps.

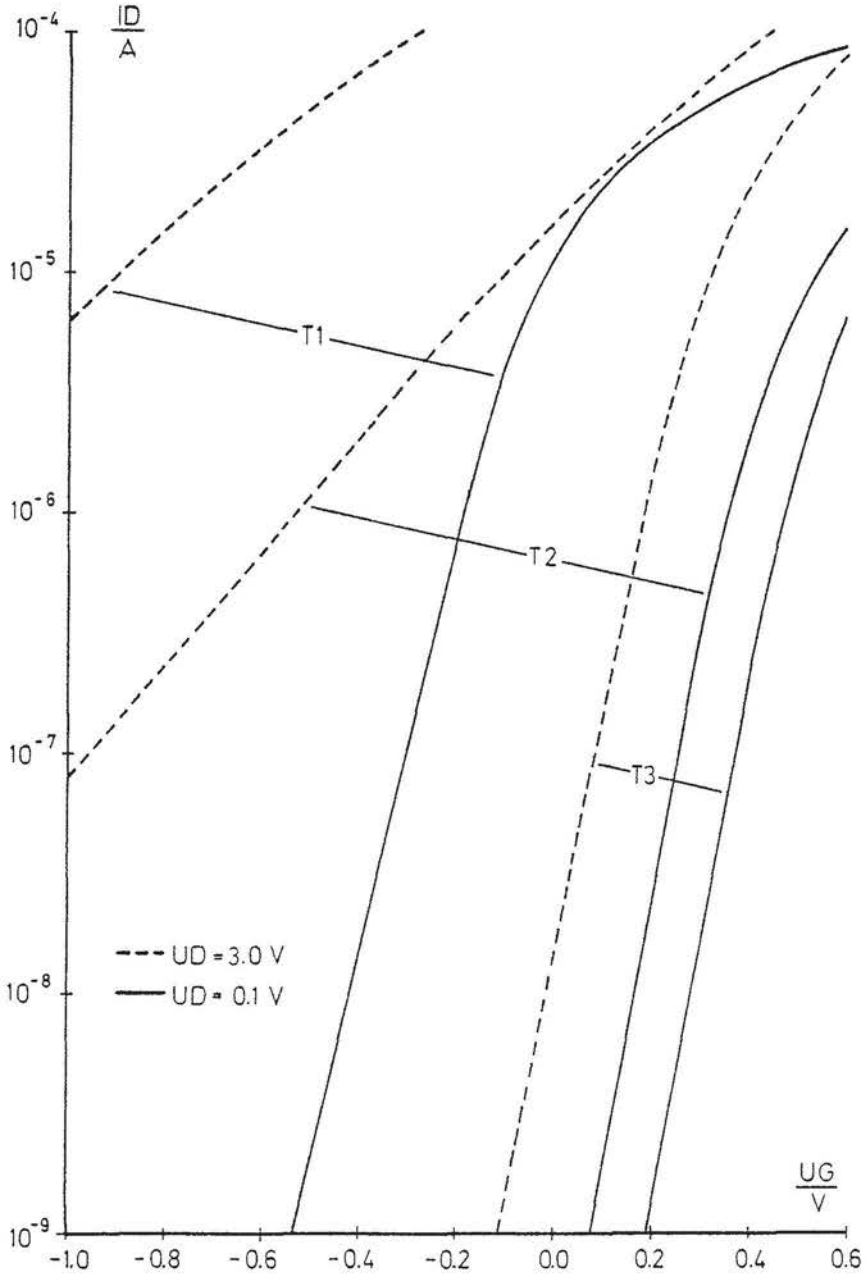


Fig. 4-11: Subthreshold characteristics

## 5. A MORE SOPHISTICATED EXAMPLE (AVALANCHE ANALYSIS)

In order to increase the number of functional units per chip it is necessary to decrease the size of the devices (e.g. channel length and channel width for MOS transistors). As the performance of a device depends strongly on its geometry, any reduction requires to obey certain design rules (c.f. /19/ for MOS devices). However, in recent years devices have been miniaturized without reduction of supply voltage, mainly to stay compatible with existing circuits and to keep hold of acceptable a signal to noise ratio. In that manner problems with punch through and avalanche breakdown arise. Punch through can be controlled relatively well by technological steps as already outlined in the last chapter for an MOS transistor. Thus the demand for a transparent description of the physical processes which lead to avalanche breakdown exists.

Avalanche problems have so far been treated /44/, /76/ in the following manner: First Poisson's equation is solved to obtain a solution for the electrical potential distribution and then the ionization integral is evaluated by integrating the strongly field dependent ionization coefficients over the high field region. As result multiplication factors are obtained which describe the increase of current due to avalanche. Since the carrier densities need not be calculated, this method seems to be very efficient in calculating breakdown voltages. However, any feedback of the increase in carrier densities on the electrical field is, therefore, neglected. A more serious treatment requires the solution of both carrier continuity equations with proper modeling of the generation term /65/, /67/.

In this chapter calculations for a 1 micron gate length n-channel MOS transistor are presented. The lateral subdiffusion and the junction depth of the source and drain regions are 0.2 and 0.3 $\mu$m, respectively. A deep channel implantation with fairly high dose was supposed to have been performed to suppress punch-through.

Fig. 5-1 shows calculated drain and bulk currents versus drain voltage for that transistor. For $U_{GS}$=1V breakdown is reached at $U_{DS}$=5.6V whereas 8.4 Volts are necessary to lead the device into breakdown if no gate voltage is applied. On first glance that

seems to be paradox, if one considers that $U_{GS}$=0V certainly causes larger peak values of the electric field. The explanation of this phenomenon lies in the low current level.

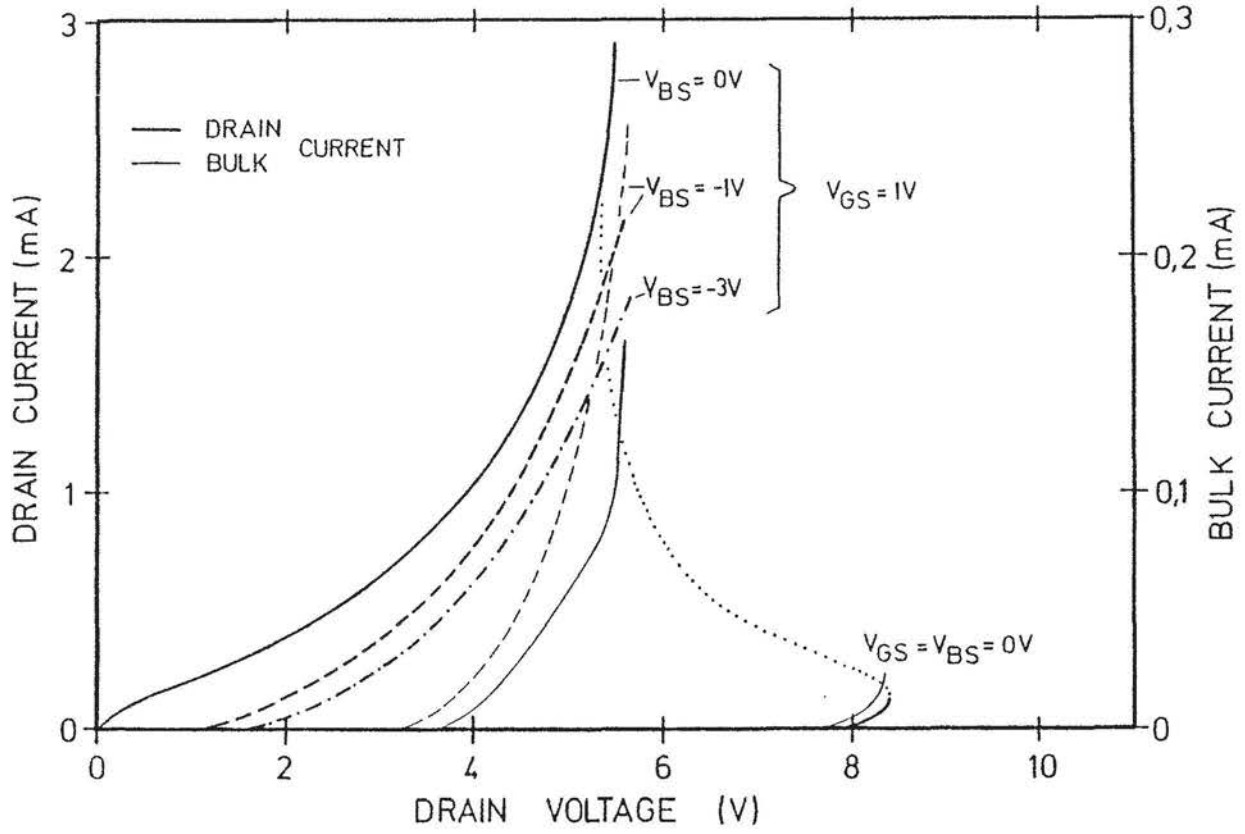


Fig. 5-1 Drain and bulk current characteristics

Although the probability of ionization is larger for $U_{GS}$=0V than for $U_{GS}$=1V, the generation rate still remains small as there is little current flow causing ionization. With increasing drain voltage the drain current and consequently avalanche generation as well as hole density increase. This additional space charge even lowers the potential barrier between source and bulk. Now an internal feedback mechanism exists which acts as follows: Because of the lower potential barrier the electron current injected by source, and consequently, the avalanche generation increase. Thus the hole density rises even more and, in turn, further lowers the potential barrier. Once the feedback gain becomes unity the node currents rise unlimited unless controlled by external resistors in the current paths. Furthermore, owing to the higher current level, the situation now becomes more and more similar to the situation at larger gate voltages. The I-V characteristic, there-

fore, has to move towards the $U_{GS}$=1V characteristic and the drain voltage decreases with increasing drain current. This effect implies negative resistance and is usually called "snap-back". The voltage drop of the hole current at the parasitic resistor of the deep bulk also lowers the potential barrier and thus enhances the feedback gain.

Applying a negative bulk voltage renders breakdown more difficult although it increases the bulk current level. The reason for this phenomenon lies in the hole density which is decreased by applying a more negative bulk bias which attracts the holes.

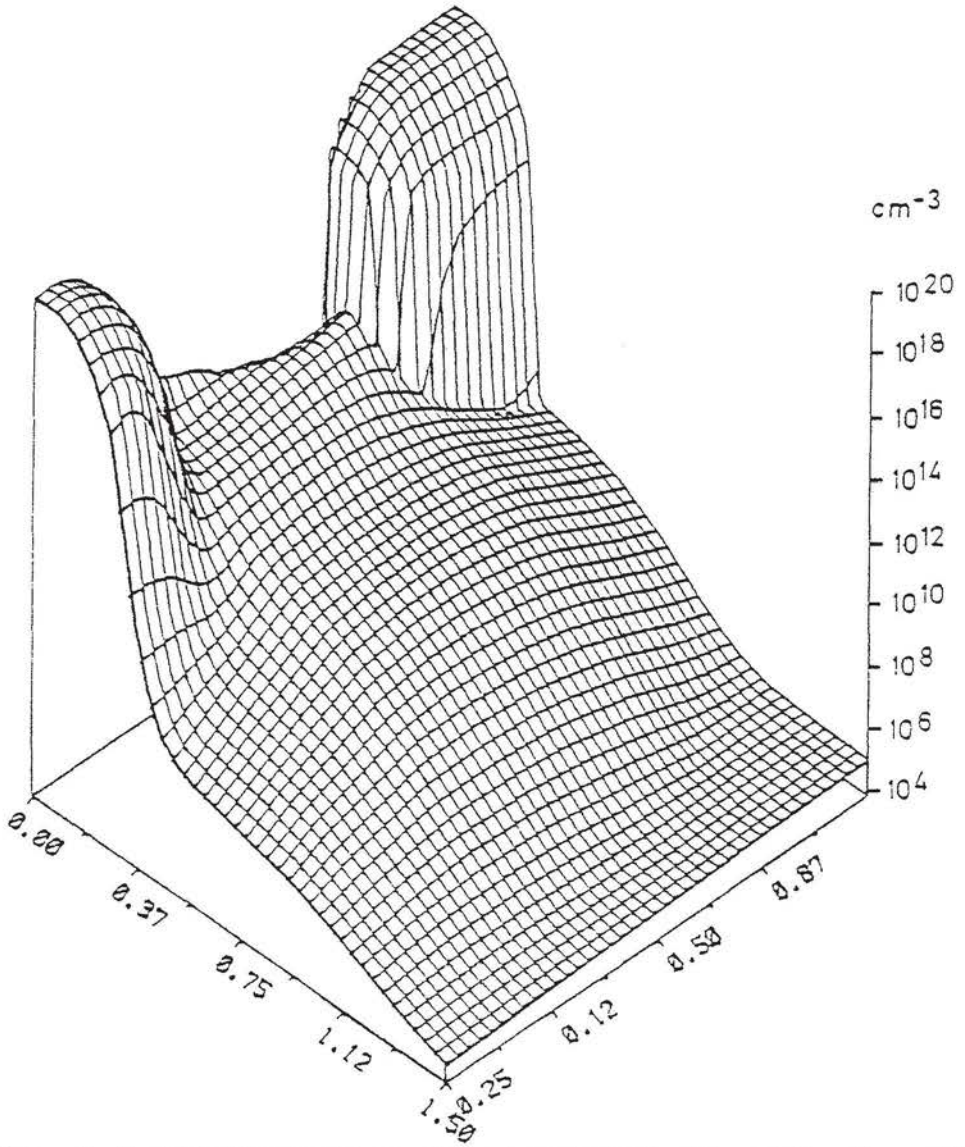


Fig. 5-2 Concentration of electrons ($U_{GS}$=0V, $U_{DS}$=8V)

There exists an additional feedback mechanism apart from the one just mentioned: The carriers generated by ionization cause

again ionization. This effect leads to an "avalanche-like" increase of both carrier densities, and determines the breakdown voltage of a p-n junction. The feedback depends on the ionization ability of both carrier types and is of little importance in our case. For MOS transistors the mechanism described above is much stronger and is active with even vanishing ionization ability of holes.

In the following we should like to discuss internal physical quantities at $U_{GS}$=0V, $U_{DS}$=8V, and $U_{GS}$=2V $U_{DS}$=5.6V, respectively. These operating points have been chosen to explain clearly the physical phenomena which eventually lead to the snap back effect. The computed drain currents are about 20μA and 15mA, respectively. Since the $U_{GS}$=2V characteristic was out of locus bounds, it is not drawn in Fig. 5-1.

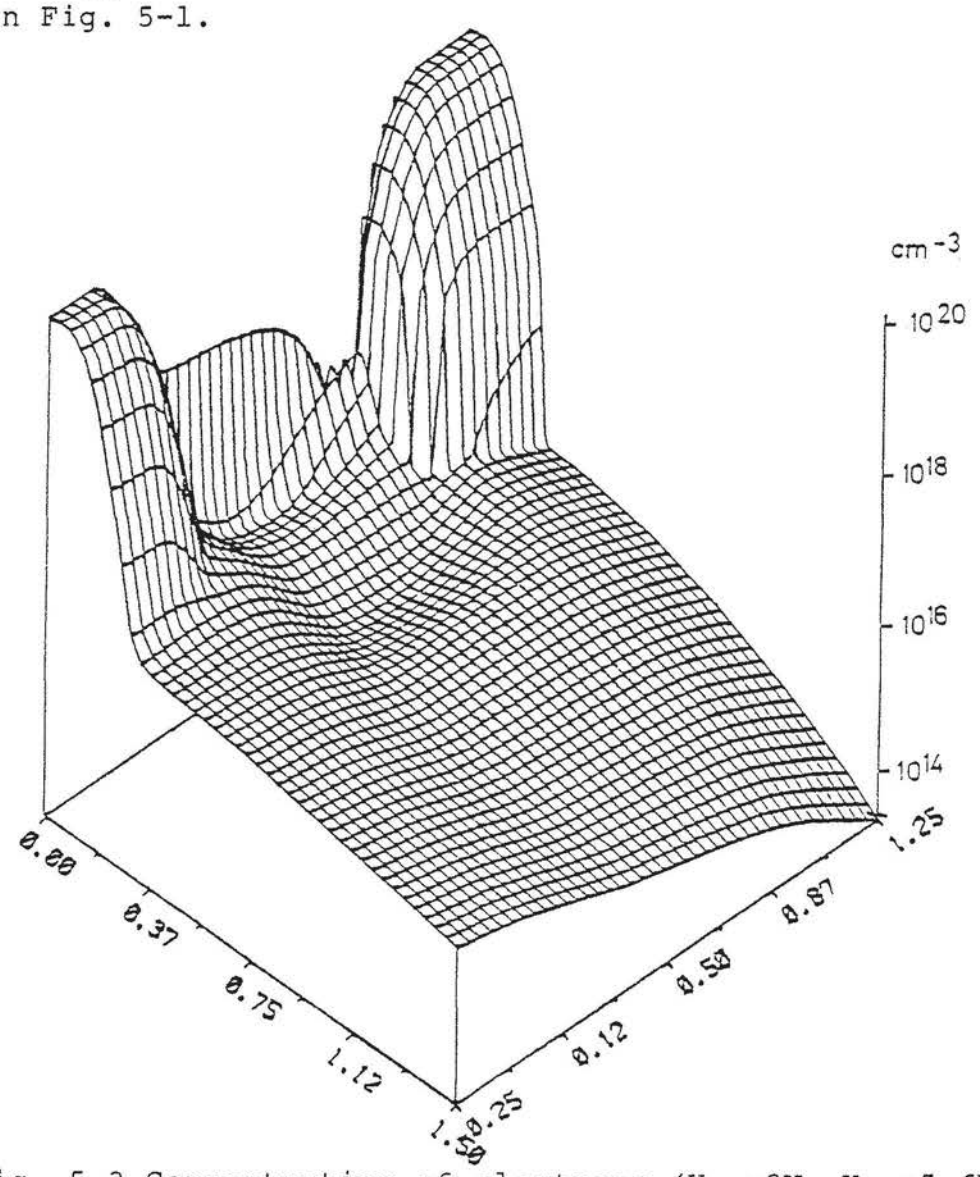


Fig. 5-3 Concentration of electrons ($U_{GS}$=2V, $U_{DS}$=5.6V)

Fig. 5-2 and Fig. 5-3 show the electron distribution for both operating points in a logarithmic scale. At the first operating point, Fig. 5-2, the transistor is turned off; there is no inversion layer between the source and drain regions which can be found, as expected, in Fig. 5-3 at the second operating point. It should be noted that in Fig. 5-3 the electron density does not drop below the intrinsic number in contrast to Fig. 5-2. The reason for this can be found in source barrier lowering brought about by the increased hole density.

The corresponding hole densities are given in Fig. 5-4 and Fig. 5-5, respectively. One should bear in mind that all the holes outside the undisturbed bulk region are generated by impact ionization. In agreement with the electron densities the hole density is also much larger for $U_{GS}$=2V. The large hole density near the source partially compensates the acceptor doping. Thus the potential barrier at the source is lowered and high electron injection from the source region ensues.

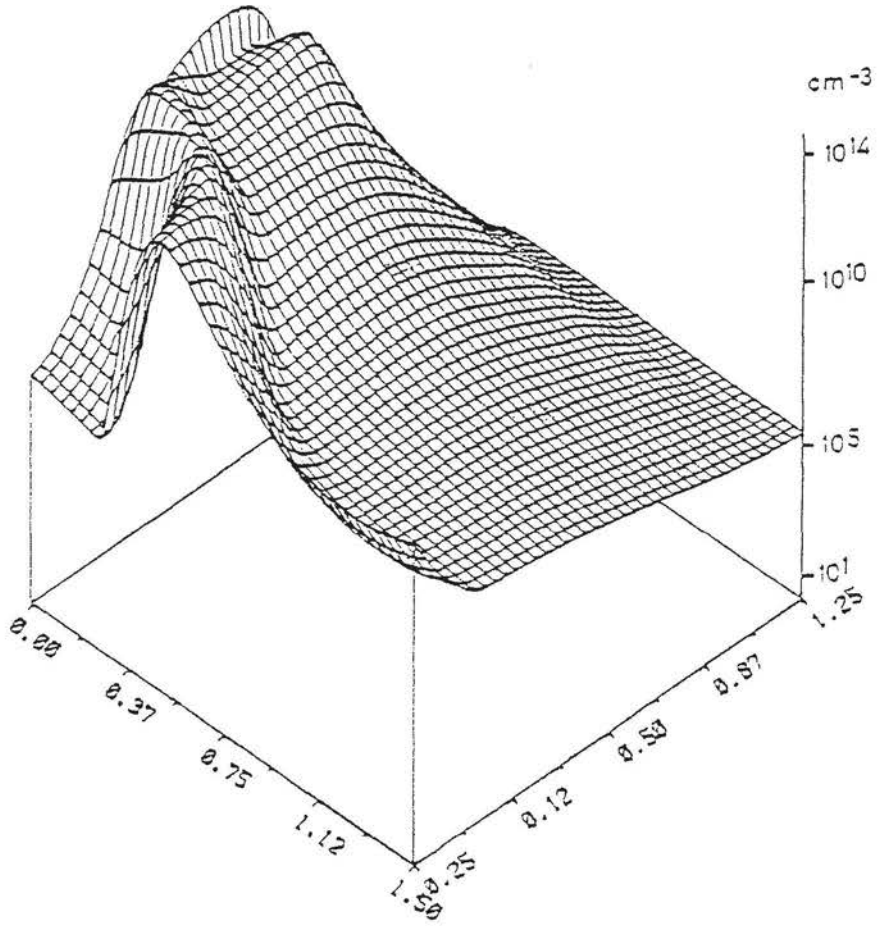


Fig. 5-4 Concentration of holes ($U_{GS}$=0V, $U_{DS}$=8V)

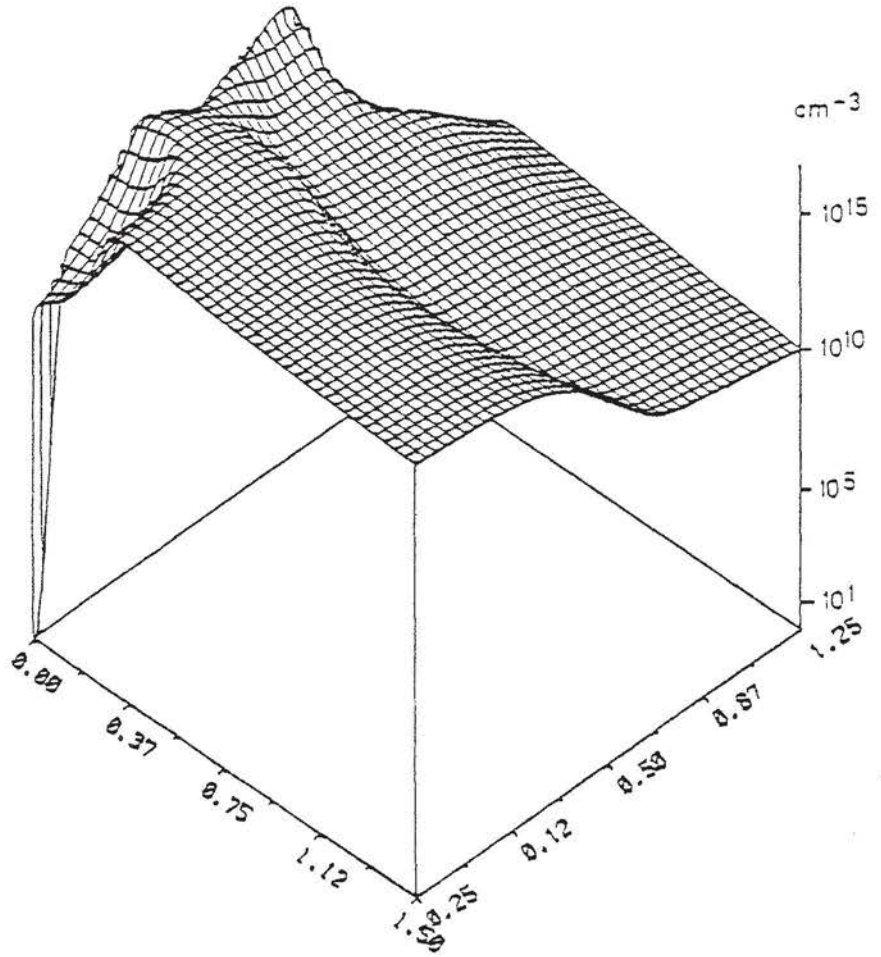


Fig. 5-5 Concentration of holes ($U_{GS}$=2V, $U_{DS}$=5.6V)

Looking at Fig. 5-1 again, we find that the negative resistance branch of the $U_{GS}$=0V characteristic for large current levels leads into a vertical slope, i.e. the decrease of $U_{DS}$ is stopped. The corresponding drain voltage is called "sustain voltage"; it increases weakly with increasing $U_{GS}$ because a large gate bias smoothes the electric field distribution thus lowering its peak value. The existence of a nearly unique sustain voltage can be explained by heavy recombination as demonstrated in /66/.

## 6. CONCLUSION

In this paper we tried to sketch the state of the art in modeling semiconductor devices. It became evident that only progress in basic semiconductor physics will lead to the development of models which are capable of simulating device behaviour more reliably. One highly important objective of a model, its ability to predict the performance of a new device prior to having built the actual device, can only be reached, if the physical parameters of some basic equations are analyzed even more thoroughly. This seems to be the only way to get rid of the enormous amount of fitting parameters and the heuristic formulae which just simulate more or less precisely some complex physical phenomena. The underlying physics has to be analyzed very carefully before one can begin to synthesize a model which is able to simulate reality better. Much effort in analysis and simulation will have to be spent to make device miniaturisation and integration keep pace with the speed of recent days.

## ACKNOWLEDGMENT

This work has been supported by the "Fond zur Förderung der wissenschaftlichen Forschung" (Projekt Nr. S22/11). Essential help of Siemens AG, Munich, in providing MOS devices is gratefully acknowledged. Critically reading our manuscript by Dr. J.Machek is very appreciated. Last but not least the authors wish to thank Dr. D. Schornböck and the whole staff of the computer center for the excellent computer access.

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