F. Straker, S. Selberherr
Abteilung für Physikalische Elektronik
Institut für allgemeine Elektrotechnik und Elektronik
Technische Universität WIEN
Gußhausstraße 27, 1040 WIEN, AUSTRIA

Computation of Integrated Circuit Interconnect Capacitances

ABSTRACT--The two dimensional Laplace equation is solved numerically for various geometries. The surface charges are computed by integrating the normal electrical displacement component over the conductor surfaces. An overdetermined system of linear equations defining the coefficients of capacitance is formed and solved by standard QR-decomposition. Thus numerically reliable and stable capacitance values are obtained. The application of this concept to VLSI design problems is shown by examples.

1) Introduction

The exact knowledge of the influence of device and metallisation capacitances on circuit performance is becoming more and more important by the progressive miniaturization of circuit components and the resulting high packaging density. The wire cross section and spacing is reduced by scaling of the horizontal dimensions. Thereby the impedance - capacitance product increases. The wire capacitance loads the transistor output and deteriorates the transistor switching performance.

2) Calculation of Interconnect Capacitances

The multiconductor capacitance problem is frequently stated in integral equation form. This approach is used e.g. in/5/. The difficulty of this concept is to find and to evaluate Green's Function suitable for the examined conductor geometry. The use of differential methods is used e.g. in /1,2,6/.

Orthogonal series expansion is treated in /3/. Capacitance calculation of three dimensional multiconductor systems is investigated e.g. in/4/.

Equation (1) defines the coefficients of capacitance in a n-conductor system:

$$Q_i = \sum_{\substack{j=1 \\ j\neq i}}^{n} C_{ij}(\Phi_i - \Phi_j) + C_{ii}\Phi_i \qquad (1)$$

Q_i denotes the charge, Φ_i the electrostatic potential and C_{ii} the capacitance of conductor i, C_{ij} is the coupling capacitance between conductor i and conductor j. This paper is concerned with the calculation of the $1/2 \cdot n(n+1)$ coefficients C_{ij}. The approach to accomplish this task is described in the following paragraphs.

The two dimensional Laplace equation is solved numerically by means of a finite difference method. The domain represents a cross section of a multiconductor/multidielectric system. The number of conductors/dielectrics is only limited by the available computer resources. The computed potential distribution allows the calculation of the charge distribution on the conductor surfaces.

For the non-trivial case of more than two conductors ($n > 2$), we use multiple solutions of Laplace's equation with different boundary conditions to compute all the C_{ij}. The i-th solution is computed with

$$\Phi_j = 1,\ j=1,\ldots,i; \quad \Phi_k = 0,\ k=i+1,\ldots,n.$$

This approach leads to an overdetermined system of equations (2) for the C_{ij}

$$A\,c = q \qquad (2)$$

c and q are the vectors with components C_{ij} and Q_i respectively. Introducing the singular value decomposition of the matrix A

$$A = UQV^T \qquad (3)$$

into (2) and solving for the unknown vector **c** with a standard QR-decomposition algorithm results in

$$\mathbf{c} = VQ^{-1}U^T\mathbf{q} \qquad (4).$$

The advantage of this method is obvious. The QR algorithm evaluates the equation with the best condition number first, giving numerically reliable and stable results.

3) Application and Discussion

To carry out a rigorous test of the method we recalculated data already published. Comparisons with /2/ and /5/ show good agreement of the results within 2% to 10%. We present the results of investigations concerning

a) the impact of thickness and material of passivating layers and line spacing on the capacitance of VLSI interconnections;

b) the calculation of the mutual capacitance between transfer gate and bit line of a dynamic RAM cell.

3.1) Interconnection Capacitances

We calculated the mutual and the substrate capacitances of the lines shown in Fig. 1. Note that only half images of the conducters have been drawn. For the further discussion the following geometry was used: W/T=6, H/T=1, L/T=.75. Line spacing varied from S/W=.375 to S/W=2.125. Four types of lines were studied:

Oxide passivated ε_r=3.9 G/T=1.5 (L1) and G/T=.75 (L2)
Nitride passivated ε_r=7.0 G/T=1.5 (L3) and G/T=.75 (L4)

Simulation Geometry

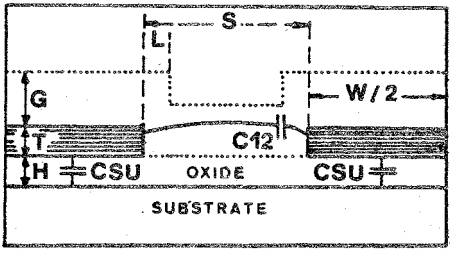


Fig. 1

Parallel Plate Capacitance

$$C_{12} = \frac{\varepsilon_o \cdot \varepsilon_r}{6} \cdot \frac{1}{(S/W)}$$

MUTUAL CAPACITANCE C12

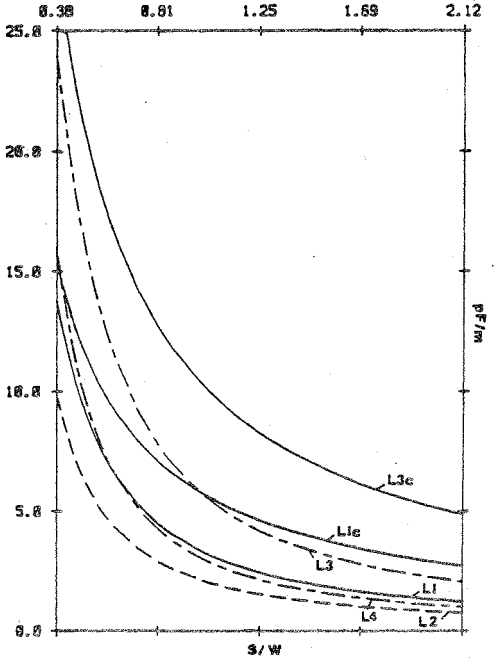


Fig. 2

You see the plot of mutual capacitance C_{12} vs. spacing S/W in Fig. 2. Comparing the curves L2-L3 capacitance relations of $a_1=C_{12L3}/C_{12L2}=2.44$ at S/W=.375, $a_2=2.80$ at S/W=1.25 and $a_3=2.73$ at S/W=2.125 are obtained. This three spacing values will be used for comparison throughout this chapter. Thickness and material of the passivating layer can change the mutual capacitances by a factor of 2.8 in the worst case.

The passivation material affects the line capacitance via its dielectric constant ε_r. Using a thick passivation layer (L1-L3) gives nitride/oxide capacitance relations of $a_1=1.63$, $a_2=1.71$ and $a_3=1.58$. The material dependence is largest at medium spacings. Looking at the curves for thin passivation (L2-L4) reveals $a_1=1.61$, $a_2=1.40$ and $a_3=1.33$. The material influence on the capacitance is most important at small line spacings.

Setting up the capacitance relations for the two oxide passivations (L1-L2) at the standard spacings gives $a_1=1.50$, $a_2=1.63$, $a_3=1.73$. The largest dependence on thickness G occurs at S/W=2.25. Furthermore notice the approximately proportional growth according to line spacing. Repeating this comparison for the nitride case (L3-L4) yields $a_1=1.51$, $a_2=2.00$ and $a_3=2.05$ respectively. Again the thickness impact on capacitance is biggest at large spacings but growing of the thickness dependence is very slow after reaching medium spacings.

Also included in Fig. 2 are curves that show the mutual capacitance for L1 and L3 calculated with the formula for a parallel plate capacitance. This curves are labeled L1c, L3c and overestimate the true value, say, 150% in the average.

Fig. 3 shows the substrate capacitance of the cases L1...L4 vs. spacing. Comparing L2-L3 and thus obtaining $a_1=1.025$ and $a_3=1.135$ shows a minor dependence on passivation processing. Influence of layer thickness and material is less than 10%. This was expected because the relevant electric field is between the conductor bottom and substrate surface mostly in

the oxide layer. With W/T=6 fringing effects are not yet significant. For decreasing W/T ratio greater substrate capacitance variation is expected.

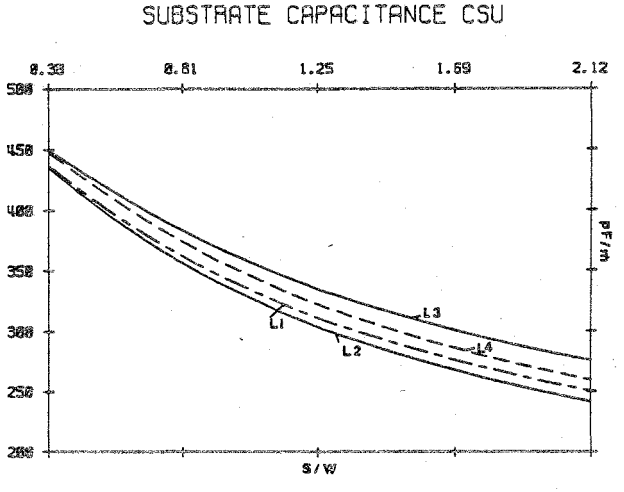


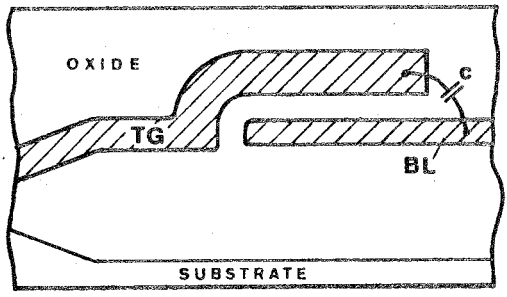
Fig. 3

3.2) Dynamic RAM Cell

Fig. 4a shows a detail of a one transistor RAM cell. Fig. 4b shows the simplified geometry actually used for simulation. C denotes the mutual capacitance between transfer gate and bit line. For the cell designer a decomposition of C in C_1 and C_2 and a rest capacitance C_3 is desirable because of layout considerations. It is not possible to achieve such a decomposition via series of electrical measurements. Computer simulation delivers such a separation as a byproduct.

The simulation was carried out on a non-aequidistant grid using 36 gridlines in horizontal and 34 in vertical direction. Near the conductor surfaces the grid was chosen up to four times finer than in distant regions to obtain accurate surface charge values. The capacitances have been evaluated to C=374.9 pf/m, C_{1sub}=130.9 pf/m and C_{2sub}=83.0 pf/m. The relative numerical error was less than 10^{-7}.

RAM Cell Detail



Simulation Geometry

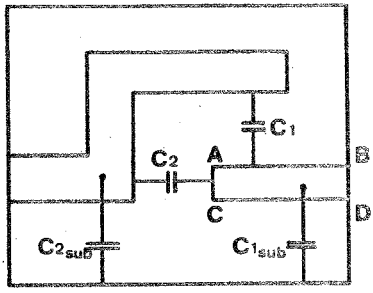


Fig. 4a (Fig. 4 not to scale) Fig. 4b

To decompose the capacitance as stated above we computed the following 'subcharges'

$$Q = q_1+q_2+q_3 = \varepsilon\int_A^B E\cdot dA + \varepsilon\int_C^A E\cdot dA + \left(\varepsilon\int_C^D E\cdot dA + \varepsilon\int_D^B E\cdot dA \right) \quad (5)$$

The capacitance decomposition

$$C_i = C \cdot q_i/Q \qquad i=1,2,3 \quad (6)$$

evaluates to C_1=222.8 pF/m, C_2=48.0 pF/m and C_3=104.1 pF/m.

4) Conclusions

Mutual and substrate capacitances of four VLSI interconnection types were calculated vs. line spacing. The passivation process has strong influence on the mutual but minor influence on the substrate capacitances. Material dependence is different for thin and thick passivation layers.

The transfer gate - bit line capacitance of a dynamic RAM cell was numerically calculated. Because of layout considerations a decomposition into three capacitance components was performed.

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