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2-D STEADY STATE AND TRANSIENT SIMULATION OF POWER THYRISTORS

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Abstract

This paper presents a novel program system capable of simulating 2-D transient device behaviour under various operating conditions. Automatic set up and refinement of the grid by equidistribution of the local discretization error has been implemented in view of a reasonable amount of computer resources. For the time discretization an automatic time step control algorithm is used. The new time step is calculated with a predictor-corrector method. Due to the possibly large variation of the solution during transient simulation, it is necessary to introduce a "Moving Grid". This is accomplished by tracing the local discretization error which is equidistributed by inserting grid points. As an example the rate effect in thyristors is analyzed for devices with and without emitter shorts. The shorted devices are not triggered even if the distance between shorts is increased to 1.4 mm, whereas simulations of equivalent devices without the emitter short show fireing.

Introduction

The optimum design of power thyristors requires numerical analysis tools capable of simulating device behaviour under various conditions. Special emphasis must be laid on the transient simulation of such structures. In spite of a number of successful aproaches /1/-/3/ no efficiently applicable program has been designed so far. The extreme operating points (high voltages or high current densities) have forced restrictions on bias conditions and/or geometry. Therefore we have designed a more rigorous approach to the solution of the semiconductor partial differential equation (PDE) system. An exact numerical 2-D transient model with locally refined grid structures, automatic grid adaption to the different stationary and transient operating points, and an automatic time step control algorithm will be presented. The design and handling of the program system is explained in /4/. This paper here concentrates on the discretization methods both for space and time. Algorithmic aspects will be explained first, followed by a discussion of the advantages of numerical methods over

heuristic ones. A detailed investigation of the rate effect in power thyristors will give an insight into the broad range of applications for the program sytem BAMBI (Basic Analyzer of MOS and BIpolar devices).

Theory

The numerical analysis of semiconductor devices requires the solution of three PDEs (Poisson's equation and two continuity equations for electrons and holes, respectively). Considering typical properties of power devices (large geometries, high voltages, high current densities) special emphasis has to be laid on the discretization methods in order to guarantee convergence and to limit the expenditure of computer resources. The methods used in BAMBI will be outlined and discussed in the following sections.

Spacial discretization - "Finite Boxes"

Basically there are two possible approaches for the discretization of space in two dimensions: the finite difference and the finite element method. Both of them have been discussed in many papers and we will not contribute to that here. Instead, we have developed a more generalized method, based on finite differences, the so called "Finite Boxes" discretizations /5/ which can be described as follows: usually a finite difference grid consists of a regular pattern of rectangles, which means that a mesh line passes throughout the whole device. This leads to a large number of points in regions where a coarse grid suffices (eg. the weakly doped bulk) if there is a small part of the device requireing a very fine grid (eg. a shallow emitter in a power thyristor). Therefore, particularly in power devices the computer resources are dramatically increased. A better approach is to restrict the fine mesh to regions where it is enforced by the PDE system and to generate a coarse grid in domains where the solution does not vary much. This idea is realized in the "Finite Boxes" concept. The mesh is built up by rectangular cells of different size according to the variation of the solution. This method permits lines to terminate anywhere in the device in any direction. Figs. 1 and 2 show the difference between this approach (Fig. 1) and the classical

finite difference grid. The advantages of the "Finite Boxes" method are not only a reduction of the total number of grid points by more than 50 % but also a number of other important aspects:

- First of all improved stability of the solution of the PDE system is achieved because of the fact that there are only few mesh points in domains where the solution is constant. Otherwise, due to a large length to width ratio of grid distance oscillations may occur if the change from small boxes to large ones is too rapid.
- Secondly and even more important is the possibility to generate a mesh for an arbitrarily shaped device automatically. A mapping is used for the representation of the grid points. For the initial guess new grid points are inserted locally according to the specified device geometry and the doping profile. During the iteration process the mesh is refined by evaluating a weight-function (local discretization error) until both the solution and the truncation error match their criteria.
- It is also possible to trace the local discretization error during transient analysis and to introduce a "Moving Grid". Considering the building up and removing of space charge regions during turn-off and turn-on of thyristors such a concept is of particular interest. Not the whole mesh lines must be shifted, like it should have been done in a classical grid, but adaption of the grid is restricted to small areas around the critical regions.

Time discretization - Transient Analysis

Numerical analysis of thyristors, particularly of GTO-elements, requires steady-state as well as transient calculations. Therefore, we have implemented algorithms for a time dependent solution in BAMBI. Again we have to consider carefully the discretization methods for the time domain. Following the design rule, to establish an easy to use and very flexible software tool, an automatic time step control algorithm has been implemented. We use a standard backward Euler method for the transient solution of the semiconductor equations, which implies no methodological restrictions on the time steps. Never the less, accuracy as well as convergence properties are highly influenced by the choice of the step width. Up to now heuristic methods have

been used /2/, /3/, but only an automatic algorithm based on a mathematical calculus can guarantee stability for arbitrary devices. In BAMBI a corrector-predictor method is implemented. The space charge change between two succeeding time steps is calculated. If it reasonably small (typically lower than 0.1 As/cm^3) the new time step can be up to twice as large as the old one. If it increases during transient analysis, the time increment is decreased. This calculus is the transient equivalent to the weigth-function for the spacial discretization and can be looked upon as a time discretization error. Investigations showed that the analysis of the switching behaviour of majority devices like DMOS transistors require smaller time steps than that of minority devices (eg. bipolar transistors). The turn-on of a SIPMOS transistor /6/ does not allow larger time steps than $\Delta t = 1$ ns during the final formation of the electron channel whereas in transient analysis of the GTO-performance the time steps are mainly restricted by the "Moving Grid" criterion as outlined in the next section.

In case of poor convergence, the actual time step, Δt_n, is dropped and the calculation is restarted from the solution at point t_{n-1} with a smaller increment. Since the fully imlicit method causes a Newton iteration at each time step, we need an initial guess. It is derived by linear extrapolation of the previous two solutions at points t_{n-1} and t_{n-2}. As explained previously the local discretization error is traced during the transient analysis. If the error exceeds a certain tolerance value the mesh is adapted. In this manner, the calculation is always accomplished with a minimum number of mesh points saving a great deal of computation time.

As an example we present the "Moving Grid" during dU/dt-triggering of a thyristor. Details of the geometry and doping profile can be found in the result section. In this particular investigation the emitter width is 600 um. Fig. 3 shows a section of a "Finite Boxes" grid 20 um deep around the cathode contact for the steady state operating point at $U_A = 0V$, at $t = 1.66$ ns ($U_A = 8.3V$) and $t = 82.3$ ns ($U_A = 411.4V$). The lateral voltage drop along the emitter forces a refinement of the grid there. The largest distance between grid points in x-direction shrinks from 300 um at $t = 0$ to 75 um at $t = 82.3$ ns.

Results

The program system BAMBI has been successfully applied to the analysis of thyristors /7/, GTO-elements /8/, GaAs MESFETs /9/ and SIPMOS transistors /4/. Steady state calculations of power thyristors have been presented in /7/ both for 2-D planar and cylindrically symmetric devices. In this paper we concentrate on the study of the rate effect in thyristors and the influence of emitter shorts.

The Rate Effect in Thyristors

As it is commonly known a n-p-n-p structure can be triggered either by injection of carriers through the gate contact into the p-base or by a displacement current resulting from a steep ramp of anode voltage, which is called the rate effect. The current flow is proportional to the dU/dt value of the ramp. The emitter is forced to inject carriers into the p-base which drift towards the blocking p-n-junction. If the ramp is steep enough, the device is fired. This unwanted triggering can be avoided by emitter shorts. They set the emitter potential equal to the p-base potential and so injection of electrons is prohibited. In the following two sections both effects will be studied.

Triggering of a n-p-n-p Structure

The device geometry of the analyzed thyristor element is shown in Fig. 4. The device exhibits a cylindrical symmetry. The calculations can be performed quasi three dimensional after reformulation of the basic semiconductor equations in cylindrical coordinates /7/. The cathode contact is assumed to be a circular area with 96 um radius. The device is assumed to have a floating gate. Fig. 5 is a plot of the doping profile. A steep voltage ramp has been applied to the anode (1):

$$U_A = 1000\ V/us \cdot t \qquad (1)$$

Fig. 6 shows the anode current versus time characteristic. A constant current value can be observed for about 50 ns (corresponding to an anode bias of 50V). This current loads the depletion capacitance.

After that period we can observe a linear increase of the anode current with a slope of about 15 mA/us. This increase becomes exponential and leeds to triggering at t = 450 ns (U_A = 450V).

In the following we discuss snapshots of the electron and the hole concentrations. Figs. 7 and 8 show the electron and hole concentrations at t = 0, i.e. at equilibrium. The next series is taken at t = 25 ns (U_A = 25V) during the load phase (Fig. 9,10). We observe that the electron concentration in the p-n-junction, which should block, is increased, due to injection from the emitter, and the holes injected from the anode flood the bulk. The next snapshot is taken at t = 170 ns (U_A = 170V). The electron concentration (Fig. 11) shows a slightly more extended depletion region, but the level is already above the intrinsic concentration. The injection of holes (Fig. 12) from the anode is so strong that the entire n-body is flooded now. The final series is taken just before triggering at t = 430 ns (U_A = 430V). The carrier concentrations (Figs. 13,14) have reached enormously high values during this operating condition. There is almost no barrier left, particularly regarding the hole concentration.

Analysis of Emitter Shorts

The dU/dt triggering is usually prohibited by emitter shorts. The displacement current in the blocking p-n junction is continued by a conduction current through the p-base where the carriers are exhausted by the short. So, the injection of electrons by the emitter is suppressed. This ideal description neglects the lateral expansion of the device. The holes collected by the p-base contact pass laterally along the emitter and induce a voltage drop there. If the bias in the centre of the emitter reaches 0.7V the emitter starts to inject electrons in spite of the short. The effectiveness of the short depends on the lateral dimensions and on the p-base sheet resistance. In the following section these considerations are proved by 2-D numerical simulations.

The basic geometry and the doping profile of the analyzed device is identical to that in the previous section. The emitter short is simulated by connecting gate and cathode contact (equal bias value). At the anode a voltage (2) is applied.

$$U_A = 5000\ V/us \cdot t \qquad (2)$$

The steady state solution at equilibrium is certainly identical to that of the unshorted device (cf. Fig. 7,8). The calculated I(t) - characteristic is plotted in Fig. 15. A constant load current into the depletion capacitances can be observed for about 20 ns. Then the anode current decreases towards a constant level (depletion current). The emitter short prohibits the injection of electrons into the p-base and the space charge layer around the blocking junction is formed. According to the calculus deduced in the theory section the time steps are continously increased (up to Δt = 100 ns). At t = 360 ns (U_A = 1800V) an abrupt rise of the anode current due to beginning carrier multiplication in the space charge layer occurs. The current increases dramatically up to 0.2 A where the slope decreases because of the n^- sheet resistance. The effect of avalanche generation can clearly be seen in the plots of the carrier concentrations at t = 360 ns (U_A = 1800V) and t = 380 ns (U_A = 1900V) (Fig. 16-19). The electron and hole concentrations immediately before the avalanche breakdown (Fig. 16,17) exhibit a 150 um thick space charge region in the centre of the device. In the following plots (Fig. 18,19) at t = 380 ns this layer has been removed completely by the generated electron-hole pairs. The emitter starts to inject electrons into the p-base. In Fig. 20 the total generation - recombination rate is plotted quasi logarithmically ($z = sign(a)*log(1+a/10^{18})$). The large area of carrier multiplication can be seen, but towards the anode recombination dominates because of the injected holes.

This result demonstrates the effectiveness of the assumed emitter short. The thyristor - designed to block 1600V - is not triggered by the steep ramp voltage up to its performance limits. The maximum possible distance between emitter shorts able to block the assumed dU/dt of 5000 V/us has been investigated. The results are summarized in Fig. 21. The average cathode current densities over time are plotted for different emitter widths. The area underneath the curves equals the total charge (electrons) injected by the emitter during the rapid anode voltage increase. Up to an emitter width of 1400 um this charge is too small to trigger the device.

Conclusion

A novel 2-D transient simulation system BAMBI has been presented. Basically it has been designed for the analysis of power devices with respect to the high voltage/high current operating points. Sophisticated algorithms for the spacial and time discretization have been designed and successfully applied. As a demonstration, the results of a study of the rate effect in power thyristors have been presented and analyzed.

Acknowledgement

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References

/1/ M.S.Adler, V.A.K.Temple, IEEE Trans.Electron Devices, vol. ED-27, pp.483-494, Feb. 1980.

/2/ A.Nakagawa, D.H.Navon, IEDM Technical Digest 1982, pp.496-499.

/3/ Y.Shimizu et al., IEEE Trans.Electron Devices, vol.ED-28, pp.1043-1047, Sept. 1981.

/4/ A.F.Franz et al., Proc. AMSE Int. 84 Athens Summer Conf., 1984.

/5/ A.F.Franz et al., IEEE Trans.Electron Devices, vol.ED-30, pp.1070-1082, Sept. 1983.

/6/ A.F.Franz, to be published.

/7/ G.A.Franz et al., Proc. NASECODE III Conf., pp.122-127, June 1983.

/8/ G.A.Franz, M.Stoisiek, IEDM Technical Digest 1983, pp.214-217.

/9/ A.F.Franz et al., Proc. NASECODE III Conf., pp.117-121, June 1983.

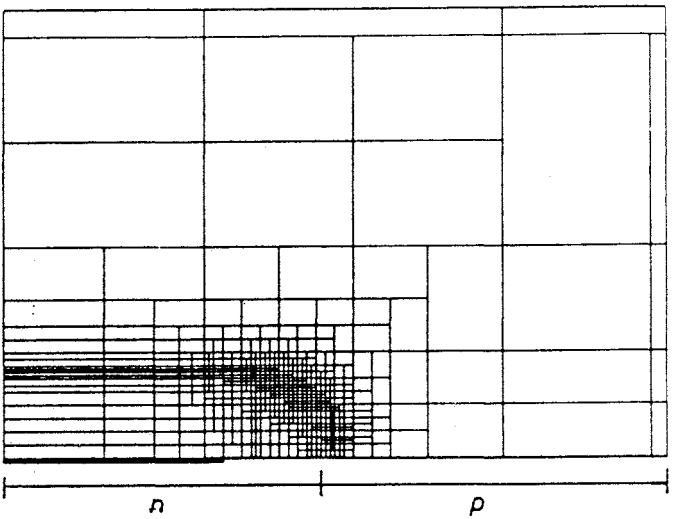

Fig. 1: Finite Boxes Grid for a p-n junction.

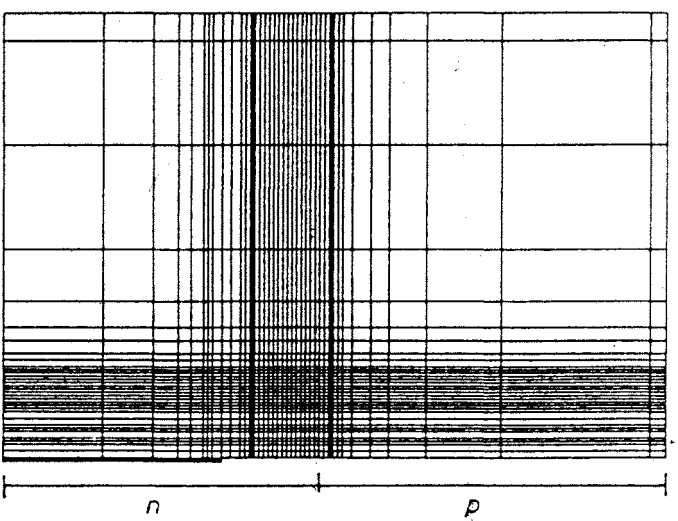

Fig. 2: Finite Differences Grid for a p-n junction.

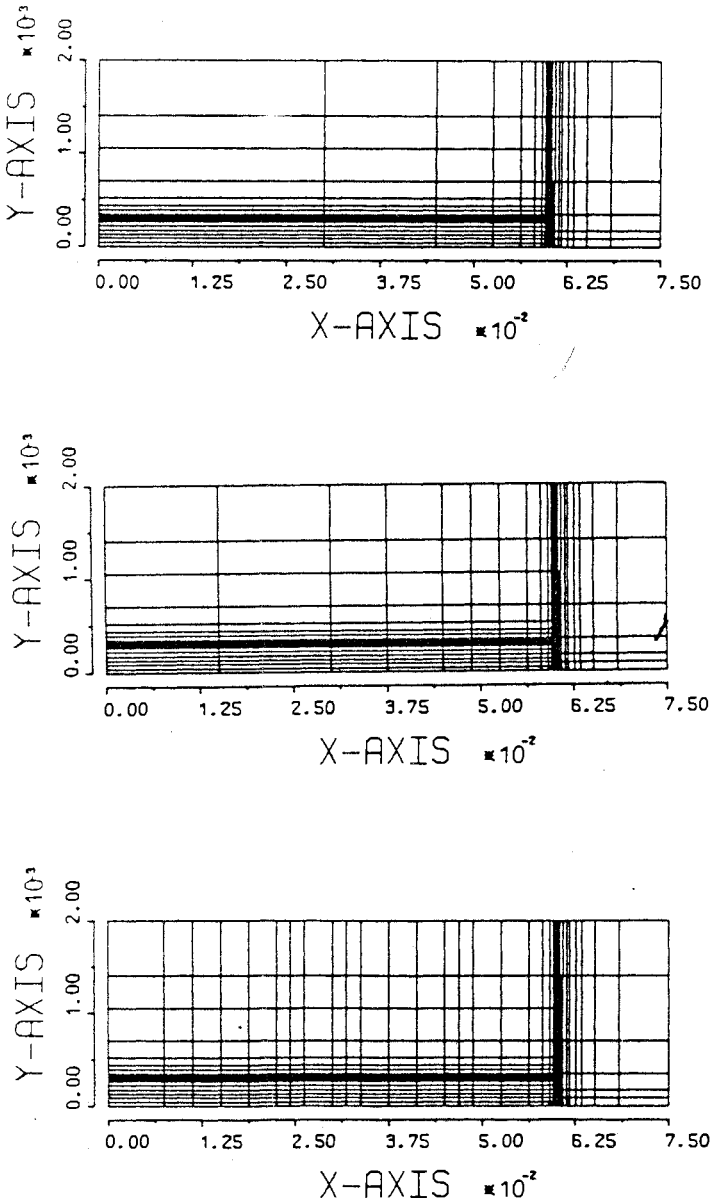

Fig. 3: Section of a Finite Boxes Grid
(750 um x 20 um) for a thyristor
at t = 0, 1.66 ns and 82.3 ns.

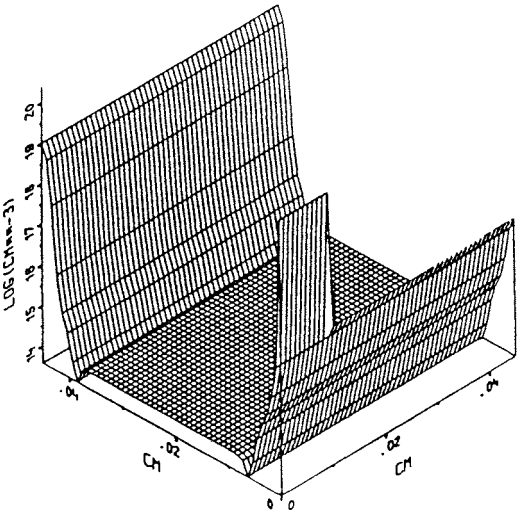

Fig. 5: Doping Concentration for the thyristor.

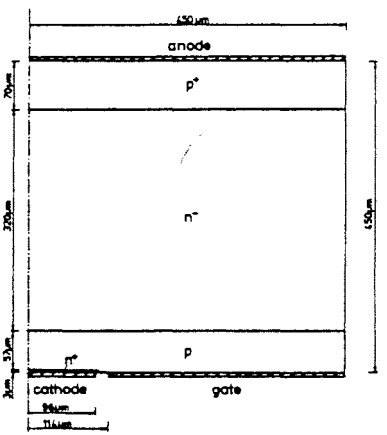

Fig. 4: Simulation Domain for the analyzed thyristor.

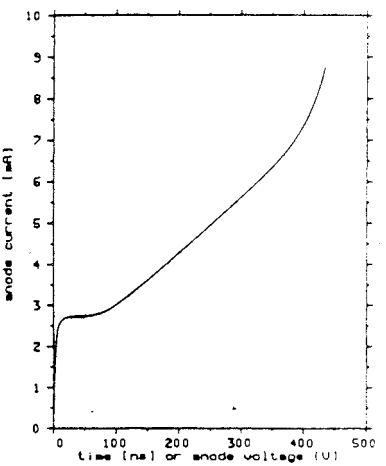

Fig. 6: Transient Anode Current for U_A = 1000 V/us·t

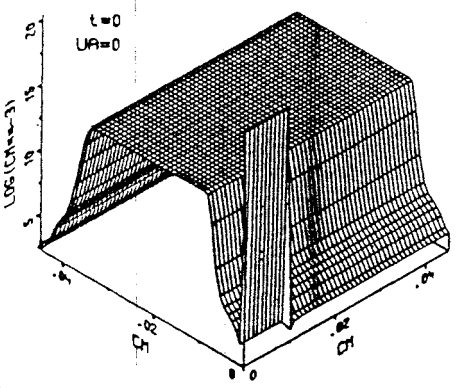

Fig. 7: Concentration of Electrons at t = 0.

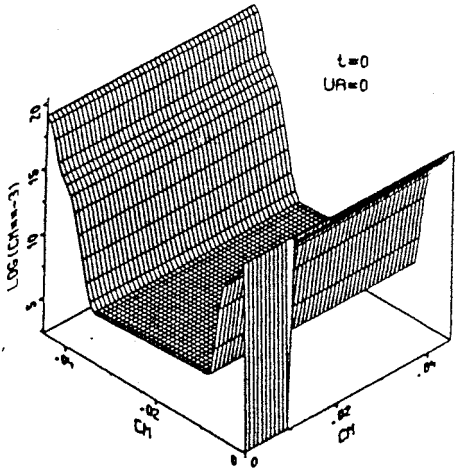

Fig. 8: Concentration of Holes at t = 0.

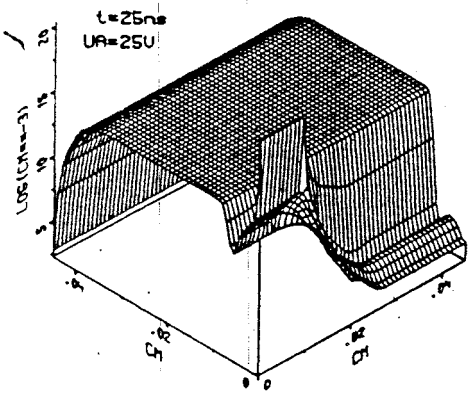

Fig. 9: Concentration of Electrons at t = 25 ns.

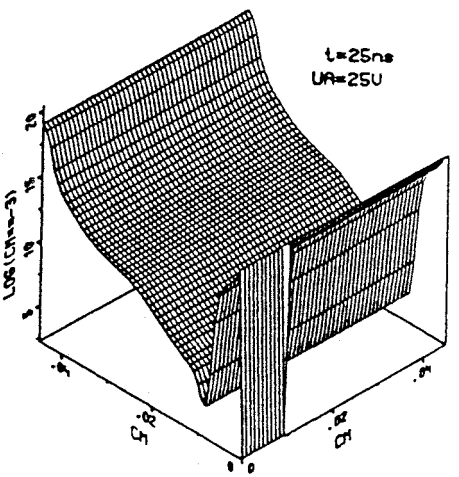

Fig. 10: Concentration of Holes at t = 25

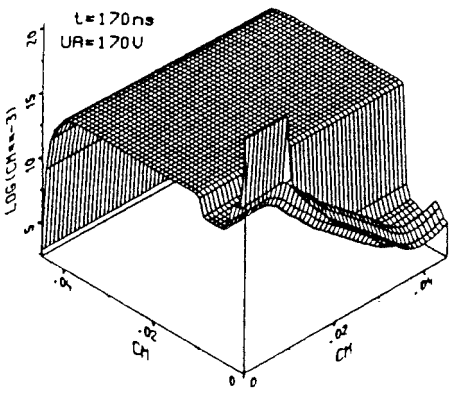

Fig. 11: Concentration of Electrons at t = 170 ns.

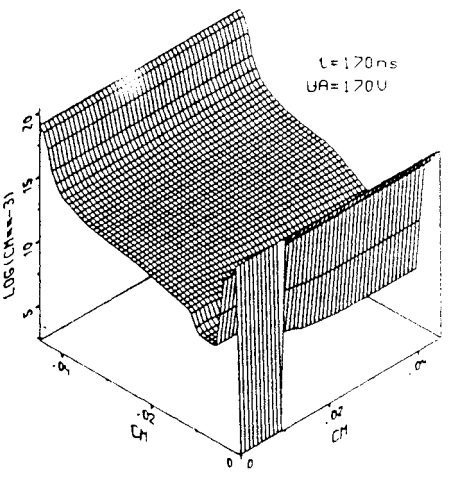

Fig. 12: Concentration of Holes at t = 170 ns.

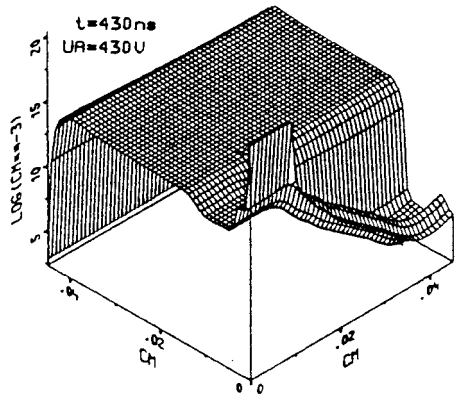

Fig. 13: Concentration of Electrons at t = 430 ns.

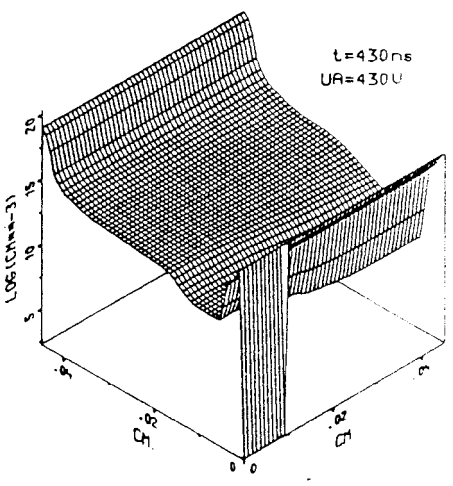

Fig. 14: Concentration of Holes at t = 430 ns.

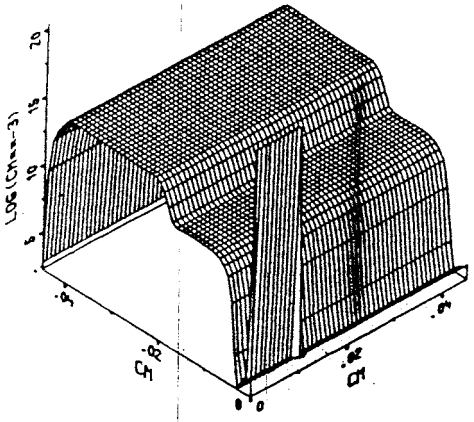

Fig. 16: Concentration of Electrons at t = 360 ns (U_A = 1800V).

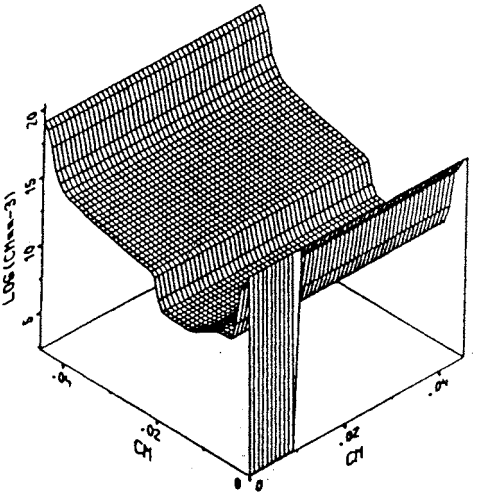

Fig. 17: Concentration of Holes at t = 360 ns (U_A = 1800V).

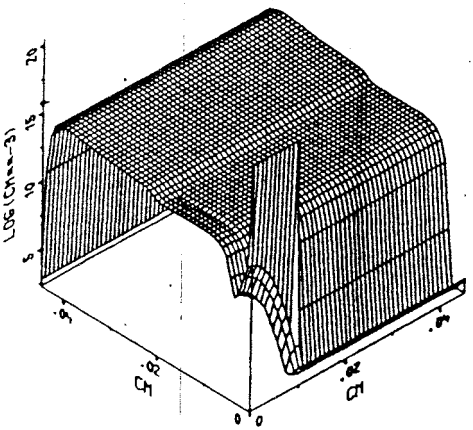

Fig. 18: Concentration of Electrons at t = 380 ns (U_A = 1900V).

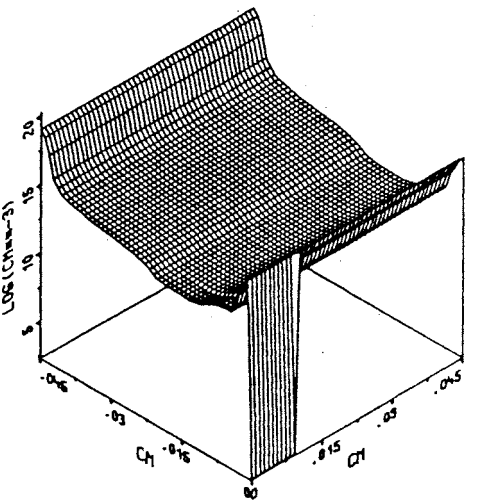

Fig. 19: Concentration of Holes at t = 380 ns (U_A = 1900V).

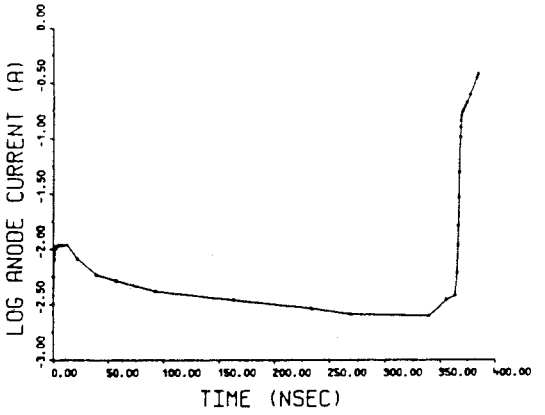

Fig. 15: Transient Anode Current for U_A = 5000 V/us·t.

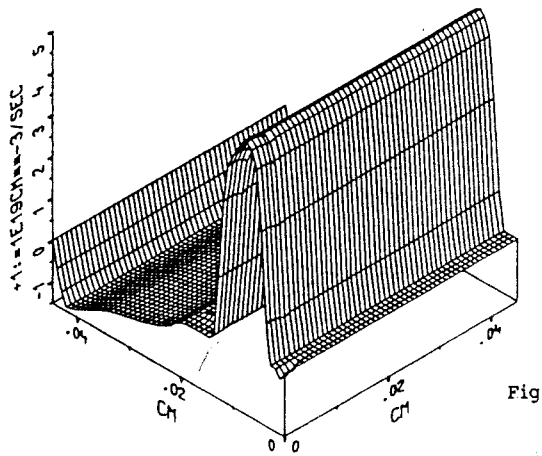

Fig. 20: Generation - Recombination Rat at t = 380 ns (U_A = 1900V).

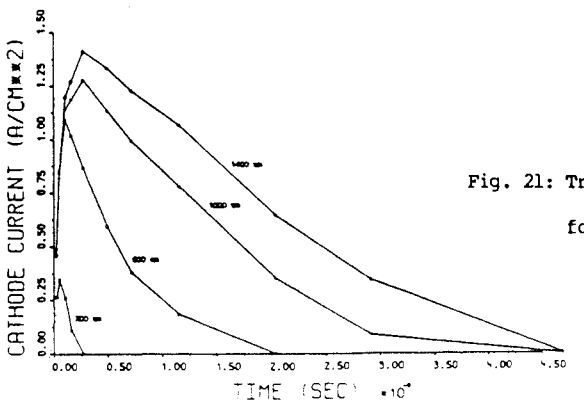

Fig. 21: Transient Cathode Current Densitie for different Emitter Widths.