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NUMERICAL 2-D SIMULATION OF VERTICAL POWER MOSFET'S

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Abstract

The area of application for power MOSFETs has steadily increased in spite of the fact that these devices appeared on the market only a few years ago. Their greatest advantages over bipolar power devices involve their fast switching capability and the presence of a well defined safe operating area, which stems from the lack of second breakdown. This broadening of application requires not only measuring the devices but also simulating their performance with numerical tools. To help tackle this problem, the program-system BAMBI (Basic Analyzer of MOS and BIpolar devices) has been developed to analyze arbitrarily shaped devices using new simulation techniques. It has been succesfully applied for the simulation of vertical DMOS power transistors. The presented results, concerning a particular SIPMOS transistor, encompass the three different ranges of the IV-characteristic.

Introduction

Semiconductor device simulation has become more and more necessary when one considers the time period required from the design to the production and the ability to measure the device. Most of the published simulation systems are restricted to certain aspects: either to a special kind of device or to predefined physical parameter models. Therefore it was our goal to design a program of broad generality, which can handle both bipolar and MOS devices, which is not resticted to a rectangular device geometry and which handles arbitrary physical parameter models, even tabulated data obtained by measurements. This program system BAMBI (Basic Analyzer of MOS and BIpolar devices) is described in the first section.

One application is the investigation of vertical power MOSFETs, in particular SIPMOS transistors. The simulation results are described in the second section. They encompass both calculated IV-characteristics in comparison to measured results and internal distributions for typical bias points.

BAMBI - the numerical tool

First of all the advantages of BAMBI shall be outlined. The Input-Output-flow in the program system has been designed as follows: BAMBI is a three pass concept.In Pass 1 the user input is processed, in Pass 2 the three semiconductor equations are solved by a simultaneous Newton method, and in Pass 3 the "Post-Processing" (line printer output, plots, etc.) is performed.

The input of Pass 1 contains all the information about the device to be simulated: The boundaries are described by polygons, with each edge having a unique boundary condition (Dirichlet condition for contacts and Neumann condition for free surfaces). The polygons describe a semiconductor area where all 3 partial differential semiconductor equations (PDE) are solved and in the case where surrounding dielectrica are also specified, only the Laplace equation is calculated. Due to the fact that very different devices can be analyzed, it is necessary to formulate a rather generalized initial guess: space charge neutrality and carrier equilibrium. This starting condition is not sufficient if a device has two steady state solutions for one bias point, like a thyristor. It is then necessary to allow for the option of a high injection starting condition, where an initial plasma, existing throughout the device, is estimated.

The program system is not only able to simulate DC-characteristics but also to analyze transient behaviour. In order to step a characteristic a "step" - command has been established taking a previously calculated bias point as the initial guess for a succeeding bias point. Another item is the "restart" - option which is very helpful if the user wants to investigate the influence of certain parameters and their variations on the device. As explained in the following paragraph each model can be easily changed and, by taking the previous calculations as input, sensitivity tests can be performed. This user input is read by Pass 1, checked and subsequently translated into a number of subroutines and functions for Pass 2.

With respect to the doping profile and the physical models, it should be pointed out that the user is responsible for supplying several subroutines in accordance with required data. The coordinates of a point inside the described simulation area are supplied to the

subroutine for the doping profile, which has to return the net doping concentration ($N_D - N_A$) and the total impurity concentration ($N_D + N_A$) at this point. These values can be calculated analytically, eg. by an error function, or they can be derived from the output of a process simulator. For time dependent calculations the user has to supply a subroutine which gives the actual bias for a given time and boundary. The physical models for the carrier mobilities and the generation - recombination rate are designed as functions with several input parameters: the coordinates of the point where the mobility is calculated (this allows for surface or substrate effects), the carrier and impurity concentrations (to define the respective scattering processes), the x- and y-components of the electric field and the current densities (to take into account velocity saturation in the mobility model and avalanche generation in the generation model).

Additionally the user has the possibility to write a function for the intrinsic concentration n_i. The input parameters are the coordinates of a point inside the simulation area and the donor- and acceptor-concentrations.

In pass 2 the solution of the semiconductor equations in the described area has to be achieved. The subroutines written by Pass 1 together with the user supplied subroutines and functions are the only input for Pass 2. The discretization is done by the "Finite Boxes" - method. /1/. At first a relatively coarse grid is set up automatically for the inital guess, and during calculation it is refined by equidistributing the local truncation error of the PDE system. The generated output yields the resulting current values and the internal distributions chosen by the print card on the input-deck. To restart the calculation or to continue the calculation with a time dependent investigation binary files are provided which contain information about the grid, the values of the electrical potential and the carrier concentrations, and some internal scaling factors. Those binary files together with the user supplied routines and the routines written in Pass 1 are the input of the "Post-Processor" Pass 3 where the user can recalculate any internal distribution for the purpose of printing and plotting.

SIPMOS transistor - calculated results

Before discussing results it is necessary to describe a SIPMOS transistor /2/, /3/, particularly, the simulation area and the doping profile: A SIPMOS transistor chip consists of several thousands of cells (Fig.1) with a common drain region (bulk of the chip). The source and gate contacts on top of the chip are separated by a field oxide. It is only necessary to simulate half a cell because of the periodic structure of the cells as shown in Fig. 2. The boundary conditions of the simulation area are either Dirichlet conditions - for the source, drain and gate contacts on top and bottom of the cell - or Neumann conditions - for the left and right edges of the cell and the free oxide surface between source and gate. The following terms will be adopted in the text: the component of the electric field or the current densities parallel to the $SiSiO_2$ - interface is called the lateral component whereas the component perpendicular to the interface is called the transverse component. Fig. 2 is a schematic plot of the p- and n-doped areas: the very shallow n^+ source diffusion, the double diffused p area, the n^- epitaxial layer and the n^+ substrate. The doping profile is shown in Fig. 3; it is calculated with SUPREM /4/ in one dimension (different runs for the 3 areas) and extended analytically to two dimensions. Fig. 4 shows the calculated IV-characteristics: the characteristics for gate voltages UG = 6V and UG = 10V were investigated more precisely. Considering the shape of these curves a characteristic can be divided into three different regimes: The first region is the resistance region, characterized by a drain current increase coinciding with a drain voltage increase. This part extends approximately towards a bias point where UD = UG. The characteristic parameter is the on-resistance for which a value of 0.16 Ohm is calculated. Measurements of actual devices show the same result.

The next part of the IV-characteristic - the saturation region - is described by a constant current value in spite of an increasing drain voltage. By comparing simulations in this region with experimentally obtained curves a significant difference at higher gate voltages (UG > 8V) is observed. The measurements show a decreasing current value, if the drain voltage is increased: looking at the internal distributions, especially at the electron concentrations (Figs. 5-7) which will be done later, it can be concluded that this has to be a thermal effect.

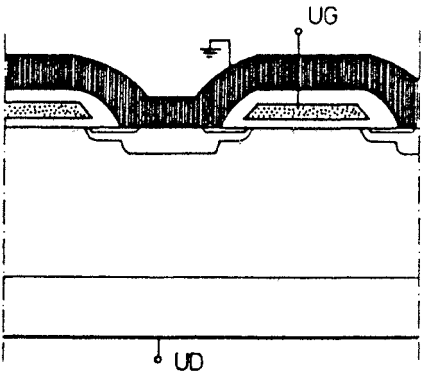


Fig 1: Unit Cell Structure of a SIPMOS Transistor.

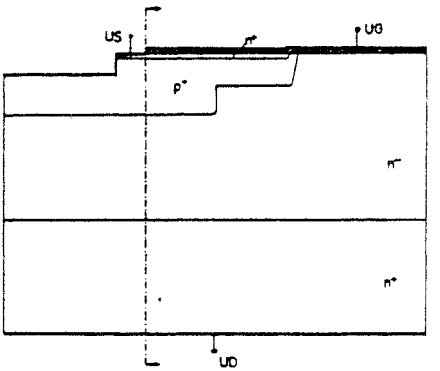


Fig 2: Simulation Geometry for a SIPMOS Transistor.

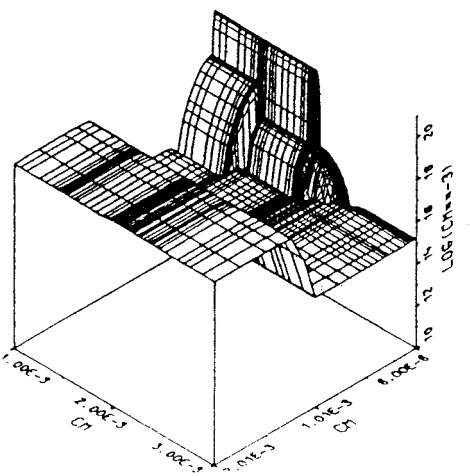


Fig 3: Doping Profile of a SIPMOS Transistor.

The heat flow equation is not solved and, therefore, this effect of a negative differential resistance can not be seen in the simulations. This aspect is the only notable difference between the calculations and the experiment.

The third part of the IV-characteristic is characterized by an increase of the drain current at very high drain voltages. It is the carrier multiplication and breakdown region where carriers are generated resulting in an additional hole current due to impact ionization. The advantage of a simulation in this range of the IV-characteristic is obvious: measurements are impossible due to thermal destruction of the device whereas calculations can be utilized for an optimum design.

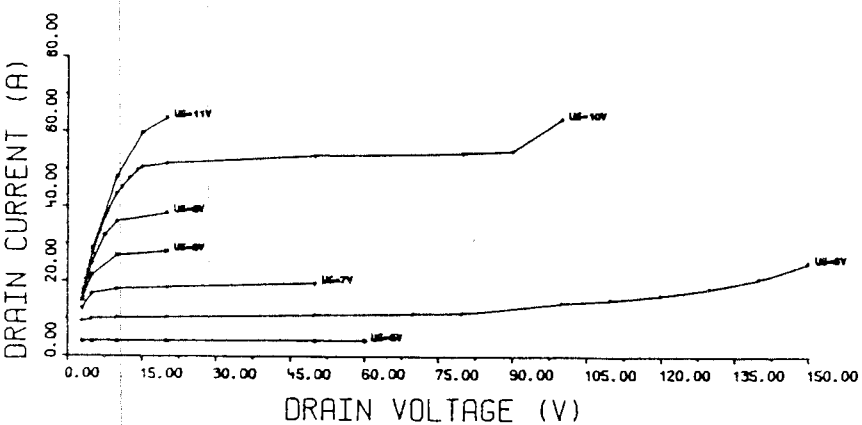


Fig 4: Calculated IV-Characteristic for the investigated Power Transistor.

Finally we present internal distributions for the three parts of the IV-characteristic at a gate voltage UG = 10V. For the resistance region the bias point UD = 3V is analyzed, in the saturation region UD = 20V, and in the carrier multiplication region UD = 100V are considered. The physical parameters are taken from /5/. Figs. 5-7 show the electron distributions: in the resistance region (Fig. 5) an accumulation layer underneath the whole gate contact can clearly be observed. This accumulation is removed by a space charge region spreading out from the centre of the gate contact at higher drain voltages (Fig. 6). The space charge around the p-base is also in-

creased. The electrons are squeezed into a very narrow band from the channel through the epilayer. In this layer the electron concentration equals the doping concentration, but in the carrier multiplication region it exceeds this level (Fig. 7). The space charge region around the p-area is increased enormously and extends towards the n^+ substrate.

The electric field and current components are plotted quasi logarithmically using transformation (1):

$$z = \text{sign}(a) * \log(1 + a/10^n) \qquad (1)$$

The transverse component of the electric field (Figs. 8-10) will be investigated first at the $SiSiO_2$ - interface and afterwards in the epilayer. A considerable large value is observed at the interface due to the high electric field in the oxide, as well as to the expansion of the space charge area. In the resistance region (Fig. 8) a homogenous field distribution is formed, which corresponds to the accumulation of electrons. For larger drain voltages however, (Figs. 9,10), the component changes its sign from a large positive value in the channel to a large negative value under the centre of the gate contact. In the n^+ substrate the potential is shorted. In the n^- epilayer the electric field has a small negative value which increases if there is a space charge. This space charge region is notably larger at higher drain voltages. The lateral electric field components (Figs. 11-13) reflect the spreading of the electric field around the p-zone space charge region as well as around the gate space charge region. The negative peak in the n^+ source region results from a doping step which is technologically caused. The electrons flow with saturation velocity from the channel through a narrow path in the epilayer towards the n^+ substrate. The transverse electron current density components (Figs. 14-16) demonstrate clearly the squeezing of the electron concentration. At UD = 3V (Fig. 14) they flow homogeneously from the accumulation zone to the n^- epilayer. In the saturation region (Fig. 15) the accumulation terminates shortly after the channel. The small area of a large positive component characterizes the end of the n^+ source region where the electrons are squeezed in order to pass through the channel. The lateral electron current density components (Figs. 17-19) demonstrate the current flux from the source contact through the n^+ source region and the channel. They

then move parallel to the interface - relatively far in the resistance region (Fig. 17) and only a short distance at higher drain voltages (Figs. 18,19) - until they turn into the epilayer where they spread around the space charge region. The modulus of the electron current density (Figs. 20-22) again shows the electron path for the three bias points.

Regarding the hole concentrations at low drain voltages the positively charged carriers are kept in the double diffused p zone, but at avalanche conditions (Fig. 23) an area of excess holes in the n^- epilayer and underneath the $SiSiO_2$ - interface is observed. The carriers are not generated directly at the interface but at a distance of 1 um underneath as also demonstrated by the generation - recombination rate (Fig. 24). The holes flow directly towards the interface as well as to the p-zone from the point of maximum generation, where they are exhausted by the shortage of the source contact resulting in a lateral hole current component. The fraction of holes at the interface either recombines or passes parallel to the interface also towards the p-zone.

Conclusion

The 2-D semiconductor simulation system BAMBI has been presented. The features of BAMBI - the generality of device geometries and physical parameter models - have been described. It is possible to simulate various kinds of devices. The user is requested to only describe the simulation area as simply as possible and to supply the external subroutines. Discretization and solution are done automatically. BAMBI has been successfully applied to the simulation of SIPMOS transistors. The calculated IV-characteristics are compared to measured data and differences are explained. A discussion of the internal distributions improves the understanding of the physical mechanisms. The results help to optimize the design of such transistors with regard to blocking voltage and on-resistance.

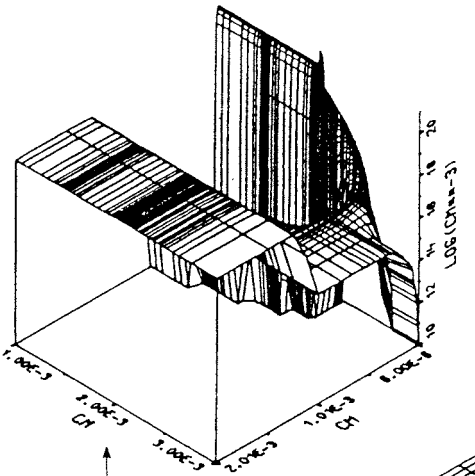
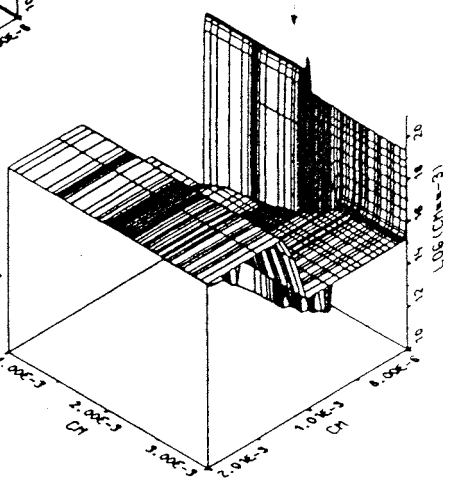


Fig 5: Electron Concentration at UD=3V,UG=10V.

Fig 6: Electron Concentration at UD=20V, UG=10V.



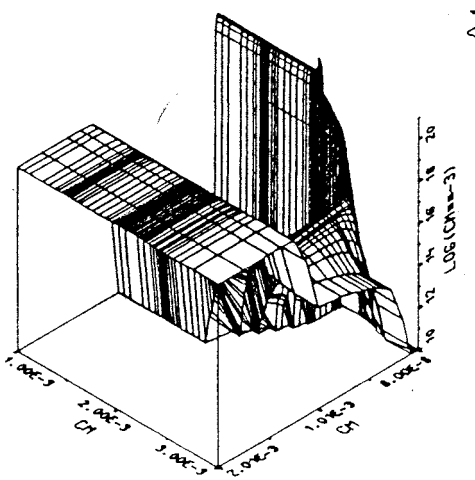


Fig 7: Electron concentration at UD=100V, UG=10V.

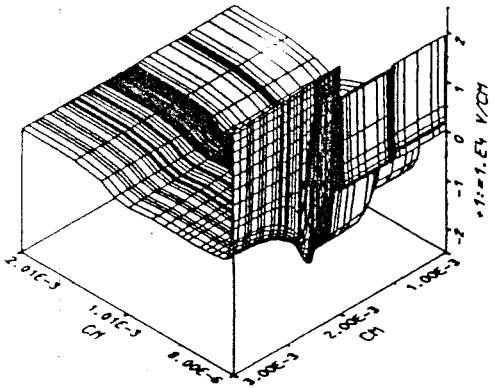
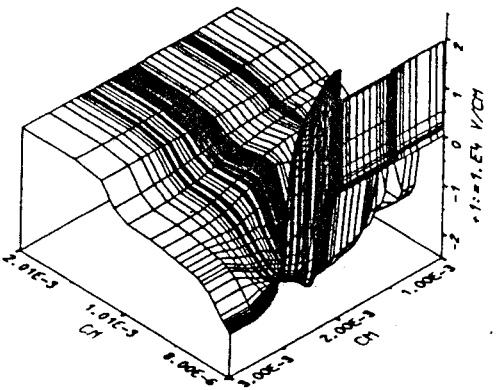


Fig 8: Transverse Electric Field Component at UD=3V, UG=10V.

Fig 9: Transverse Electric Field Component at UD=20V, UG=10V.



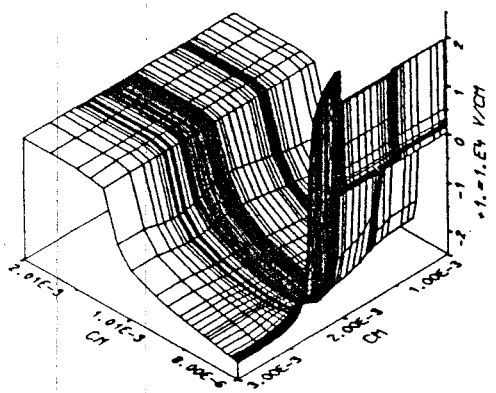


Fig 10: Transverse Electric Field Component at UD=100V, UG=10V

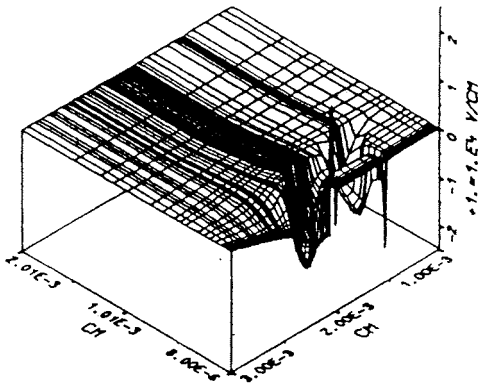
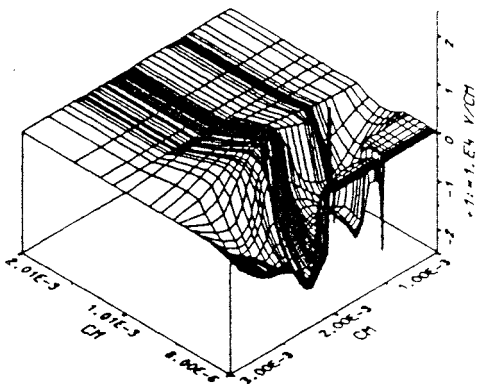


Fig 11: Lateral Electric Field Component at UD=3V, UG=10V.

Fig 12: Lateral Electric Field Component at UD=20V, UG=10V.



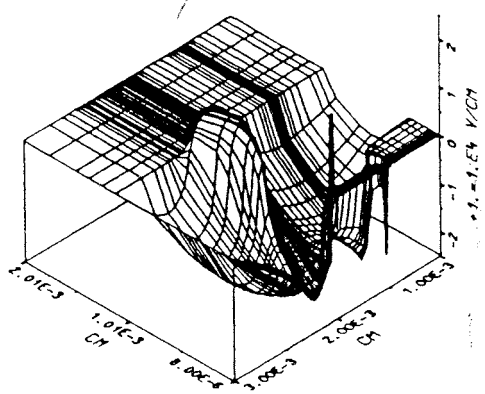


Fig 13: Lateral Electric Field Component at UD=100V, UG=10V.

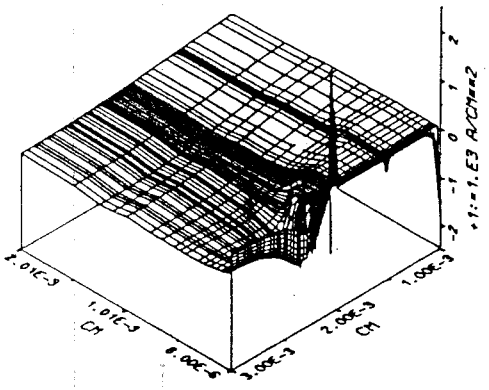
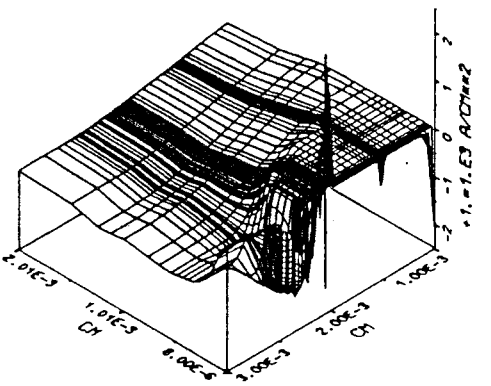


Fig 14: Transverse Electron Current Density Component at UD=3V, UG=10V.

Fig 15: Transverse Electron Current Density Component at UD=20V, UG=10V.



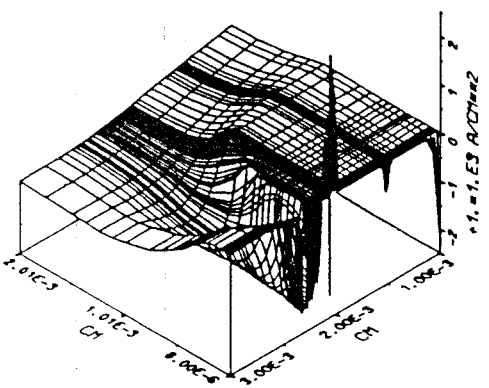


Fig 16: Transverse Electron Current Density Component at UD=100V, UG=10V.

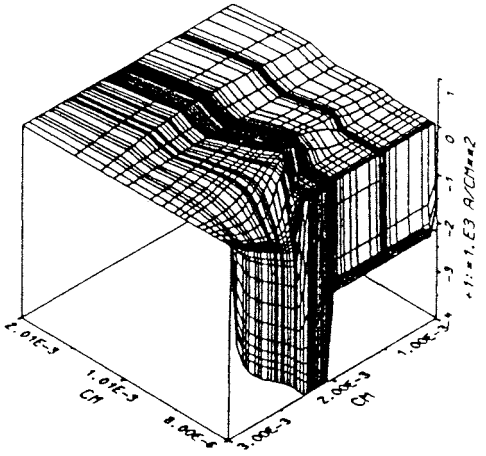


Fig 17: Lateral Electron Current Density Component at UD=3V, UG=10V.

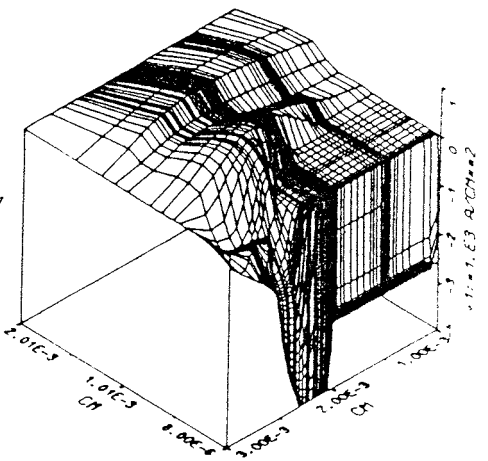


Fig 18: Lateral Electron Current Density Component at UD=20V, UG=10V.

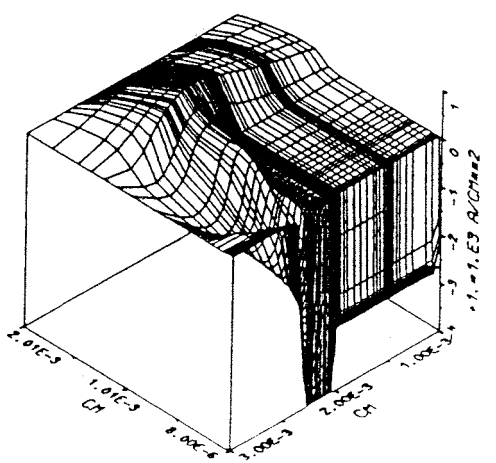


Fig 19: Lateral Electron Current Density component at UD=100V, UG=10V.

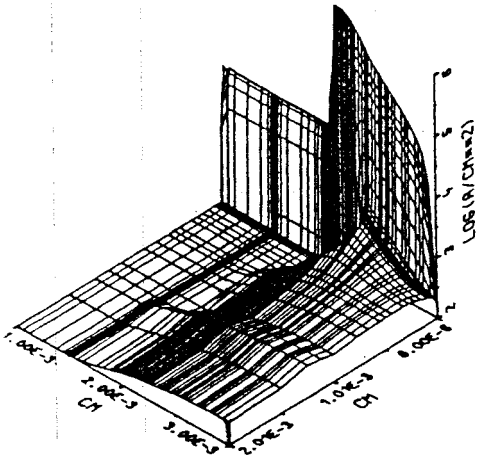


Fig 20: Modulus of the Electron Current Density at UD=3V, UG=10V.

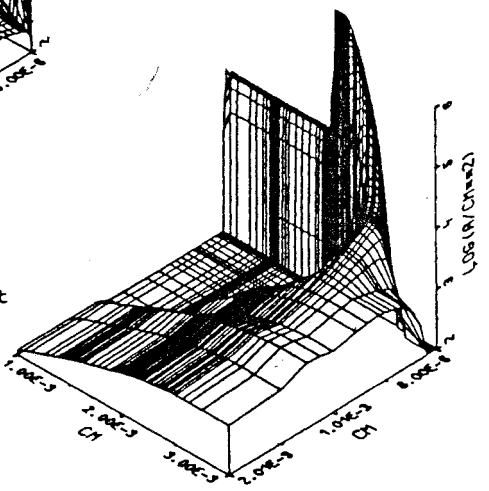


Fig 21: Modulus of the Electron Current Density at UD=20V, UG=10V.

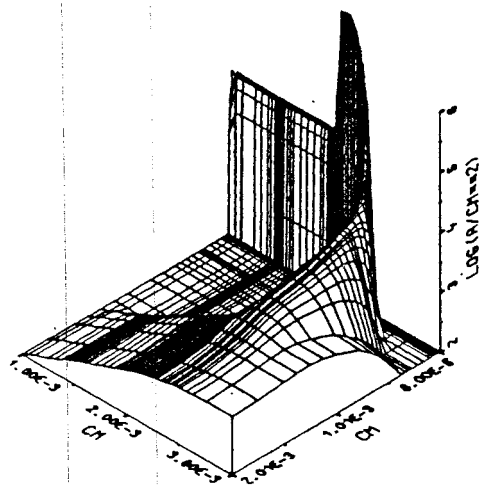


Fig 22: Modulus of the electron Current Density at UD=100V, UG=10V.

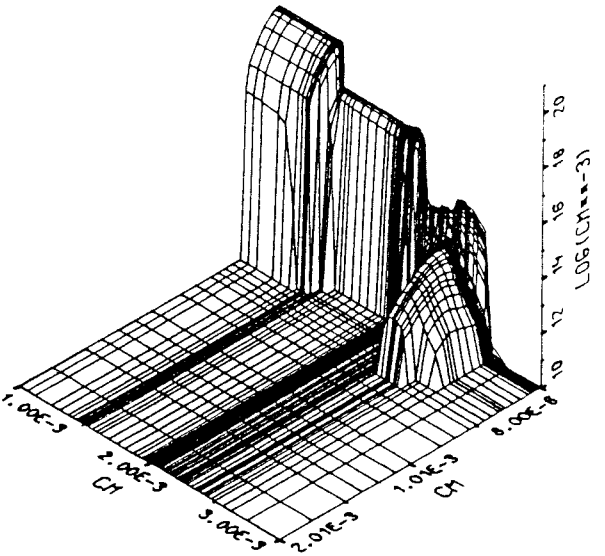


Fig 23: Hole Concentration at UD=100V, UG=10V.

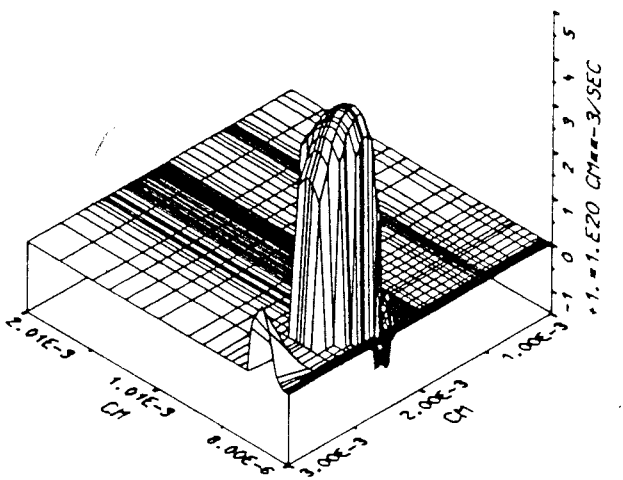


Fig 24: Generation - Recombination Rate at UD=100V, UG=10V.

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