BAMBI - A DESIGN MODEL FOR POWER MOSFET'S

A.F.Franz, G.A.Franz, S.Selberherr
Institut für Allgemeine Elektrotechnik und Elektronik
Abt. Physikalische Elektronik
TU Wien, Gußhausstraße 27, A-1040 Vienna, AUSTRIA

Abstract : The program system BAMBI is presented and applied to the simulation of power MOSFETs. Calculated output characteristics including the resistance, saturation and carrier multiplication region are discussed with special emphasis on the avalanche generation process.

Introduction

The area of applications for power MOSFETs has steadily increased in spite of the fact that these devices appeared on the market only few years ago. The broadening of application requires not only to measure the devices but also to simulate their performance with numerical tools. To help tackling this problem, the program-system BAMBI (=Basic Analyzer of MOS and BIpolar devices) has been developed. /1/. It has been successfully applied to simulations of power MOS transistors. Typical results are presented in this paper: not only the resistance and the saturation region are investigated, but also a detailed examination of the carrier multiplication region has been performed. Such calculations are very helpful for the design of the devices, because it is not possible to measure avalanche generation directly.

BAMBI - The Numerical Tool

The 2-d program system has been implemented using new simulation techniques /2/ in view of the extreme operating points in power devices (high current densities and large voltages). The major advantages are the possibilities to calculate arbitrarily shaped device geometries and the definition of mobility- and generation-recombination-functions as external subroutines which can be supplied by the user. These subroutines are provided with input parameters and are to deliver the mobility-, recombination-, doping- and intrinsic number-values either from an analytical function or interpolated data points. The device geometries are described by polygons in an input deck. The initial grid is set up and adapted automatically towards a final grid that matches the criterion of an equidistributed local discretization error. BAMBI solves all three semiconductor equations simultaneously using a modified Newton scheme.

SIPMOS - Results

As a typical example of a power MOS transistor, a SIPMOS structure /3/ has been investigated. Its simulation geometry is pictured in Fig. 1. Fig. 2 shows the calculated output characteristics for a 100V-SIPMOS transistor. Comparing these results to experimental data it is remarkable that for gate voltages UG $\geq$ 10V the measured curves exhibit a slightly negative slope at drain voltages greater than the gate bias. Obviously the calculations do not represent such an effect. Thereby, it can be concluded that the small electron path is heated locally due to high electron current densities and so the flux is decreased because of the negative temperature coefficient of the current in MOS devices.

The IV-characteristic features three different regions which have been investigated in detail. The series of the magnitude of the electron current density (Fig. 3) demonstrates the three regimes: resistance, saturation and carrier multiplication region at a gate voltage UG = 10V and drain voltages UD = 3V,20V and 100V, respectively. In the resistance region an electron accumulation layer exists at the interface and therefore a large lateral current component can be observed. The electrons are injected by the n^+ source, pass the channel and, together with those coming from the accumulation layer, flow in a broad path throughout the n^- epilayer towards the n^+ substrate. However, in the saturation region the space charge region around the p^+ zone enlarges and another one is built up underneath the middle of the gate contact. Therefore the electrons are squeezed in the upper part of the n^- epilayer. Stepping up the IV-characteristic the spreading takes place more and more in the bulk until the space charge regions have covered all of the epilayer. Such bias points lay in the carrier multiplication region. The current density in the epilayer increases rapidly due to impact ionization, the spreading of the electron current flux is immediately in front of the substrate.

A detailed analysis of the carrier multiplication regime has been performed at a gate voltage UG = 6V. The plots of Fig. 4 show a series (logarithmic scale) of hole densities (cf. detail a in Fig. 1) for three different drain voltages (UD = 50V,100V, and 160V). The hole density at UD = 50V references the region where no carrier multiplication takes place. Impact ionization starts at about UD = 70V. However, this effect can only be seen regarding the internal hole distribution, whereas the total current value is equal to the electron current value. The situation changes at UD = 100V where the hole current value is about 15% of the total current value. This quota increases rapidly and reaches more than 30% at UD = 160V. At this bias point a hole inversion layer can be observed at the interface. It should be noted that the maximum of the hole concentration is situated at the interface in the n-doped region about 2um away from the end of the p-doped channel. This phenomenon can only be explained by examining the impact-ionization-rate (Fig. 5: UG = 6V, UD = 160V). The value of the generation rate is described by $z = \mathrm{sign}(a)*\log(1+a/10^{19})$ which means that $1 \triangleq 10^{20}\ cm^{-3}/s$. The maximum of avalanche generation is observed not at the

interface but 1.6um underneath, in the epi-layer. Looking at the magnitude of the hole current density (Fig. 6) one can see that a small part of the generated holes flows directly towards the interface because of the potential drop (large transverse current component) where an accumulation layer is built. However, the majority of holes flows towards the p^+ region (large transverse and lateral current component resulting in a diagonal flow). There they pass the p^+ region, resulting in a lateral holes flux, and are then collected by the p-sided shorting of the source contact.

The series of Fig. 4 also shows the increase of the avalanche area with increasing drain voltage. At a drain voltage UD = 160V the current has more than doubled and the device is burnt out (UI-product P = 5kW!). Thereby, the SOAR can be determined without destructive tests and the design can be improved.

Conclusion

We have described the MOS features of the program system BAMBI and outlined its advantages (large flexibility concerning device geometry and physical parameter models). Some results of a SIPMOS transistor have shown the application of BAMBI to rather complex structures. Describing the internal distributions of the three different IV-characteristic regions and looking at these quantities in case of avalanche generation, the designer of such devices gets a good insight into the physical phenomena.

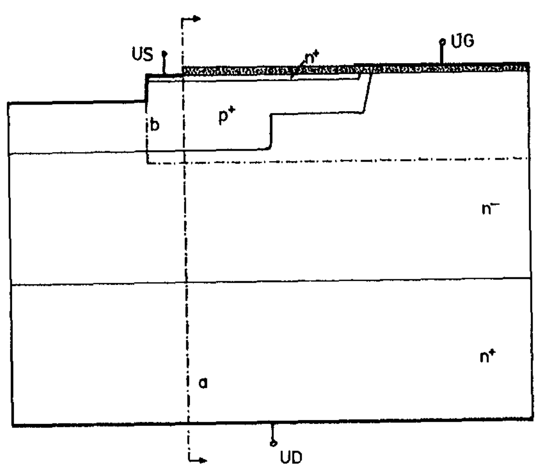


Fig. 1: Simulation Geometry.

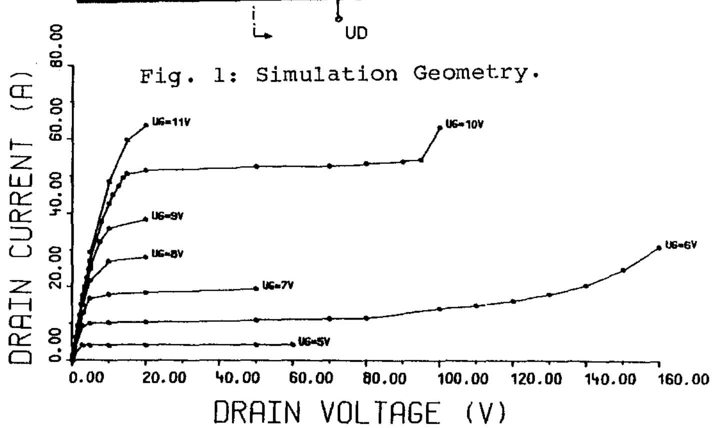


Fig. 2: Output Characteristics for a 100V SIPMOS Transistor.

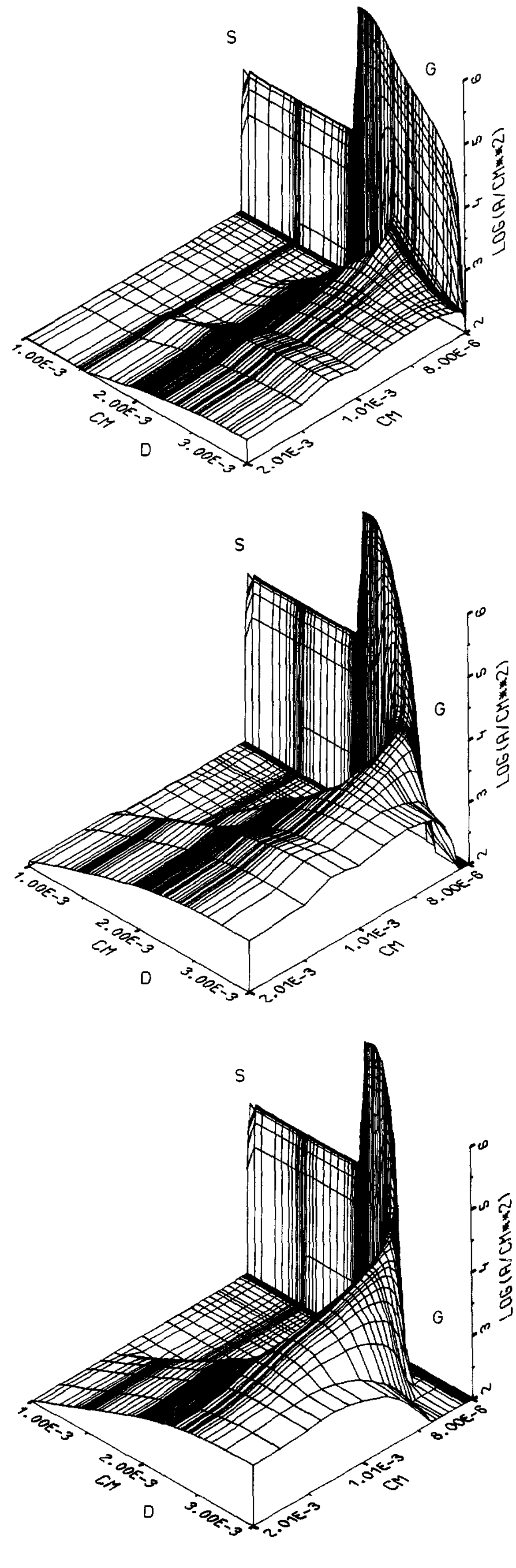
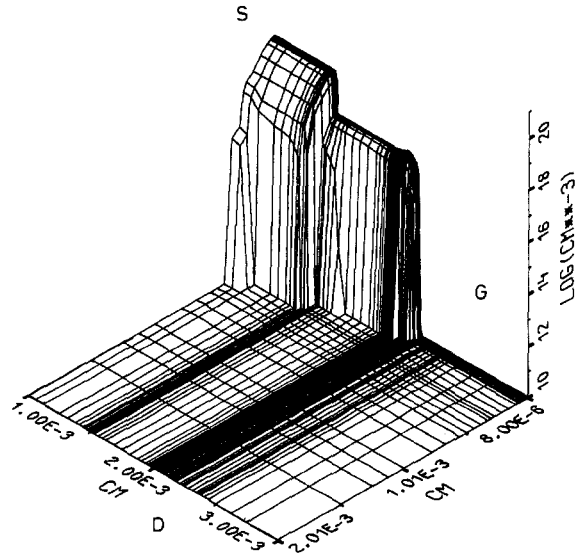
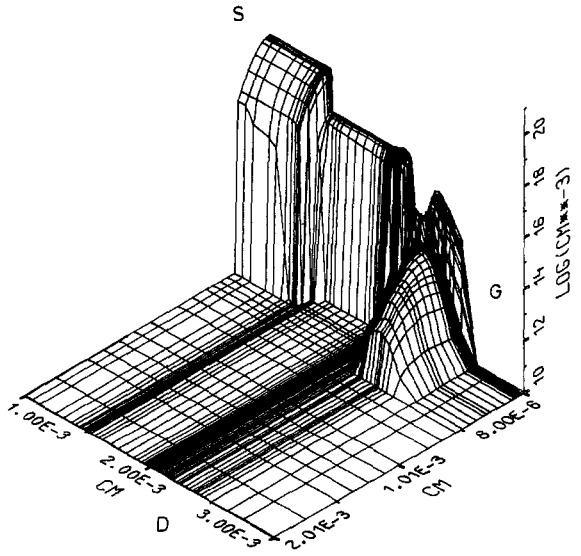


Fig. 3: Magnitude of Electron Current Density for UG=10V and UD=3V,20V and 100V.





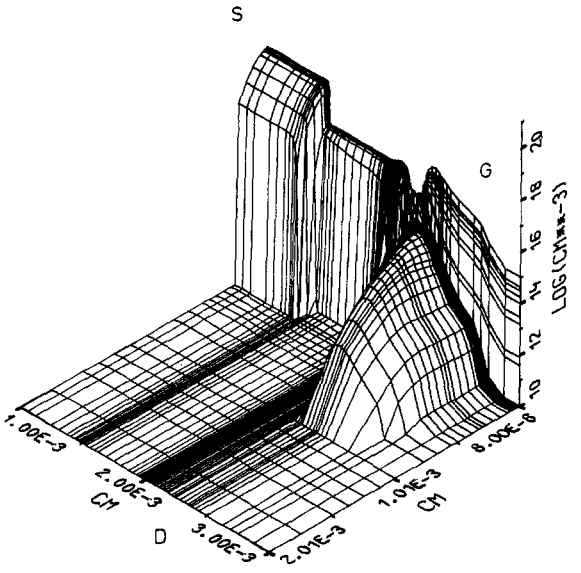


Fig. 4: Hole Concentration for UG=6V and UD=50V,100V and 160V.

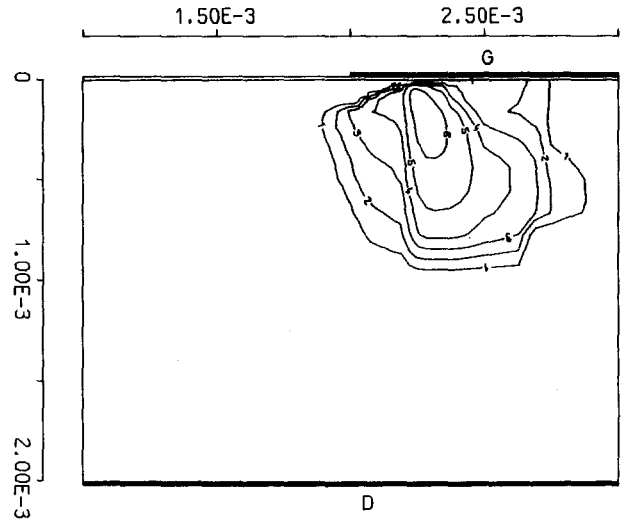


Fig. 5: Generation-Recombination Rate for UG=6V, UD=160V.

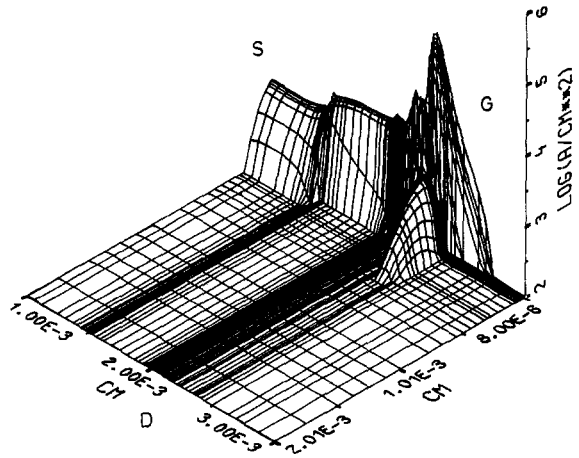


Fig. 6: Magnitude of the Hole Current Density for UG=6V, UD=160V.

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