COMPUTATION OF WIRE AND JUNCTION CAPACITANCE

IN VLSI STRUCTURES

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ABSTRACT

A method for the two-dimensional computation of metallization and junction capacitances in multiconductor systems is presented. The charge distribution on the conductor surface and in the space charge regions is computed with a computer program using the finite element method with triangular elements. The initial grid is automatically refined. During the refinement process no angle smaller than a prescribed lower bound is generated. A postprocessor computes the coefficients of capacitance from the potential distribution. The program handles a variety of VLSI structures. Specific numerical examples are presented to show applications of the concept.

1.) Introduction

The scaling theory of MOS transistors is the key to VLSI chip manufacturing. However, the progressive shrinking of the device dimensions creates a number of problems for circuit designers. A careful consideration of capacitance related phenomena like circuit delays and crosstalk signals is necessary to ensure a successful chip layout. Due to the lack of space we can only refer the interested reader to /1,2/ for a detailed analysis of VLSI layout problems.

The capacitance computation as outlined in this paper is a two stage procedure. The final step, the computation of coefficients of capacitance from conductor charges, is described in chapter 2). The preliminary step of charge computation is explained in chapter 3). Examples in chapter 4) close the presentation.

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2) Computation of Coefficients of Capacitance

The 3-conductor system of Fig.2-1 shall serve as an example for the following discussion. For the moment let us assume that all conductors are surrounded by a linear dielectric. The generalization to nonlinear media follows in paragraph 3.2). We define C_{ij} as the coupling capacitance between conductor i and conductor j, C_{ii} as the self capacitance of conductor i, Q_i and φ_i as the charge and potential of conductor i, respectively. The number of conductors is k. The set of equations (2.1) shows the relationship between the variables.

$$Q_{ij} = C_{ij}(\varphi_i - \varphi_j) \qquad (2.1a)$$

$$Q_i = \sum_{\substack{j=1 \\ j \neq i}}^{k} C_{ij}(\varphi_i - \varphi_j) + C_{ii}\varphi_i . \qquad (2.1b)$$

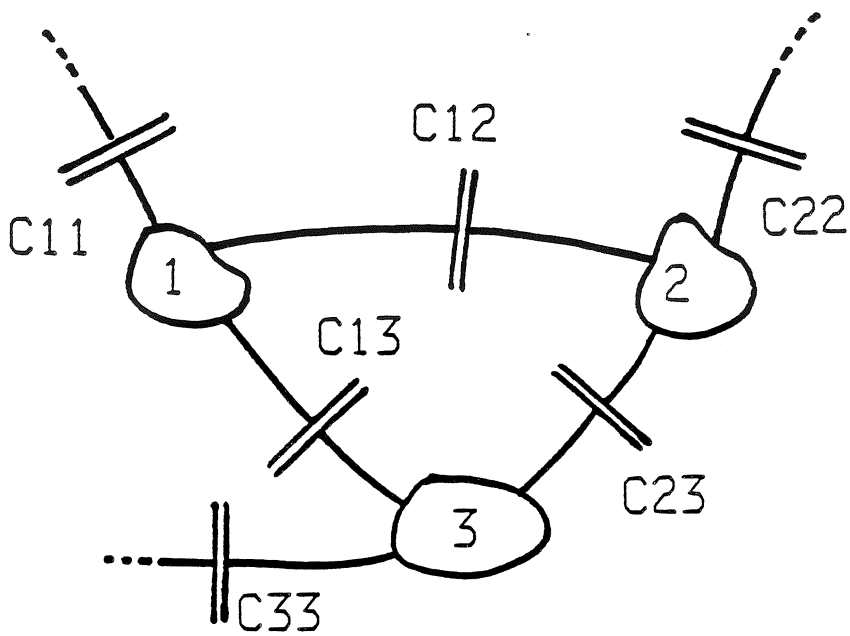


Fig.2-1 Three-Conductor System

The unknowns are the coefficients C_{ij}. Please note that solving (2.1b) is different from solving a system of linear equations $\mathbf{Ax} = \mathbf{b}$. For a certain bias point the number of unknowns is $k(k+1)/2$ but only $k-1$ linear independent equations exist. The conductor potentials are not necessary in the linear case because the capacitance depends purely on the geometry of conductors and dielectric interfaces. Therefore, we are allowed to simply assume some sets of conductor potentials in order to compute a charge

distribution Q until enough linear independent equations are available to match the number of unknowns. The determination of the charges is outlined in chapter 3).

2.1) Generalization for Nonlinear Dielectrics

The capacitance is no longer voltage independent. We are not allowed to simply assume a set of conductor voltages for the charge computation. Assert that the conductors are biased with the prescribed potentials φ_1, φ_2, φ_3. We employ the principle of linearization on the operating point of the circuit. The conductor potentials are replaced by the conductor bias plus the deliberately assumed potential offsets. Besides that, the method of the previous paragraph remain unchanged. The magnitude of the offset must be large enough to get a significant change in the charge and at the same time small enough to allow application of the linearization principle. A good 'rule of thumb' is to choose $\Delta\varphi$ = 1%...5% of the conductor bias.

3.) Computation of Surface and Space Charges

Again we consider first the presence of linear dielectrics only. To solve (2.1) for the C_{ij} we have to calculate the surface charges on the conductors. We solve the Laplace equation (3.1) in the two-dimensional simulation region which represents a cross cut of the interesting conductor geometry.

$$\text{div grad } \varphi = 0. \qquad (3.1)$$

The solution of (3.1) is the potential distribution $\varphi(x,y)$. By differentiation we get the electric field **E**. Integrating the normal component of the electrical displacement $\varepsilon \cdot \mathbf{E}$ over the conductor surfaces yields the charges.

Reflecting upon junction capacitances we have to solve Poisson's equation (3.2) instead of (3.1).

$$\text{div } \varepsilon \text{grad } \varphi = -q(n_i \exp((\Phi_p - \varphi)/V_T - n_i \exp((\varphi - \Phi_n)/V_T + C_T) \qquad (3.2)$$

q is the electron charge, n_i the intrinsic number, V_T the thermal voltage, ε the dielectric constant, Φ_n, Φ_p the quasifermipotential of the electrons and holes, respectively, and C_T the concentration of active dopants. Since, the junction capacitance we are interested in exists only in reverse biased junctions, an accurate model of the reversed biased pn-junction alone is sufficient for our purposes. We modify the right hand side of (3.2) by the use

of a depletion approximation (3.3a,b). Minority carriers are neglected. Φ_n and Φ_p are set to the constant anode and cathode potential of the junction, respectively.

Anode region:

$$\mathrm{div}\ \varepsilon \mathrm{grad}\ \varphi = -q(n_i \exp(\varphi_A) \cdot \exp(-\varphi/V_T) + C_T) \qquad (3.3a)$$

Cathode region:

$$\mathrm{div}\ \varepsilon \mathrm{grad}\ \varphi = q(n_i \exp(-\varphi_K) \cdot \exp(\varphi/V_T) + C_T) \qquad (3.3b)$$

After (3.3) has been solved it's right hand side which physically corresponds to the space charge density is integrated for the anode and cathode region separately. Due to the charge neutrality theorem the same amount of charge must be located in the anode and cathode, respectively. The satisfaction of charge neutrality can be used to reject inaccurate solutions.

Surface and space charges computed in the described manner are entered into equation (2.1b).

3.1) Solving the Partial Differential Equation

The finite element method is used to solve (3.1) or (3.3). A computer program has been developed that uses triangular elements with biquadratic shape functions. The program can be adapted to a wide variety of simulation geometries due to the easy handling of complicated boundaries with finite elements. The user specifies an initial grid coarse enough to describe the simulation region. The doping profile and the bias of the circuit complete the input data. The initial grid is automatically refined in the course of computation.

The selection of a well suited triangulation is essential for convergence and solution accuracy. As shown, e.g., in /3/ the discretization error depends on the smallest angle in the triangulation. To decrease this error it is <u>not</u> sufficient to simply increase the number of elements (triangles). At the same time one must assure that the element angles are all greater than a lower bound δ. Our grid generator fulfills this reqirement. Practical values for δ are $15^o \ldots 25^o$. Furthermore, the magnitude of that single parameter δ controls the 'character' of the grid. A small δ results in a very progressive, economic grid. A more uniform, slowly varying grid is achieved with a large δ. We would like to recall the fact that an overly progressive grid can lead to a bad condition number of the stiffness matrix and therefore should be avoided.

4.) Results

4.1) Linear Capacitance

The simulation geometry is shown in Fig.4-1. The influence of the spacing S and the conductor-ground plane distance H on the capacitances C_S and C_C are investigated. H takes values from 0.1 to 1.2 μm and S is in the range from 0.2 to 2.4 μm.

A comparison between the numerically computed coupling capacitance and the classical parallel plate formula is shown in Fig.4-2. The dependent variable is C_C/C_{CO} with

$$C_{CO} = \varepsilon_O \cdot T/S \qquad (4.1)$$

The use of (4.1) is inadequate for an accurate circuit layout. The computed capacitance values are typically 50%...100% larger than (4.1) predicts.

4.2) Junction Capacitance

The second example is based on the structure shown in Fig.4-3 (not to scale). The length unit is μm. The polysilicon wire is isolated from the substrate and the aluminum by a layer of silicondioxide. The substrate, which is p-doped with $N_A=10^{16}$ cm^{-3}, contains an implanted n-region. The analytic doping profile model from /4/ is used with the following assumptions: A dose of 10^{15} (phosphorus) is implanted through a 350nm thick protective oxide layer with an energy of 40keV. After the implant a 1200s annealing at 1000 °C is performed. The resulting profile is shown in Fig.4-4. A simplified first analysis of the structure usually treats the oxide/substrate interface as a conducting plane. The wires are assumed to be ideal conductors also. The capacitance is calculated to be 8.79pF/cm.

Simulating the full structure is much more costly. Three conductors will now be considered: the polysilicon wire, the p-region of the substrate and a 'compound' wire consisting of the aluminium contact plus the n-region. Fig.4-5 and Fig.4-6 show the potential distribution for two bias points. The gate potential is 3V, the bulk potential is -1V. The source potential is 1V in Fig.4-5 and 2V in Fig.4-6. The junction capacitance was evaluated to $C_{ju}(U_S=1V)=38.8pF/cm$ and $C_{ju}(U_S=2V)=32.8pF/cm$.

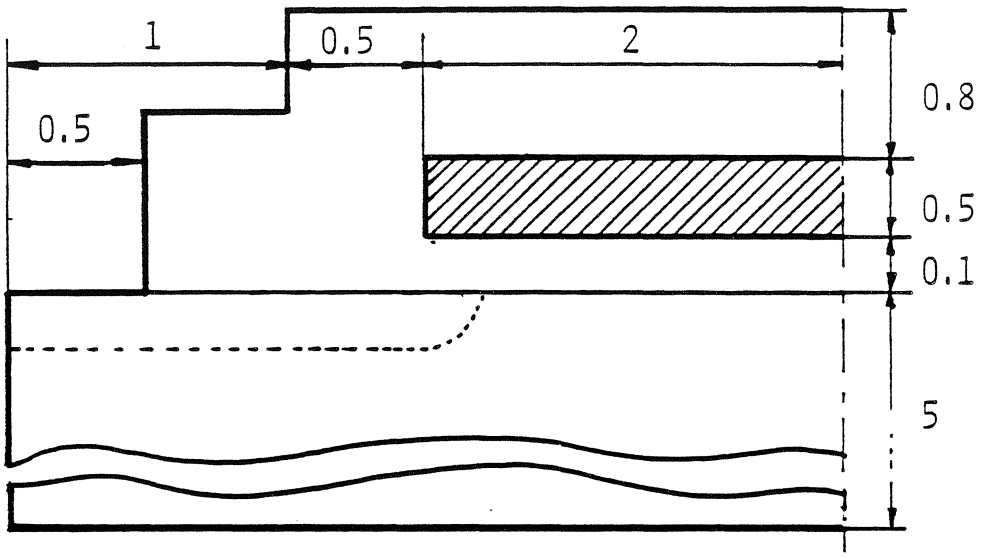


Fig.4-3 Simulation Geometry

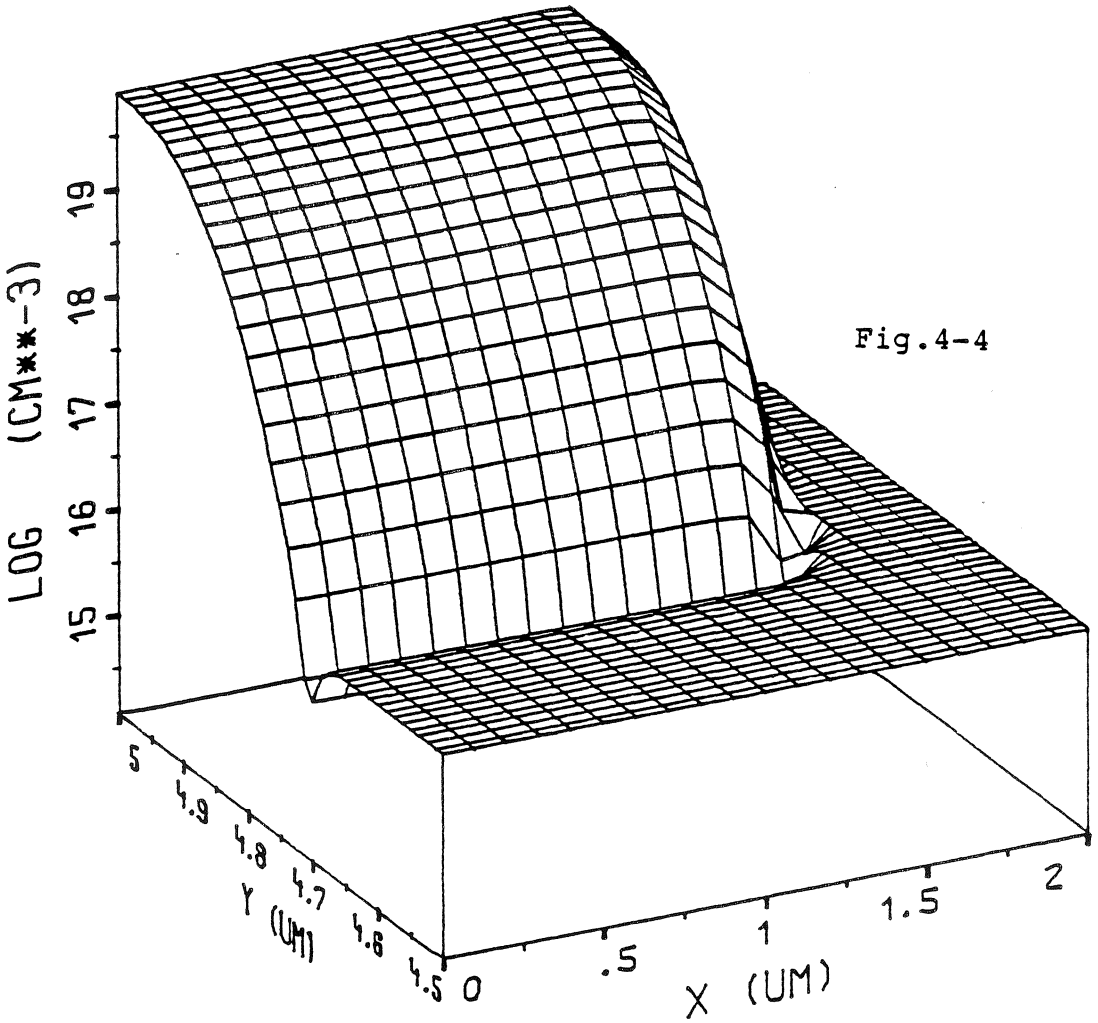


Fig.4-4

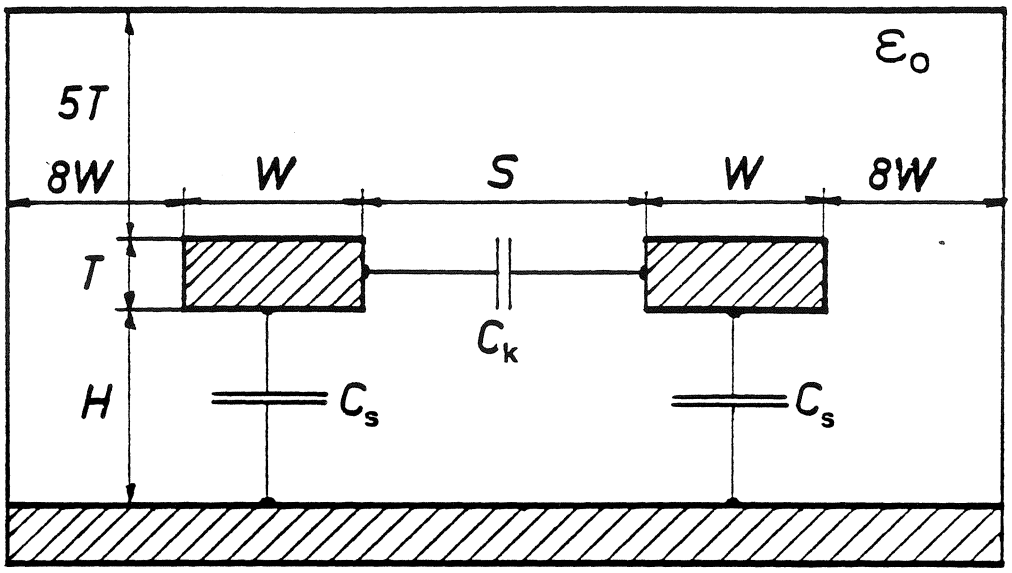


Fig.4-1 Simulation Geometry

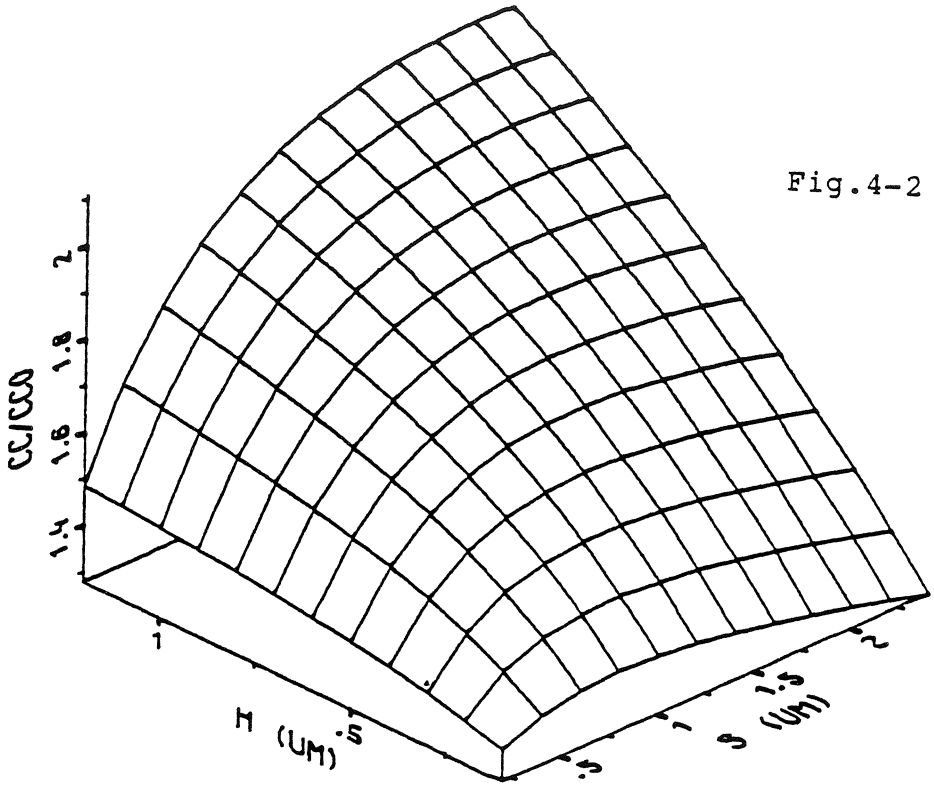
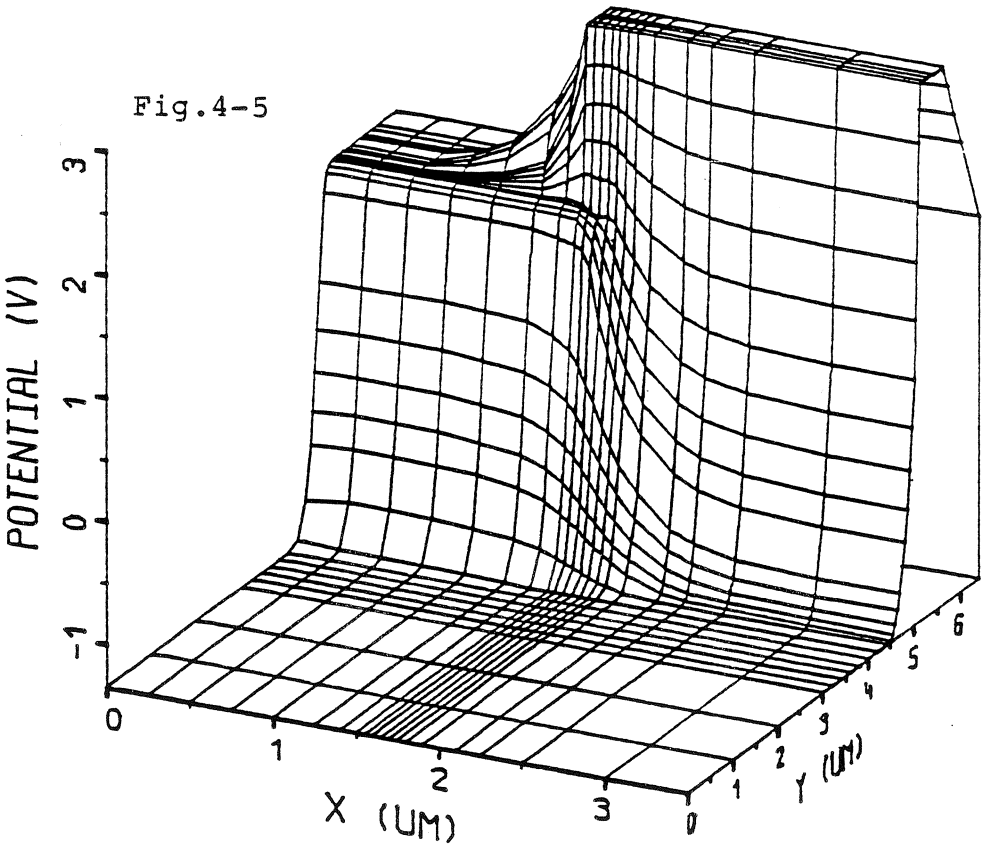


Fig.4-2

Fig.4-5


POTENTIAL (V)
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1
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X (UM)
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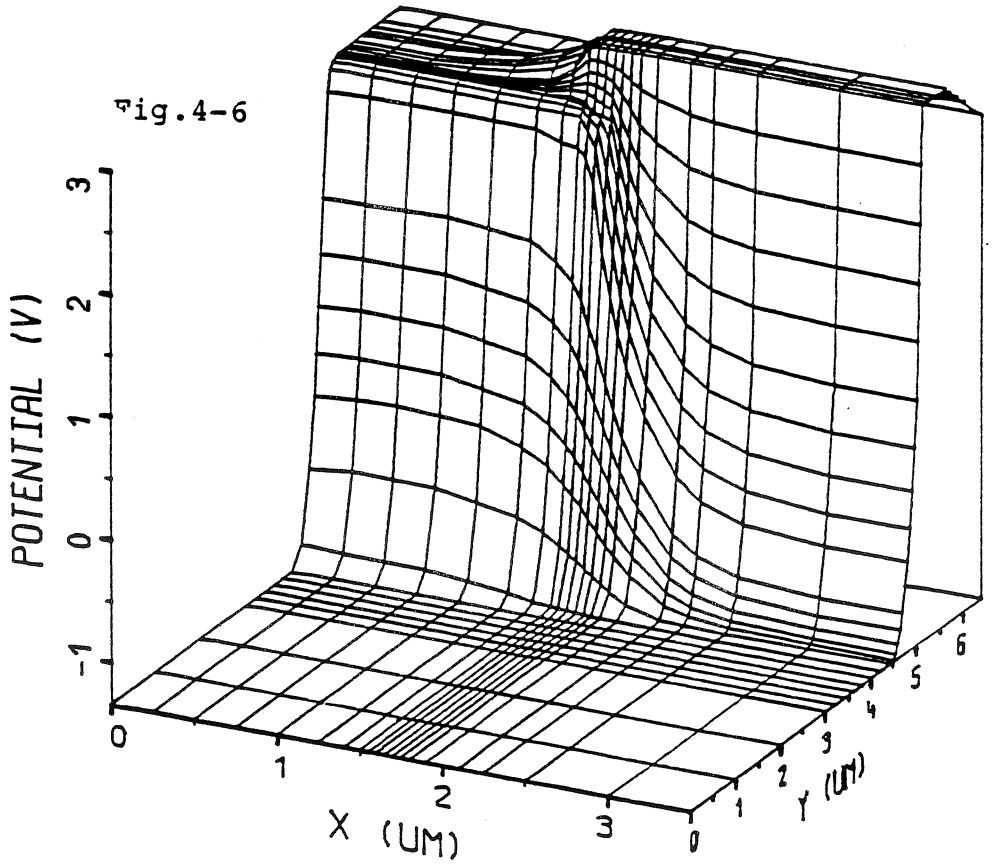
Y (UM)

Fig.4-6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5.) Conclusion

We have outlined the importance of accurate capacitance computation for the purpose of VLSI design. A method for the calculation of linear and nonlinear capacitances has been presented.

We presented a depletion approximation suitable for accurate computation of semiconductor junction capacitances. The coupling capacitance of a transmission line pair vs. line and line to ground spacing was shown in a pseudo 3D-plot. The junction capacitance of a VLSI-Structure has been computed.

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References

/1/ Hayes J.,
"MOS Scaling",
IEEE Computer, Jan. 1980, pp.8-13

/2/ Hodges D., Jackson H.,
"Analysis and Design of Digital Integrated Circuits",
McGraw-Hill, 1983, ISBN 0-07-029153-5

/3/ Strang G., Fix G. J.,
"An Analysis of the Finite Element Method",
Prentice Hall, 1973, ISBN 0-13-032946-0

/4/ Lee H.G., Dutton R.W.,
"Two Dimensional Low Concentration Boron Profiles: Modeling and Measurement",
IEEE, Transactions on Electron Devices, ED-28/10, 1981, pp.1136-1147