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COMPUTATION OF VLSI METALLIZATION CAPACITANCE

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ABSTRACT: A method for the two-dimensional computation of metallization and junction capacitances in multiconductor systems is presented. The charge distribution on the conductor surface and in the space charge regions is computed with a computer program using the finite element method with triangular elements. The initial grid is automatically refined. During the refinement process no angle smaller than a prescribed lower bound is generated. A postprocessor computes the coefficients of capacitance from the charge values. The program handles a variety of VLSI structures. Specific numerical examples are presented to show applications of the concept.

1.) Introduction

1.1) Organisation of the Paper

Chapter 1.) explains the motivation behind the present paper. Chapter 2.) gives a brief survey of relevant literature known by the authors. The capacitance computation as outlined in this paper is a two stage procedure. The preliminary step, the computation of surface and space charges, is described in chapter 4.). The final step, the capacitance computation, is explained in chapter 3.). Examples in chapter 5.) close the presentation.

1.2) Increasing Importance of Capacitances in VLSI

The scaling theory of MOS transistors is the key to VLSI chip manufacturing. However, the progressive shrinking of the device dimensions creates a number of problems for circuit

designers. As outlined below a careful consideration of wire layout, circuit delays and crosstalk problems is necessary to ensure a successful chip layout.

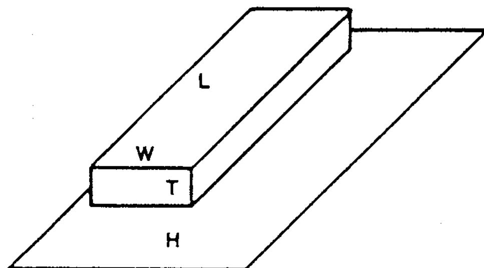

Fig.1-1 Interconnection line geometry

First we investigate how the capacitance of an interconnection line is affected if a scaling factor 1/K, K > 1, is applied to a design to reduce the vertical and horizontal dimensions. Assume the rectangular wire of Fig.1-1. A wire of width W, height H and length L is located above a conducting ground plane. Between the wire and the plane is an insulator of thickness H and relative dielectric constant ε_r. ρ is the specific resistance of the line material. By neglecting fringing effects the line capacitance (1.1a) and the line resistance (1.1b) become

$$C = \varepsilon_o \varepsilon_r WL/H \qquad (1.1a)$$

$$R = \rho L/(WT). \qquad (1.1b)$$

Using the scaling relations (1.2a-d)

$$H' = H/K \qquad (1.2a)$$
$$L' = L/K \qquad (1.2b)$$
$$T' = T/K \qquad (1.2c)$$
$$W' = W/K \qquad (1.2d)$$

the scaled capacitance (1.3) becomes

$$C' = \varepsilon_o \varepsilon_r W'L'/H' = C/K. \qquad (1.3)$$

A similar consideration of the line resistance reveals

$$R' = R \cdot K. \qquad (1.4)$$

We see from (1.3), (1.4) that the RC time constant of the line is not improved by scaling. So far our analysis has been

based on the assumption that designers will take the same circuit function and rebuild it on a smaller level. In practice they are more likely to place more components on the chip while maintaining it's area. With respect to the wiring that means the wire length is not scaled down provided that the chip architecture remains the same.

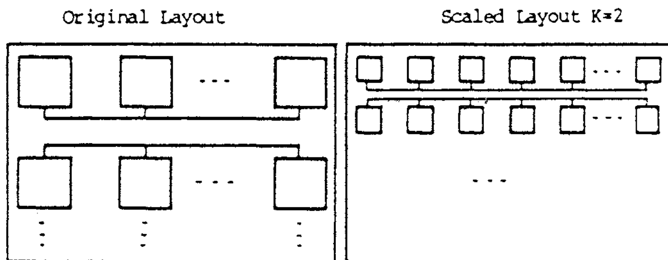

Fig.1-2

Fig.1-2 illustrates that the length of a line (i.e. a data bus) is conserved. Taking this into account (1.3) and (1.4) have to be modified and read now

$$C' = C \qquad (1.5)$$

$$R' = R \cdot K^2. \qquad (1.6)$$

The time constant is now scaled up by K^2 posing tight layout constraints if passive (parasitic) elements are not permitted to seriously degrade circuit performance. The maintainance of a suitable noise margin forces control of coupling capacitances between parallel and sometimes even crossing lines. Power requirements depend, in part, on the amount of capacitance at a gate output. For those reasons the precise knowledge of device and interconnect capacitances at the design phase of a chip is essential. For a more detailed analysis of VLSI layout problems the interested reader is referred to /2,7,10,5/.

2) Existing Work

The following is a brief survey over existing literature known by the authors and by no means intended to be exhaustive. A mathematical framework for the following problem is needed: For a given conductor geometry and a given region of interest (simulation region) compute the cofficients of capacitance for all conductors in the region. If the dielectric surrounding the conductors is nonlinear (i.e. semiconductor), then the conductor potentials must also be

given. For the linear case (i.e. silicondioxide as dielectric) bias point information is irrelevant. Two ways leading to a solution are widespread: 1) Problem formulation in integral equation (IEF) or 2) Problem formulation in partial differential equation (PDEF) form.

The first approach is favored in /1, 8, 9, 17, 11, 12, 13/. The difficulty of the IEF is the need for an analytical expression of Green's function for a particular simulation region. It is usually hard to obtain and mostly contains infinite sums which may lead to slow convergence. Furthermore a singularity of type $1/x$, $x \to 0$ is always present. This may be tackled by using weighted quadrature formulas as applied in /11,13/ to the IEF. Analytical integration of Green's function is shown in /1,17/. The IEF is good suited to the problem if Green's function is easy to calculate and the spacing between conductors is very large compared to the conductor dimensions. Using the IEF the electric field between the wires is not needed. (It is implicitly present in Green's function.) Only the field on the conductor surface is of interest. This poses an advantage if simulation regions are large or even infinite.

PDEF requires the solution of Poisson's equation for nonlinear dielectrics and Laplace's equation for linear dielectrics. Usually this is done by discretization of the simulation region with finite element or finite difference methods. Tutorial papers on the subject are /4,18/. Computer implementation of PDEF, generally speaking, is more laborious than IEF. The payoff is its easy adaption to various kinds of simulation geometries. Ideas to overcome the sensitivity of discretization methods to electric field singularities at conductor vertices are presented in /6/. /14,15/ contain an investigation of progressive grids for discretization.

3.) Computation of Coefficients of Capacitance

The 3-conductor system of Fig.3-1 shall serve as an example for the following discussion. For the time being let us assume that all conductors are surrounded by a linear dielectric. The generalization to nonlinear media follows in paragraph 3.2). First of all we define C_{ij} as the coupling capacitance between conductor i and conductor j, C_{ii} as the self capacitance of conductor i, Q_i and φ_i as the charge and potential of conductor i, respectively. The number of conductors is k. The set of equations (3.1) shows the relationship between the variables.

$$Q_{ij} = C_{ij}(\varphi_i - \varphi_j) \qquad (3.1a)$$

$$Q_i = \sum_{\substack{j=1 \\ j \neq i}}^{k} C_{ij}(\varphi_i - \varphi_j) + C_{ii}\varphi_i . \qquad (3.1b)$$

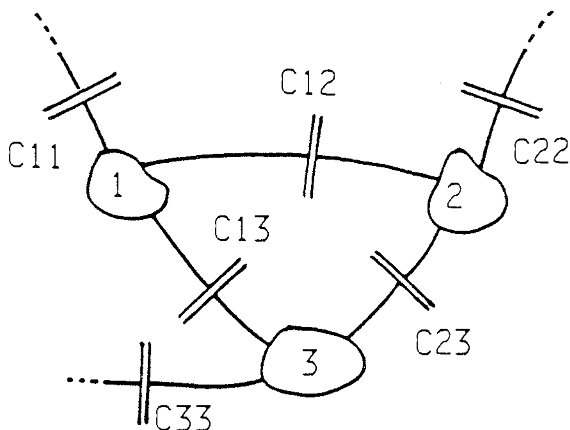

Fig.3-1 Three-Conductor System

The unknowns are the coefficients C_{ij}. Please note, that solving (3.1b) is different from solving a system of linear equations $Ax = b$. The number of unknowns is $k(k+1)/2$ but only $k-1$ linear independent equations exist. The charge distribution $Q = (Q_1, Q_2, \ldots , Q_k)$ depends on the conductor potentials and is assumed to be known. Chapter 4.) of the paper outlines how to get the charges. The conductor potentials are not necessary in the linear case because the capacitance depends purely on the geometry of conductors and dielectric interfaces. Therefore, we are allowed to simply assume some sets of conductor potentials in order to compute a charge distribution Q until enough linear independent equations are available to match the number of unknowns.

For numerical reasons we use k sets of potentials and setup k^2 system equations. Clearly not all of these k^2 equations are linearly independent. A computer algorithm can be employed to select those equations that result in the best possible condition number of the system coefficient matrix if more than the necessary $k(k+1)/2$ equations are available.

3.1) Three-Conductor Example

We assume a set of conductor potentials $S_1 = (\varphi_1 \neq 0,\ 0,\ 0)$ and compute the conductor charges ${}_1Q_1$, ${}_1Q_2$, ${}_1Q_3$. The prefix index refers to the set S_1. The following six relations hold true

$$Q_{12} = C_{12}\,\varphi_1 \qquad (3.2a)$$
$$Q_{13} = C_{13}\,\varphi_1 \qquad (3.2b)$$
$$Q_{23} = 0 \qquad (3.2c)$$
$$Q_{11} = C_{11}\,\varphi_1 \qquad (3.2d)$$
$$Q_{22} = 0 \qquad (3.2e)$$
$$Q_{33} = 0. \qquad (3.2f)$$

By summation of all contributions to the conductor surface charge one arrives at (3.3a-c)

$$Q_1 = \varphi_1\,(C_{11} + C_{12} + C_{13}) \qquad (3.3a)$$
$$Q_2 = -\varphi_1\,C_{12} \qquad (3.3b)$$
$$Q_3 = -\varphi_1\,C_{13}. \qquad (3.3c)$$

The procedure is repeated using $S_2 = (\varphi_1,\ \varphi_2,\ 0)$ which yields expressions (3.4a-f)

$$Q_{12} = C_{12}\,(\varphi_1 - \varphi_2) \qquad (3.4a)$$
$$Q_{13} = C_{13}\,\varphi_1 \qquad (3.4b)$$
$$Q_{23} = C_{23}\,\varphi_2 \qquad (3.4c)$$
$$Q_{11} = C_{11}\,\varphi_2 \qquad (3.4d)$$
$$Q_{22} = C_{22}\,\varphi_2 \qquad (3.4e)$$
$$Q_{33} = 0. \qquad (3.4f)$$

Equations (3.5a-c) give the surface charges on each conductor.

$$Q_1 = \varphi_1\,C_{11} + U_{12}\,C_{12} + \varphi_1\,C_{13} \qquad (3.5a)$$
$$Q_2 = -U_{12}\,C_{12} + \varphi_2\,C_{22} + \varphi_2\,C_{23} \qquad (3.5b)$$
$$Q_3 = -\varphi_1\,C_{13} - \varphi_2\,C_{23} \qquad (3.5c)$$

Another repetition of the cycle with $S_3 = (\varphi_1,\ \varphi_2,\ \varphi_3)$ yields two similar sets of equations not explicitly noted. Combining (3.3), (3.5) and the the result of the third cycle to matrix form yields an over-determined system of nine linear equations (3.6)

$$\mathbf{A}\mathbf{x} = \mathbf{b} \qquad (3.6)$$

with A the <u>rectangular</u> coefficient matrix, **x** the vector of unknown capacitances $\mathbf{x} = (C_{11}, C_{12}, \ldots, C_{33})$ and **b** the vector of the charges $\mathbf{b} = ({}_1Q_1, {}_1Q_2, \ldots, {}_3Q_3)$.

System 3.6 is transformed via QR-decomposition into equation (3.11). QR-decomposition is a generalization of the well-known Gaussian elimination /3/, section 11. (3.6) is solved in the sense that the L_2-norm of the residuum vector

$r = Ax - b$ is minimized. The linear least squares method, used for curve fitting, is a familiar application of QR-decomposition in two dimensions.

We start by substituting the singular value decomposition (3.7) of matrix A into (3.6). U and V are orthogonal matrices as indicated by (3.8). The resulting equation (3.9) is multiplied from the left by U^T and the vector y defined in (3.10) is introduced. Finally, equation (3.11) is arrived at and solved.

$$A = UQV^T \qquad (3.7)$$

$$U^T = U^{-1} \qquad (3.8a)$$
$$V^T = V^{-1} \qquad (3.8b)$$

$$UQV^T x = b \qquad (3.9)$$

$$y = V^T x \qquad (3.10)$$

$$Qy = U^T b = b^* \qquad (3.11)$$

The ratio of the largest element b_i^* of vector b^*, $i=1, k(k+1)/2$ to b_j^*, $j=k+1, k^2$, provides an a posteriori quality indicator. This figure describes the number of significant digits in the result not affected by roundoff and/or truncation error.

3.2) Generalization for Nonlinear Dielectrics

The capacitance is no longer voltage independent. We are not allowed to simply assume a set of conductor voltages for the charge computation. Assert that the conductors are biased with the prescribed potentials φ_1, φ_2, φ_3. We employ the principle of linearization on the operating point of the circuit. Instead of the conductor potentials we now assume potential offsets $S_1 = (\Delta\varphi_1, 0, 0)$, $S_2 = (\Delta\varphi_1, \Delta\varphi_2, 0)$ and $S_3 = (\Delta\varphi_1, \Delta\varphi_2, \Delta\varphi_3)$. The conductor potentials for the first cycle of the charge computations, yielding $_1Q_1$, $_1Q_2$ and $_1Q_3$, are $\varphi_1 + \Delta\varphi_1$, φ_2 and φ_3, for the second cycle $\varphi_1 + \Delta\varphi_1$, $\varphi_2 + \Delta\varphi_2$, φ_3, and so on. In the nonlinear case the conductor potentials are replaced by the conductor bias plus the deliberately assumed potential offsets. Besides that, the method of paragraph 3.1) remains unchanged. The magnitude of the offset must be large enough to get a significant change in the charge and at the same time small enough to allow application of the linearization principle. A good 'rule of thumb' is to choose $\Delta\varphi = 1\%...5\%$ of the conductor bias.

4.) Computation of Surface and Space Charges

Let us, again, firstly consider the presence of linear dielectrics only. To employ the method of paragraph 3.1) we have to calculate the surface charges on the conductors. We solve the Laplace equation (4.1) in the two-dimensional simulation region which represents a cross cut of the interesting conductor geometry.

$$\mathrm{div}\ \mathrm{grad}\ \varphi = 0. \qquad (4.1)$$

The solution of (4.1) is the potential distribution $\varphi(x,y)$. By differentiation we get the electric field $\mathbf{E}$. Integrating the normal component of the electrical displacement $\varepsilon \cdot \mathbf{E}$ over the conductor surfaces yields the charges.

Reflecting upon junction capacitances we have to solve Poisson's equation (4.2) instead of (4.1).

$$\mathrm{div}\ \varepsilon\,\mathrm{grad}\ \varphi = -q(n_i \exp((\Phi_p - \varphi)/V_T - n_i \exp((\varphi - \Phi_n)/V_T + C_T) \qquad (4.2)$$

q is the electron charge, n_i the intrinsic number, V_T the thermal voltage, ε the dielectric constant, Φ_n, Φ_p the quasifermipotential of the electrons and holes, respectively, and C_T the concentration of active dopants. Since, the junction capacitance we are interested in exists only in reverse biased junctions, an accurate model of the reversed biased pn-junction alone is sufficient for our purposes. We modify the right hand side of (4.2) by the use of a depletion approximation (4.3a,b). Minority carriers are neglected. Φ_n and Φ_p are set to the constant anode and cathode potential of the junction, respectively.

Anode region:

$$\mathrm{div}\ \varepsilon\,\mathrm{grad}\ \varphi = -q(n_i \exp(\varphi_A) \cdot \exp(-\varphi/V_T) + C_T) \qquad (4.3a)$$

Cathode region:

$$\mathrm{div}\ \varepsilon\,\mathrm{grad}\ \varphi = q(n_i \exp(-\varphi_K) \cdot \exp(\varphi/V_T) + C_T) \qquad (4.3b)$$

After (4.3) has been solved it's right hand side, which physically corresponds to the space charge density, is integrated for the anode and cathode region separately. Due to the charge neutrality theorem the same amount of charge must be located in the anode and cathode, respectively. The satisfaction of charge neutrality can be used to reject inaccurate solutions.

Surface and space charges computed in the described manner are entered into equation (3.3) and (3.5).

4.1) Solving the Partial Differential Equation

The finite element method is used to solve (4.1) or (4.3). A computer program has been developed that uses triangular elements with biquadratic shape functions. The program can be adapted to a wide variety of simulation geometries due to the easy handling of complicated boundaries with finite elements. The user specifies an initial grid coarse enough to describe the simulation region. The doping profile and the bias of the circuit complete the input data. The initial grid is automatically refined in the course of computation. The selection of a well suited triangulation is essential for convergence and solution accuracy.

The importance of sufficient small numerical errors in the potential becomes clear by the following reflection. Physically the carrier concentration in the device is determined by the doping profile. The carrier density is high in the space charge region, but is several orders of magnitude lower in the distant diffusion zones. Because of the depletion approximation (4.3a,b) only majority carriers are considered. Global charge neutrality requires that an amount of space charge in the anode is compensated by a charge of the same amount, but with different sign in the cathode. An error, for example, of V_T (25mV at room temperature) falsifies the carrier concentration by a factor of $2.7 n_i$; which is about $4 \cdot 10^{10}$ cm^{-3} for silicon. Therefore, the space charge in the diffusion regions may be severely in error. Since the charge balance is lost, a 25mV error in the potential makes the result useless. Hence, potential errors of $V_T/10$ or lower must be achieved.

Another important point to be considered is the refinement of the mesh. As shown, e.g., in /16/ the discretization error depends on the smallest angle in the triangulation. To decrease this error it is <u>not</u> sufficient to simply increase the number of elements (triangles). At the same time one must assure that the element angles are all greater than a lower bound δ. Our grid generator fulfills this reqirement. Practical values for δ are $15^o...25^o$. Furthermore, the magnitude of that single parameter δ controls the 'character' of the grid. A small δ results in a very progressive, economic grid. A more uniform, slowly varying grid is achieved with a large δ. We would like to recall the fact that an overly progressive grid can lead to a bad condition number of the stiffness matrix and therefore should be avoided.

5.) Results

5.1) Linear Capacitances

The simulation geometry is shown in Fig.5-1. The influence of the spacing S and the conductor-ground plane distance H on the capacitances C_S and C_C are investigated. H takes values from 0.1 to 1.2 μm and S is in the range from 0.2 to 2.4 μm.

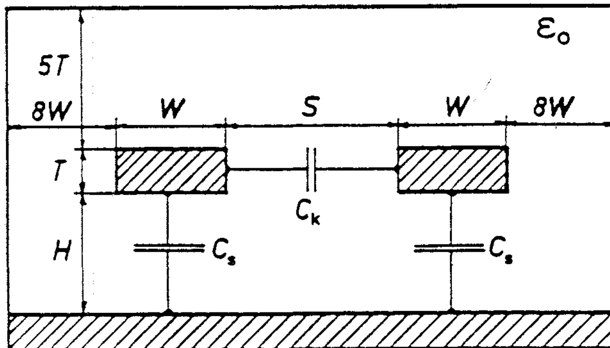

Fig.5-1 W = 2.0 μm T = 1.0 μm

The results are shown in the pseudo-3D plots in Fig.5-2 and Fig.5-3. The distances H and S are the independent variables. Fig.5-2 shows the substrate capacitance C_S and Fig.5-3 shows the coupling capacitance C_C. Although the S variation shows the main influence on C_C, one observes a non-negligible increase of C_C while increasing H. The fringing field is shielded well by the ground plane when H is low. If the transmission lines are withdrawn from the ground plane a more widespread fringing field is present. Thus, C_C shows an increase in spite of the constant S.

A comparison between the numerically computed capacitances and the classical parallel plate formula is shown in Fig.5-4 and Fig.5-5. The dependent variable is C_S/C_{SO} in Fig.5-4 and C_C/C_{CO} in Fig.5-5, respectively.

$$C_{SO} = \varepsilon_0 \cdot W/H \qquad (5.1a)$$
$$C_{CO} = \varepsilon_0 \cdot T/S \qquad (5.1b)$$

The use of (5.1) is inadequate for an accurate circuit layout. The computed capacitance values are typically 30%...100% larger than (5.1) predicts.

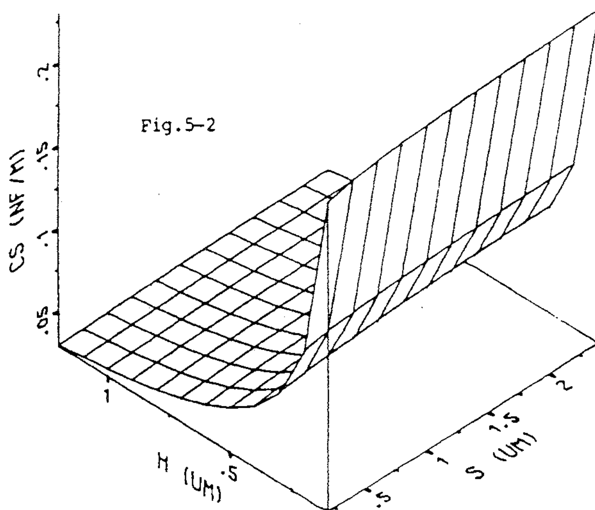
Fig.5-2
CS (NF/M)
.2
.15
.1
.05
H (UM)
1
.5
S (UM)
.5
1
1.5
2

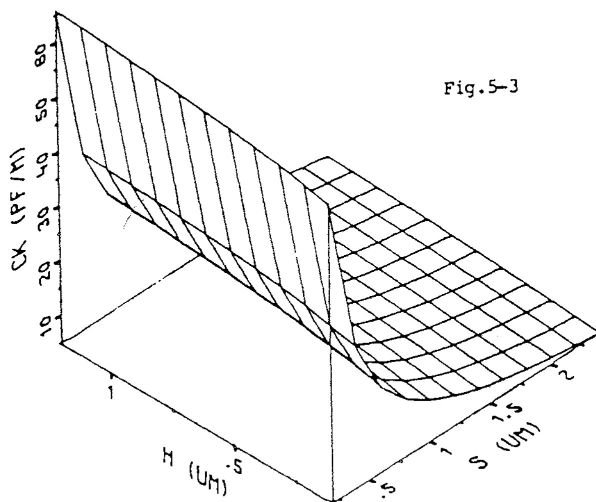
Fig.5-3
CK (PF/M)
80
50
40
30
20
10
H (UM)
1
.5
S (UM)
.5
1
1.5
2

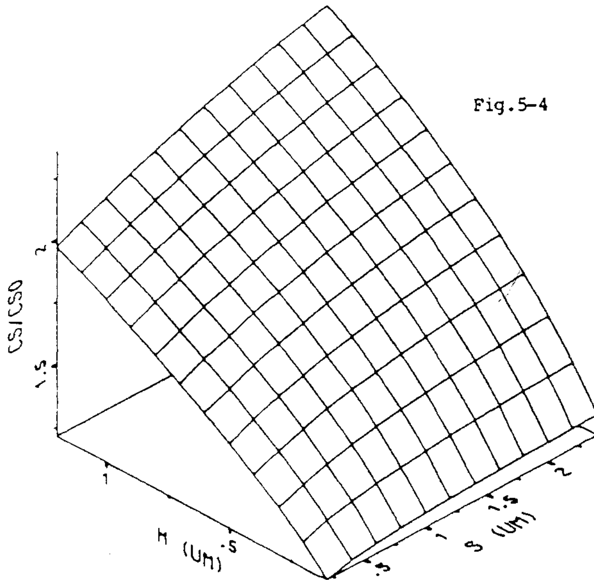

Fig.5-4

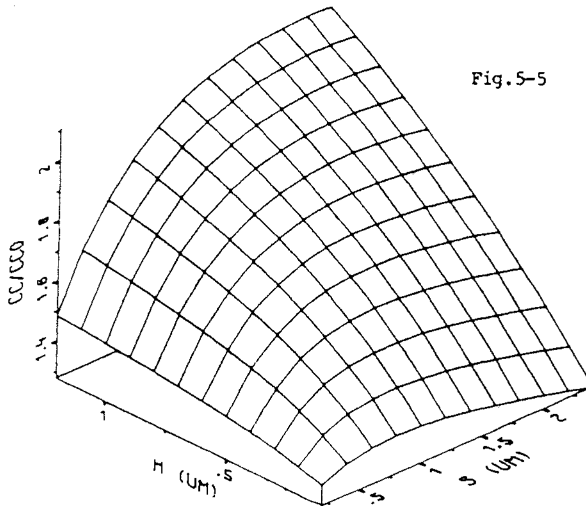

Fig.5-5

5.2) Junction Capacitance

The second example is based on the structure shown in Fig.5-6 (not to scale). The length unit is µm. The polysilicon wire is isolated from the substrate and the aluminum by a layer of silicondioxide. The substrate, which is p-doped with $N_A=10^{16}$ cm^{-3}, contains an implanted n-region. The analytic doping profile model from /19/ is used with the following assumptions: A dose of 10^{15} (phosphorus) is implanted through a 350nm thick protective oxide layer with an energy of 40keV. After the implant a 1200s annealing at 1000 °C is performed. The resulting profile is shown in Fig.5-7. A simplified first analysis of the structure usually treats the oxide/substrate interface as a conducting plane. The wires are assumed to be ideal conductors also. The capacitance is calculated to be 8.79pF/cm.

Simulating the full structure is much more costly. Three conductors will now be considered: the polysilicon wire, the p-region of the substrate and a 'compound' wire consisting of the aluminium contact plus the n-region. Fig.5-8 and Fig.5-9 show the potential distribution for two bias points. The gate potential is 3V, the bulk potential is -1V. The source potential is 1V in Fig.5-8 and 2V in Fig.5-9. The junction capacitance was evaluated to $C_{ju}(U_S=1V)=38.8pF/cm$ and $C_{ju}(U_S=2V)=32.8pF/cm$.

5.) Conclusion

We have outlined the importance of accurate capacitance computation for the purpose of VLSI design. A method for the calculation of linear and nonlinear capacitances has been presented.

We presented a depletion approximation suitable for accurate computation of semiconductor junction capacitances. The coupling capacitance of a transmission line pair vs. line and line to ground spacing was shown in a pseudo 3D-plot. The junction capacitance of a VLSI-Structure has been computed.

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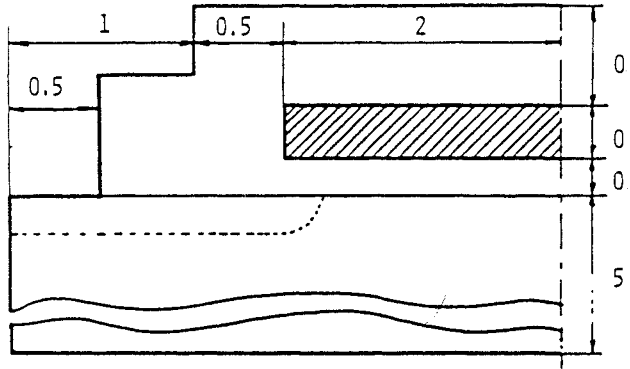

Fig.5-6 Simulation Geometry

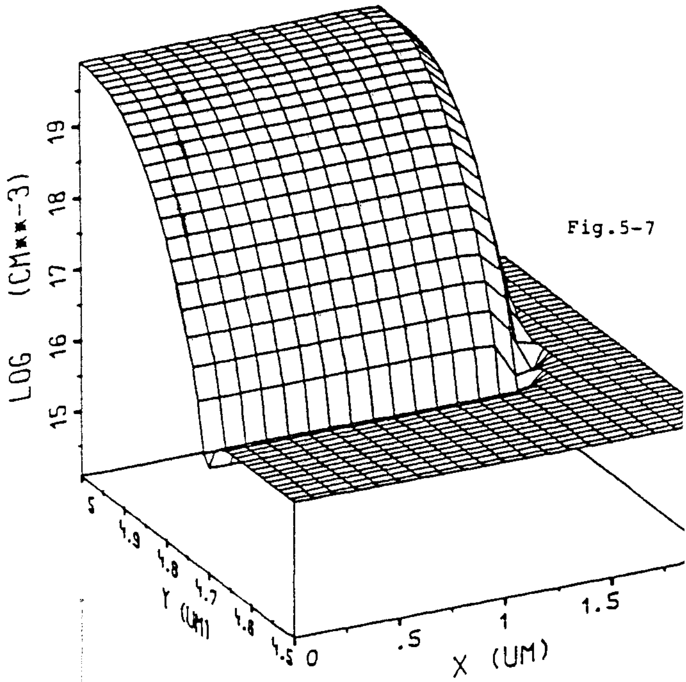

Fig.5-7

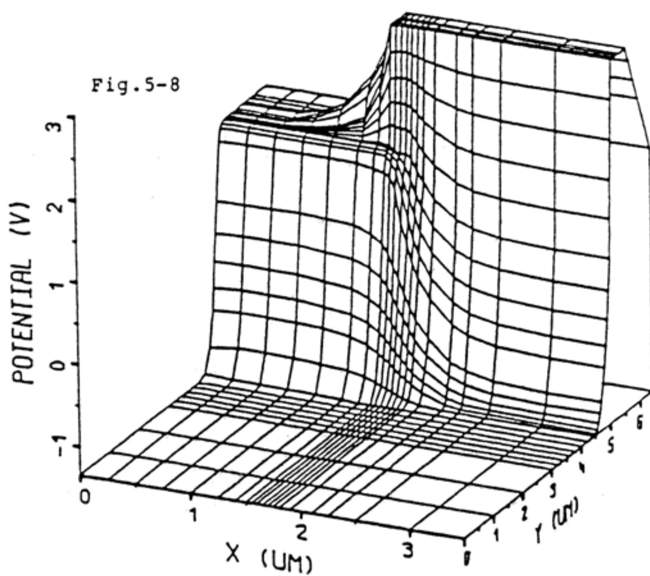
Fig.5-8
POTENTIAL (V)
3
2
1
0
-1
0
1
2
3
X (UM)
0
1
2
3
4
5
6
Y (UM)

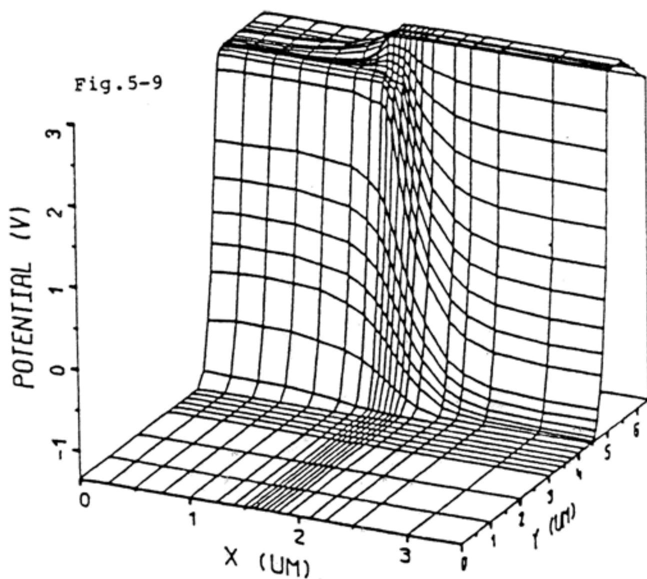
Fig.5-9
POTENTIAL (V)
3
2
1
0
-1
0
1
2
3
X (UM)
0
1
2
3
4
5
6
Y (UM)

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