Computation of VLSI Metalization Capacitance

F. Straker, S. Selberherr

Abteilung für Physikalische Elektronik
Institut für allgemeine Elektrotechnik und Elektronik
Technische Universität WIEN
Gußhausstraße 27, 1040 WIEN, AUSTRIA

I) Introduction

The progressive shrinking of semiconductor devices and inter-connection wire dimensions creates a number of problems for the circuit designer. Shorter pulse transition times and improved circuit delays may be outweighted by the rising signal travel time across interconnection lines. Advances in fabrication technology make higher package densitiy and larger chip area possible. This increases the average length of an interconnection wire. The careful consideration of capacitance, wire layout, circuit delays and crosstalk problems is necessary to ensure a successful chip design. Therefore a simulation program was developed to evaluate capacitances of common VLSI structures.

II) Calculation Method

Equation (1) defines the coefficients of capacitance in a n-conductor system:

$$Q_i = \sum_{\substack{j=1 \\ j\neq i}}^{n} C_{ij}(\Phi_i - \Phi_j) + C_{ii}\Phi_i \quad (1)$$

Q_i denotes the charge and Φ_i the electrostatic potential of conductor i, respectively. C_{ii} is the capacitance between infinity and conductor i. C_{ij} is the coupling capacitance between conductor i and conductor j. We are concerned with the

calculation of the $1/2 \cdot n(n+1)$ coefficients C_{ij}. The approach to accomplish this task is described in the following.

The multiconductor capacitance problem is frequently stated in integral equation form. The difficulty of this concept is the finding and evaluation of Green's Function suitable for the examined conductor geometry. We adopted a different concept to handle all the structures that are widely used in VLSI chips like metal and diffused transmission lines, line crossings and MOS structures.

The two dimensional Poisson equation is numerically solved. The domain represents a detail of the cross section of the chip. The number of conductors/dielectrics is only limited by the available computer resources. Fig. 1 shows a simulation example.
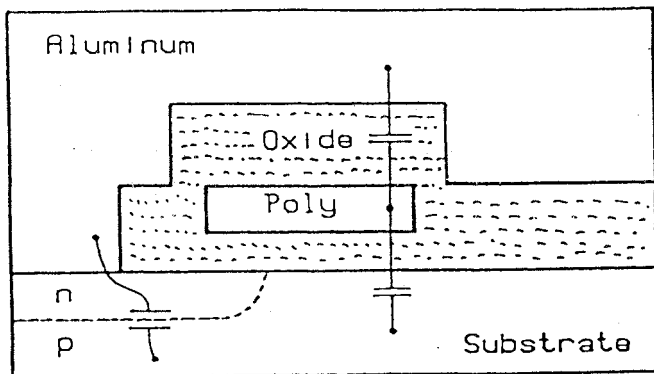

Fig. 1

Above the doped substrate there is a poly line (conductor 1) surrounded by SiO_2 insulation. An aluminum wire (conductor 2) contacts the semiconductor. We consider the substrate devided into to "wires" by the pn-junction (conductors 2, 3). Therefore the effect of the junction capacitance is also taken into account. After solving Poisson's equation the computed electrostatic potential allows the calculation of the charge distribution on the conductor surfaces.

For the non-trivial case of more than two conductors ($n > 2$), we use multiple solutions of Poisson's equation with varying boundary conditions to compute all the C_{ij}. This results in an overdetermined system of equations (2) for the C_{ij}

$$A\ c = q \qquad (2).$$

c and q are the vectors with components C_{ij} and Q_i, respectively. Introducing the singular value decomposition of the matrix A

$$A = UQV^T \qquad (3)$$

into (2) and solving for the unknown vector c with a QR-decomposition algorithm results in

$$c = VQ^{-1}U^Tq \qquad (4).$$

The advantage of this method is obvious. The QR algorithm evaluates the equation with the best condition number first, giving numerically reliable and stable results. Comparisons with data already published show good agreement of the results. Specific examples will be presented.

4

AN IMPROVED MODEL FOR THE MAXIMUM AVAILABLE POWER FROM A p-n JUNCTION SOLAR CELL

I.R.M.Mansour

Alfateh University,Faculty Of Engineering
Centre For Solar Energy Studies,Tripoli-Libya

In spite of the widespread acceptance of the importance of minority carriers recombination everywhere inside a p-n junc-