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# A HOT CARRIER ANALYSIS UTILIZING MINIMOS 3.0

W.Hänsch and C.Werner

Siemens AG, Central Research and Development, Microelectronics
Otto-Hahn-Ring 6, D-8000 Munich 83, FRG

S.Selberherr

Institut für Allgemeine Elektrotechnik und Elektronik,
Technische Universität Wien, Austria

## Introduction

Modern VLSI-circuits require a high degree of miniaturization, which is in principle achieved by employing scaling laws.
However, keeping the voltage supply on the standard 5V there will be electrical fields of considerable strength in the device. The basic task of device simulation is to optimize the device in such a way that parasitic effects like substrate current and oxide injection will be minimized. In this presentation we will show how hot-carrier effects will modify carrier density and current density distributions within the device, which are crucial to determine the above mentioned phenomena.

## MINIMOS 3.0

Current device simulations are based on the conventional semiconductor equations. Here high field effects are accounted for by a field dependent mobility for velocity saturation and simple models for impact ionisation [1] which gives the substrate current. Up to now there is no code available that takes heed of the strong non equilibrium situation of carriers in high electric fields. In the simulation programm MINIMOS 3.0 a selfconsistent treatment of the hot carrier problem is given. It is based on the hot-electron formulation published elsewhere[2]. The key is a modified current equation with a selfconsistent mobility and carrier temperature model [3]

$$j = q/u n E + q/u \operatorname{grad}(U_T n) \qquad (1)$$

$$U_T = U_{To} + \frac{2}{3}\,\tau_{\varepsilon_o} v_s^2 \left[ \frac{1}{/u_{LISF}} - \frac{1}{/u_{LIS}} \right] \qquad (2)$$

Here $U_{To}$ is the thermal voltage kT/q, $\tau_{\varepsilon_o}$ the energy relaxation time, and $v_s$ the saturation velocity. The mobility is composed of the usual isotropic contribution containing bulk (LI), surface (S), and velocity saturation (F). In addition we have an anisotropic contribution due to the presence of the $Si/SiO_2$-interface [3]

$$/u = /u_{LISF} \begin{bmatrix} 1 - \dfrac{1}{1 + \alpha(x)\,/u_{LI}/u_{LIS}} & 0 \\ 0 & 1 \end{bmatrix} \qquad (3)$$

Here x is the distance perpendicular to that interface and the function $\alpha(x)$ tends to infinity as x goes to infinity.

## Hot-electron effects in n-channel MOSFET

In Figures 1-7 we show the electron density, electronic temperature, and electron current density distributions as calculated for a typical short channel MOSFET with gate length 0.7 /um. It has AS-source/drain and an oxide of 12.5 nm thickness. The substrate doping is $N_A = 10^{17}\,cm^{-3}$. A channel implant was used to adjust the threshold voltage. The device was biased: $U_S = U_B = 0$, $U_G = 1V$, $U_D = 5V$. This provides a situation where hot electron effects should be substantial. We compare the conventional results, including impact ionisation, as calculated with MINIMOS 2.9 with the new hot carrier version of MINIMOS 3.0. As expected from previous studies, the minory carrier density is distributed smoother [4], especially in the high field region near drain. Due to the low absolute electron concentration, compared to the substrate doping, the fields do not change appreciably in this region. Quite dramatic, however, is the redistribution of the electron current density as shown in Figures 5 and 6. Hot electron effects push the current density deeper into the bulk region. Therefore the average distance from the $Si/SiO_2$ interface is increased, similar to the electron density. This redistribution of electron current and electron density will considerably influence substrate current and oxide injection. Preliminary studies show that, provided the same drain current is assumed, the substrate current will decrease. In Figure 4 we show profiles of the electron density at different positions of the channel. The solid lines are located in the middle and show only little modification. The broken lines, placed at the drain end, show substantial changes. Comparing this with the electron temperature plot in Figure 3 shows its correspondence with the hot electron effects. Similar profiles are shown in Figure 7 for the electron current densities. The bump in the current density at $x \approx 7$ nm is caused by the doping dependence of the mobility and is generated by the channel implant.
All calculations were performed on a SIEMENS VP 200 vector processor.

## References


[1] A.Schütz, S.Selberherr and H.Pötzl; MINIMOS 2.9 -Users manual

[2] W.Hänsch and M.Miura-Mattausch, submitted to Journal of Applied Physics

[3] W.Hänsch and S.Selberherr, submitted to IEEE-Electronic Device letters

[4] D.Schmitt-Landsiedel and G.Dorda, IEEE Trans. Elec. Dev. ED-32, 1294 (1985)


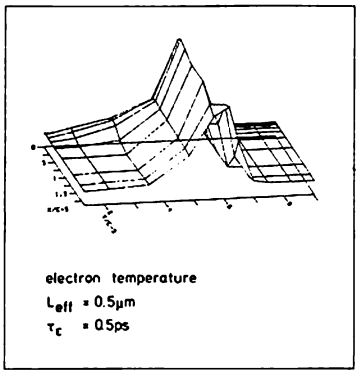


Fig 3: Electron temperature distribution at the drain side of a short channel MOSFET.

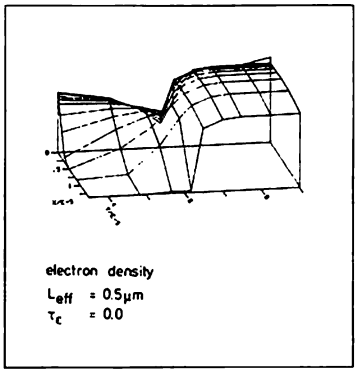


Fig 1: Electron density at the drain side of a short channel MOSFET. Conventional simulation.

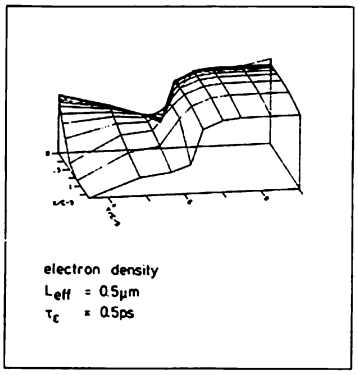


Fig 2: Electron density at the drain side of a short channel MOSFET. Hot carrier simulation.

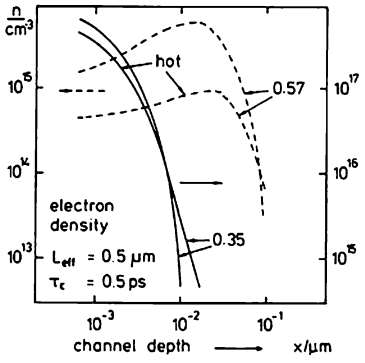


Fig 4: Profile of the electron density at different positions of the channel. Solid lines: middle of channel y=0.35 µm, broken lines: drain region y=0.57 µm. y=0 corresponds to the source side of the gate contact. A subdiffusion of 0.1 µm is assumed.

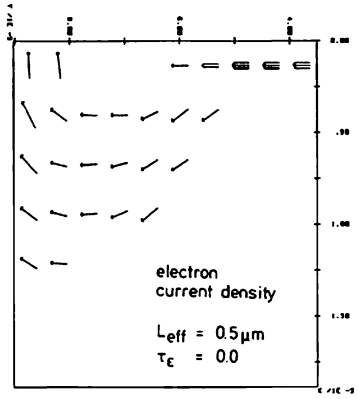


Fig 5: Electron current density distribution at the drain side of a short channel MOSFET. Conventional simulation.

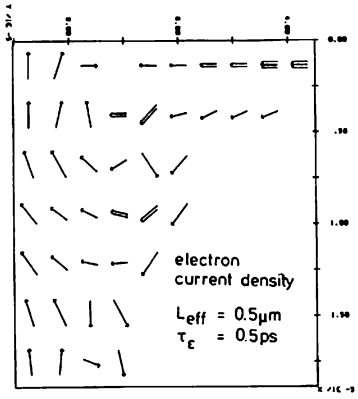


Fig 6: Electron current density distribution at the drain side of a short channel MOSFET. Hot carrier simulation.

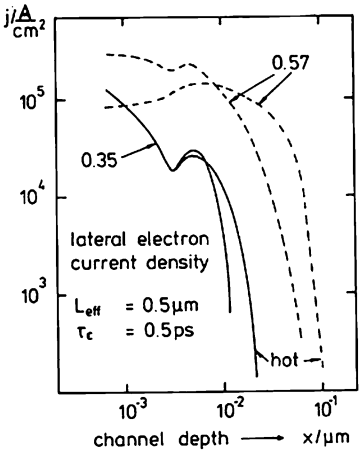


Fig 7: Profile of the electron current density at different positions of the channel. Specifications see Fig 4.