Capacitance Computation for VLSI Structures

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Abstract: The progressive shrinking of semiconductor devices and interconnection wire dimensions creates a number of problems for the designer of integrated circuits. Shorter pulse transition times and improved circuit delays may be outweighted by the rising signal travel time accross interconnection lines. This increases the average length of an interconnection wire. The careful consideration of capacitance, wire layout, circuit delays and crosstalk problems is necessary to ensure a successful chip design. Therefore a simulation program has been developed to evaluate capacitances of common integrated circuit structures. Finite elements are used to solve the two dimensional Poisson equation. The generation of the finite element mesh is fully automatic. The discretized simulation region represents a cross section of the integrated circuit. The computed electrostatic potential allows the calculation of the charge distribution on the conductor surfaces. For the non-trivial case of three or more conductors we use multiple solutions of Poisson's equation with varying boundary conditions to find all coefficients of capacitance. Comparisons with data already published elsewhere show good agreement. The analysis of a modern 256kbit dynamic random access memory cell is presented as an application of the method.

1.) Introduction

For readers who are non-specialists in the field of microelectronics we present some background information to make clear the motivation for our work.

Yield enhancement and the progressive miniaturization of components were the key factors leading to drastic savings in manufacturing costs of integrated circuits (IC). Developement of the Metal - Oxide - Semiconductor technology, improved wafer processing especially accurate mask positioning and advanced optical lithography permitted the increase of packing densities. The dimensions of the transistor itself remained roughly constant.

In 1974 a research group of IBM - Yorktown Heights published a concept /1/ for manufacturing smaller transistors with superior characteristics, especially less signal delay. In 1977 miniaturization has reached a critical stage. The logic gates made of MOS - Transistors had a switching delay comparatively to the time constant of the polysilicon interconnection wires.

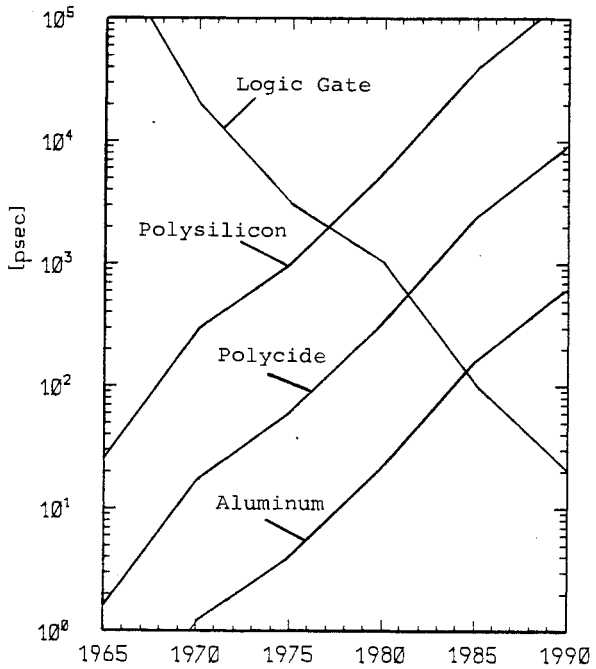

Fig. 1.-1 Logic gate and line delay

This fact is shown in Fig. 1.-1. The vertical axis represents the gate switching delay and the RC delay of an interconnection respectively. The data has been compiled or forecasted for a time frame of 25 years starting in 1965 from /2/, /5/, /6/, /7/. A hectic research activity was started to develop lines with lower resistance to decrease delay. But approximately 1984 even the low resistivity aluminum was surpassed by the ever faster gates. The influence of the chip wires on the performance of the circuit could no longer be neglected. The development of the 64kbit - RAM (Random Access Memory) during 1976...1978 may serve as a prominent example of a design that was plagued by wire capacitance problems.

$$\tau = \frac{\rho\, \varepsilon_o\, \varepsilon_r\, L^2}{H\, T} \qquad (1.-1)$$

$$\tau' = \frac{\rho\, \varepsilon_o\, \varepsilon_r\, (Lk)^2}{H\, T} = \tau\, k^2 \qquad (1.-2)$$

To illustrate this really important point we calculate the RC time constant of the rectangular wire shown in Fig. 1.-2. It's is located above a conducting ground plane and surrounded by a dielectric with dielectric constant of ε. ρ is the specific resistance of the wire material. By neglecting fringing effects the time constant τ is given by (1.-1). Reducing W, H and T by a factor 1/k, $k>1$, but conserving the length L we obtain (1.-2). τ' is the time constant of the scaled design whitch unfortunately grows with k^2.

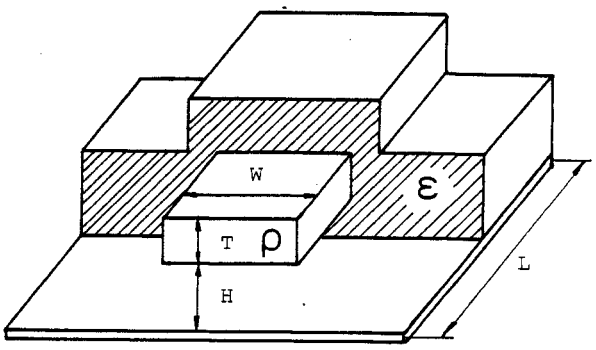

Fig. 1.-2 Geometry of interconnection

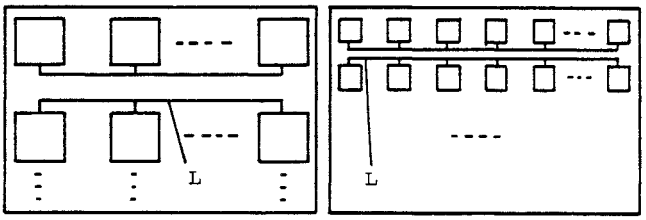

Fig. 1.-3 Scaling by k=2

The assumption of constant length is justified by Fig. 1.-3. Designers place as much components as possible on a chip of given area. With respect to the wiring that means L is <u>not</u> scaled down, provided that the chip architecture is not changed.

The maintenance of suitable noise margins forces control of coupling capacitances between parallel and sometimes even crossing lines. Power requirements depend, in part, on the amount of capacitance at a gate output. For those reasons a software tool has been developed that simulates device and interconnect capacitances of structures in very large scale integrated (VLSI) circuits.

2.) Multiconductor Capacitances

The 3-conductor system of Fig 2.-1 shall serve as an example for the following discussion. For the time being let us assume that all conductors are surrounded by a linear, homogeneous insulator with dielectric constant ε. First of all we define C_{ij} as

the coupling capacitance between conductor i and conductor j, C_{ii} as the self capacitance of conductor i, Q_i and φ_i as the charge and potential of conductor i, respectively. The number of conductors is k.

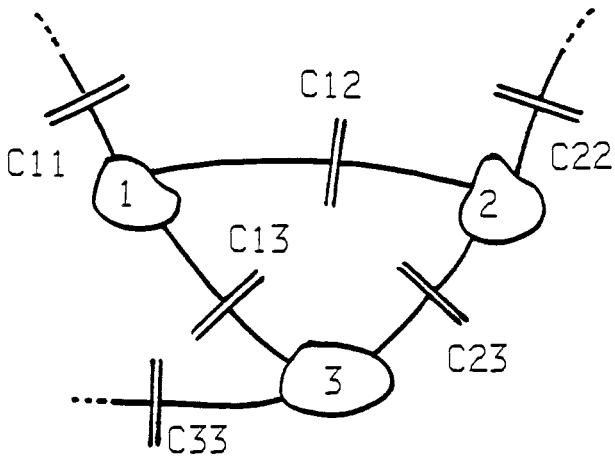

Fig. 2.-1 3-Conductor system

The set of equations (2.-1) shows the relationship between the variables.

$$Q_{ij} = C_{ij}(\varphi_i - \varphi_j) \qquad (2.\text{-}1a)$$

$$Q_i = \sum_{\substack{j=1 \\ j \neq i}}^{k} C_{ij}(\varphi_i - \varphi_j) + C_{ii}\varphi_i \qquad (2.\text{-}1b)$$

The unknowns are the coefficients C_{ij}. Please note, that solving (2.-1b) is different from solving a system of linear equations $A\mathbf{x} = \mathbf{b}$. The number of unknowns is $k(k+1)/2$ but only k-1 linear independent equations exist. The charge distribution Q_1, Q_2, ... , Q_k depends on the conductor potentials and is assumed to be known. Section 2.1 of the paper outlines how to get the charges.

If the C_{ij} are constants then relations (2.-1ab) are linear. That means capacitance depends purely on the geometry of conductors and dielectric interfaces. In order to compute the C_{ij} from the charges we may assume multiple sets of conductor potentials until enough linear independent equations are available to match the number of unknowns.

In semiconductor circuits capacitance often varies with voltage. In this case we have prescribed conductor potentials given by the circuit bias. However, we apply a small voltage offset to the conductors and use the resulting change in charges to compute voltage dependent capacitances at a certain bias point. This procedure is outlined in more detail in /8/.

2.1) Computation of Conductor Charges

Equation (2.1-1) is utilized to compute the conductor charges. This equation says that the integral of the perpendicular component of the electrical displacement D over a closed surface A equals the amount of charge inside A. Reducing this general statement to the two-dimensional case and substituting electrostatic potential u for the displacement D yields (2.1-2).

$$\int_A \mathbf{D} \cdot d\mathbf{A} = Q \qquad (2.1\text{-}1)$$

$$Q_i = -\varepsilon \int_{S_i} du(x,y)/d\mathbf{n} \cdot ds \qquad (2.1\text{-}2)$$

S_i denotes an arbitrary closed curve which surrounds conductor i. $du(x,y)/d\mathbf{n}$ is the spatial derivative of the potential perpendicular to S_i. We must find the potential $u(x,y)$ in the simulation region in order to solve (2.-1) for the C_{ij}. Poisson's equation (2.1-3a) is appropriate to give that information.

$$\varepsilon \operatorname{div} \operatorname{grad} u = -\rho(x,y,u) \qquad (2.1\text{-}3a)$$

Insulator (dielectric)

$$\rho = 0 \qquad (2.1\text{-}3b)$$

p-region:

$$\rho(x,y,u) = q\,(p + C_t(x,y)) \qquad (2.1\text{-}3c)$$
$$p = n_i \cdot \exp((\varphi_A - u)/U_T) \qquad (2.1\text{-}3d)$$

n-region:

$$\rho(x,y,u) = q\,(-n + C_t(x,y)) \qquad (2.1\text{-}3e)$$
$$n = n_i \cdot \exp((u - \varphi_K)/U_T) \qquad (2.1\text{-}3f)$$

$$C_t(x,y) = N_D(x,y) - N_A(x,y)$$
$$U_T = kT/q$$

Boundary conditions:

$u - u_{Fix} = 0$ on C_{Fix} (fixed boundary)
$du/d\mathbf{n} = 0$ on C_n (Neumann boundary)

$\rho(x,y,u)$ denotes the space charge density. In insulating regions (dielectrics) ρ is assumed to be zero (2.1-3b). Semiconductor regions are either n or p-type, depending on the doping profile C_t. It is defined as donor concentration N_D minus acceptor concentration N_A. C_t is a known quantity. (2.1-3c,d) is the expression for ρ in a p-type region. In a n-type region ρ is modeled by equation (2.1-3e,f). The electronic charge of $1.6 \cdot 10^{19}$ As is denoted by q, n_i is the intrinsic number of silicon. φ_A, φ_K is the applied contact potential in the p or n region. C_{Fix} unified with C_n is the boundary of the simulation region B. Boltzmann's constant k and the absolute temperature T complete the list of symbols used in (2.1-3). Due to the limitited space we have to confine ourselves to state this set of equations without any derivation. The justification of the above model (2.1-3) can be found in /8/.

In case of semiconducting material (2.1-3a) is a non-linear partial differential equation (PDE). No analytical solution is known for general doping profiles C_t and geometrically irregular domains.

2.2) Numerical Aspects

Numerical methods have to be used to tackle (2.1-3). The finite element scheme was employed to solve the PDE. Triangular elements with biquadratic basis functions have been found as the optimal choice. An algorithm has been developed that generates the spatial discretization of the simulation region (finite element mesh) automatically. Solutions of non-linear problems are found by iteration. A Newton algorithm modified to control potential overshoot during the first few iterations was implemented. The system of linear equations in each Newton-step is solved by the classical frontal method.

3.) A Realistic Example

Dynamic memories (dRAM, dynamic random access memory) have always been the leader in packing density among integrated circuits of comparable production period. This is mostly because of the regular device structure. The semiconductor industry used the development of memories to protrude into new levels of technology and complexity. A 256kbit memory from Mitsubishi /3/ will serve as an example for the application of computer simulation to a real-word design problem.

3.1) RAM Operation Principle

This section is intended for non-specialists to provide a simplified description of memory operation. Experienced readers may well skip it.

The circuit model in Fig. 3.-1 explains the function of major memory elements. The storage cell consists of a MOS capacitor and a transistor. One contact, the so called plate, is held on fixed potential U_P (mostly 0V). The second contact is connected via the MOS transistor with the bit line (BL). The word line (WL) switches the transistor from off to on-state and vice versa. Charging of the storage capacitor C_C depends on the BL voltage level during on-state. C_C is charged if $U_{BL} > U_P$. After switching the transistor off the charge already in C_C is conserved. Several leakage mechanisms which however will not be discussed here require refreshing of the stored information 200...300 times in a second. This explains the term dynamic RAM.

To read information additional cells, so called dummy cells, are needed. Their storage capacitor is $C_C/2$. Before any read operation a zero is written into the dummy cell by clock PS. Simultaneous sensing of the storage and the dummy cell provides the cell signal of approximately 200mV. The sense amplifier regenerates this signal to 5...9V. A word line pulse refreshes the cell information which was erased by the sensing operation.

A problem is the ratio of C_{BL}/C_C = 10...20 in 256kbit memories. Prior to the evaluation of the cell information the large parasitic C_{BLO} must be charged in order to detect the small signal from C_C. This is called presensing. The exact knowledge of C_{BLO} and C_C is essential for the layout of the memory peripheral circuits like line drivers and sense amplifiers. Coupling between the bit and word line is another important question. The coupling capacitance is needed to estimate the storage array noise level.

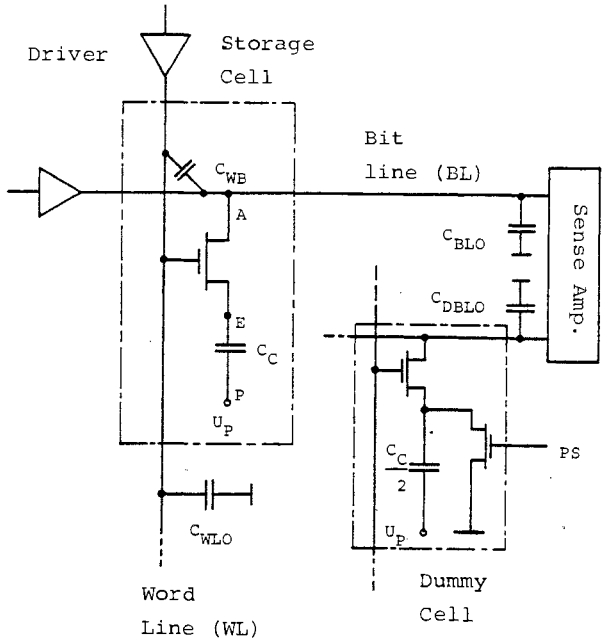

Fig. 3.-1 RAM Circuit model

3.2) Memory Cell Physical Structure

Fig. 3.-2 shows the cross section of a cell along the bit line /3/. Vertical dash-dotted lines are axes of symmetry. Note, that functionally equivalent elements are labeled identically in the circuit (Fig. 3.-1) and in Fig. 3.-2.

The source of the MOSFET is the n^+ implant A which is also used to contact the bit line with the substrate. Implant E is the drain region. It reaches far under the plate P and makes the second electrode of the storage capacitor C_C. WL' is the word line of the neighbour cell.

The important capacitances are also shown in Fig. 3.-2. Some have been neglected, for example the coupling between WL and WL'. These are very small and can safely be assumed zero.

3.3) Computation of the Storage Capacitance

As shown in Fig. 3.-3 C_C consists of a MOS capacitance C_m and a junction capacitance C_j in series. This arrangement improves storage capability without increasing the cell area. This Hi-C cell concept was presented in /9/.

The doping profile for the simulation is shown in Fig. 3.-4. Values on the vertical axis are base 10 logarithms of concentration in cm^{-3}. We used the analytical doping model for gaussian profiles described in /4/. The pn-junction is at a depth of approximately 0.2um at x = 4um. Following the junction in

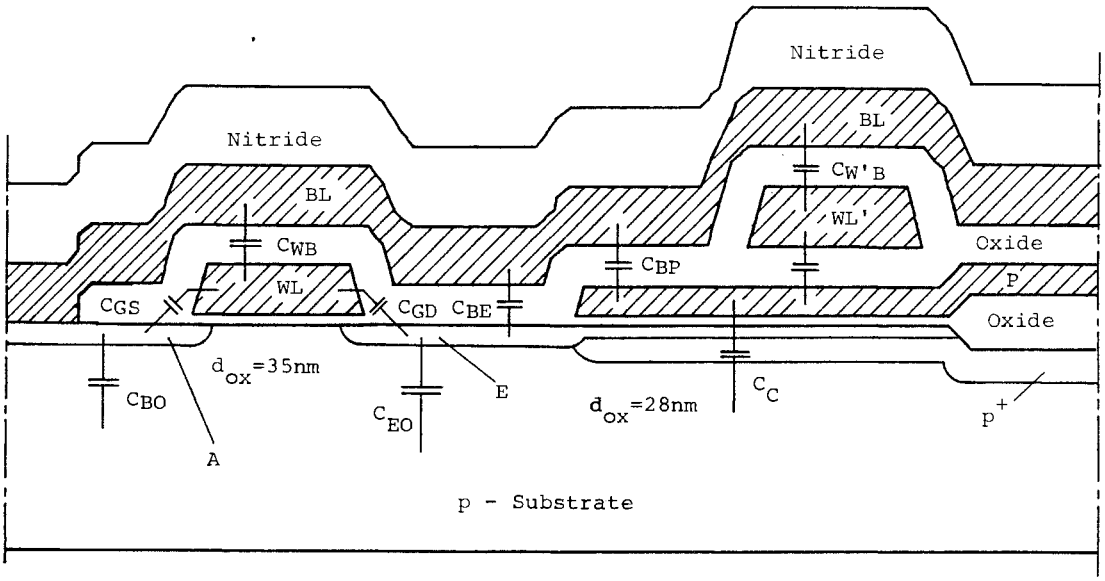

Fig. 3.-2 Memory Cell Cross Section

negative x-direction it bends away from the surface until a depth of 0.4um is finally reached.

The vicinity of the plate P is the interesting region for the computation of C_C. The geometric definition of the simulation domain is the next step. The perimeter and interfaces of the domain are splitted up into single edges and numbered. Fig. 3.-5 shows the simulation region after this preparation. The arrows near the edge numbers denote the edge orientation. On the contacts (edges 1, 5, 9, 11, 10, 19, 26) we have Dirichlet boundary conditions. Their specific value is fixed by the memory cell bias. On all the other boundary edges we have homogenious Neumann conditions.

A subregion is specified by grouping it's boundary edges together. Observation of orientation is required. Moving along the boundary in positive orientation, we must have the region interior to the left and the exterior to the right. For example the oxide subregion is defined by edges 6, 7, 18, -8, 19, 10, 20, -11, -9, -15.

After having specified the region of interest in a rigorous way the required finite element net is generated automatically. Doing this with the computer is an enormous speedup compared against creating the grid manually. It is also very less error-prone. The grid is shown in Fig. 3.-6. For details about the mesh generating program see /8/.

The numerical solution of Poisson's equation in the simulation region can be seen on the next plots. The potential distribution and the electric field are shown in Fig. 3.-7 and Fig. 3.-8, respectively. The circuit bias was U_S = -3V and U_W = 0V. The field is normalized to the silicon breakdown field of 30MV/m. The space charge layer of the Hi-C diode extends 1.7um into the substrate which is lightly p-doped with $10^{15}cm^{-3}$. The p^+ implant achieves a very short space charge layer under the plate. The junction capacitance C_j is large, as desired. The maximal field of 90% of the breakdown field appears at the junction of the Hi-C diode.

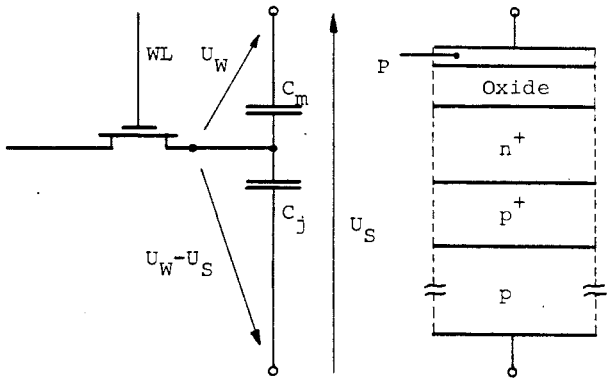

Fig. 3.-3 Storage Capacitance

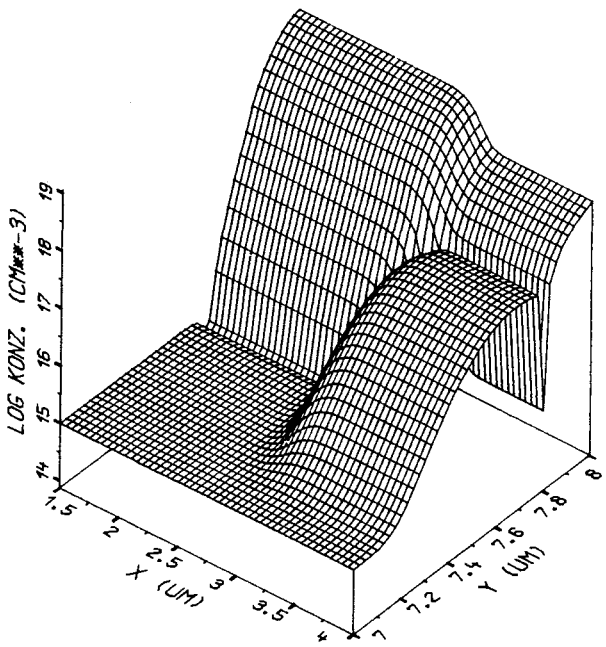

Fig. 3.-4 Doping Profile

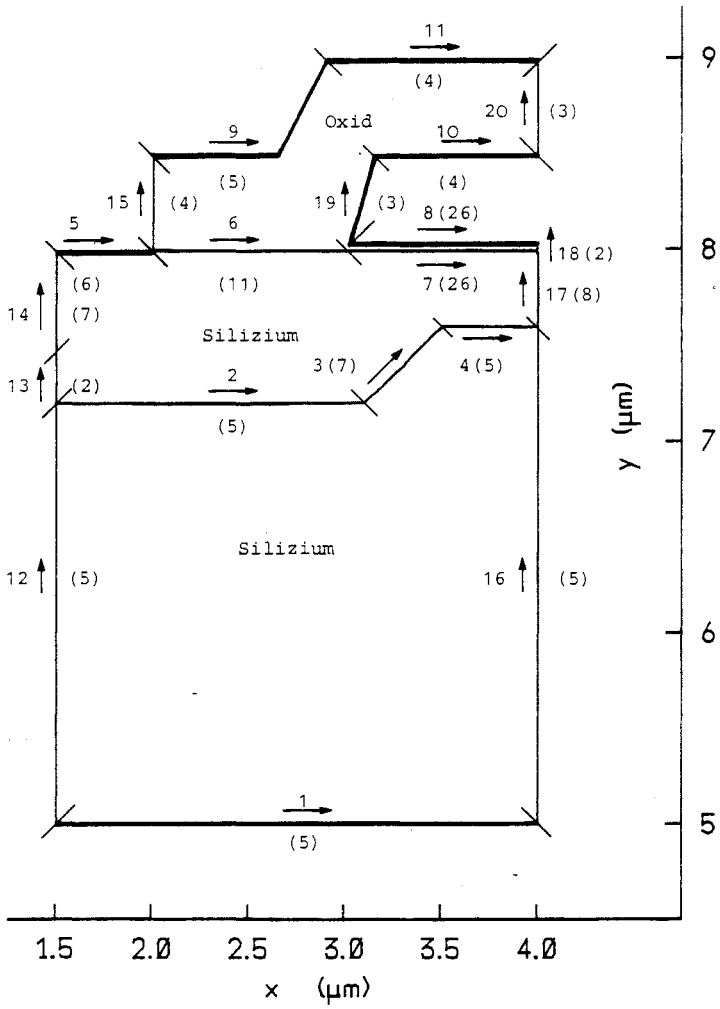

Fig. 3.-5 Simulation Region

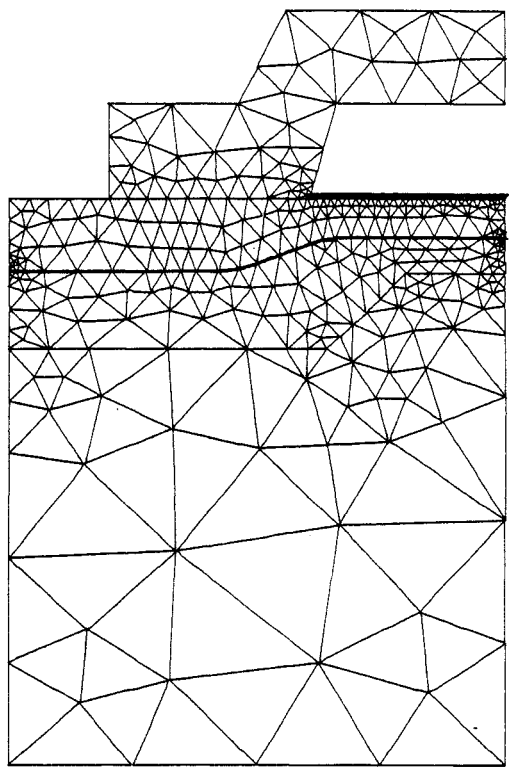

Fig. 3.-6 Discretized Region

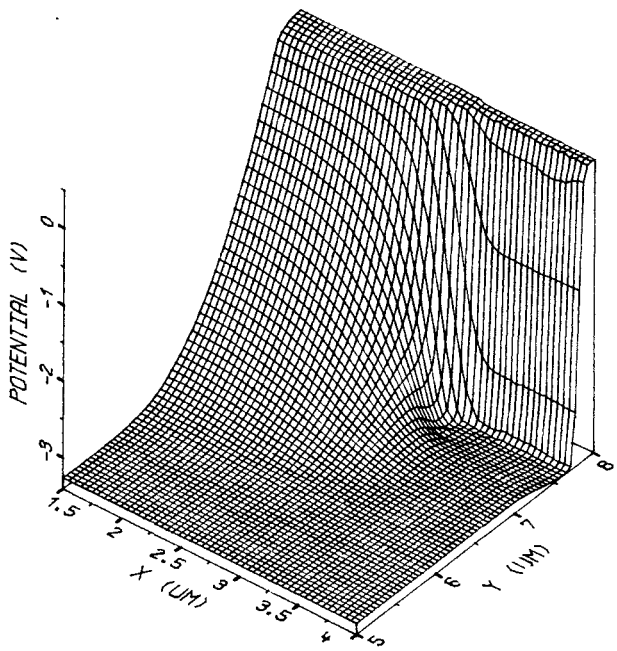

Fig. 3.-7 Electrostatic Potential

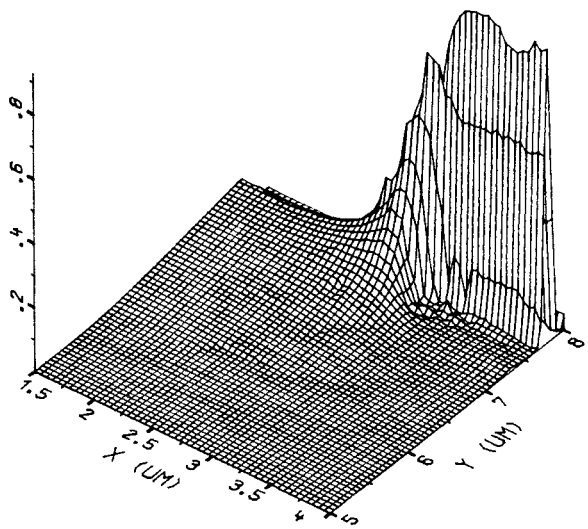

Fig. 3.-8 Normalized Field

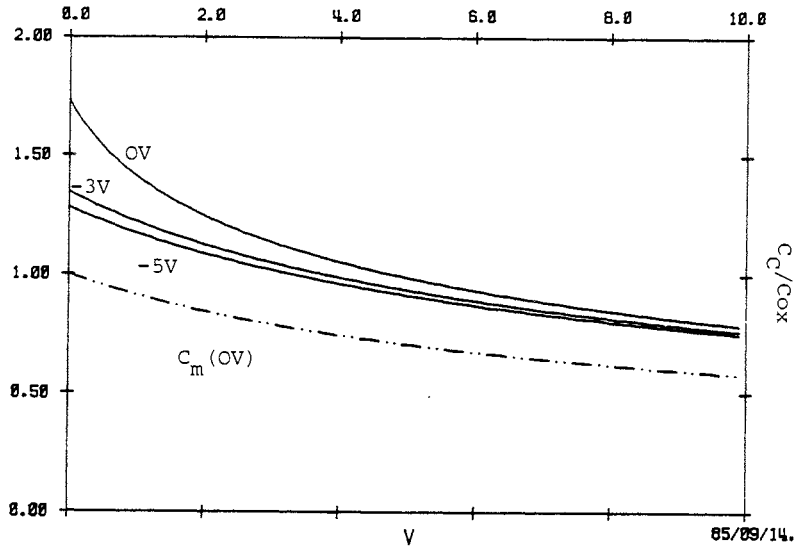

Fig. 3.-9 Cell Characteristic

Calculating the cell capacitance for many values of U_W yields the C_C-characteristic Fig. 3.-9. C_C is normalized to the oxide capacitance of 36fF. The dash-dotted curve is for a MOS capacitance only. The solid curves are for the Hi-C structure with the additional contribution of the junction capacitance in 0.2um depth. Curve parameter is the substrate bias U_S. The margin between solid and dash-dotted curves visualizes the improvement in storage capacitance. It is most significant for zero bias. However a negative bias of 3...5V is desirable to improve soft error performance and to reduce capacitive loading of the bit line.

4.) Conclusion

A concept for the evaluation of capacitances in VLSI structures has been presented. The necessary mathematical framwork has been stated. We calculated the storage capacitance of a modern 256kbit RAM with Hi-C cell as a practical example for an application of this method. The improvement in charge storage capability over the conventional cell design has been shown clearly.

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