Punch–Through in Resurf Devices

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One key issue for high voltage CMOS structures is the proper design of the output driver devices, which are usually lateral DMOS transistors. We present results of the punch–through analysis of these so called resurf devices with respect to parasitic transistors depending on epitaxial and substrate doping.

The geometry of one particular transistor of this category is given in Fig.(1):
an n–channel device with 2μm channel length, oxide thickness 0.2μm, substrate doping $1.5 \cdot 10^{15}$ cm^{-3} and $1.5 \cdot 10^{14}$ cm^{-3}, respectively, epitaxial doping $3.0 \cdot 10^{15}$ cm^{-3} and $3.0 \cdot 10^{14}$ cm^{-3}, respectively.

By applying the two - dimensional transient device simulator BAMBI we have particularly analyzed the influence of the epitaxial and substrate doping on punch-through effects. For the first simulation we assumed an epitaxial doping of $3.0 \cdot 10^{15}$ cm^{-3} and a substrate doping of $1.5 \cdot 10^{15}$ cm^{-3}. At a drain voltage of about 50V the onset of a parasitic transistor at the npn–junction under the gate could be observed. In Fig.(2) the current density at 105V drain voltage in off–condition is shown. There is a moderate current flow from the drain contact (right peak in Fig.(2)) through the epitaxial layer towards the parasitic npn–transistor, where it raises to the n^+–doped source region (left peak in Fig.(2)). By this punch-through source and drain are short-circuited while the MOS transistor still remains in off–condition.
For the second simulation both the epitaxial and substrate doping was reduced by a factor of 10. From Fig.(3) (current density) it can nicely be seen that there was no punch–through even at 130V drain voltage in off-condition regarding that the scales of the current density in Fig.(2) and Fig.(3) differ by more than a factor of 10^2.
We also present results of a low voltage simulation, where the parasitic transistor is built up, but does not influence the behaviour of the MOS transistor in on–condition in a critical way.

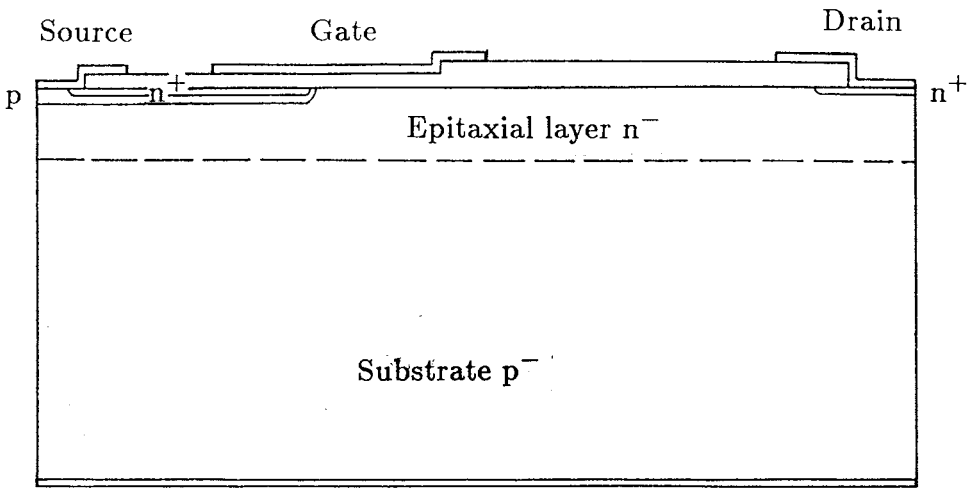

Fig.(1) Geometry

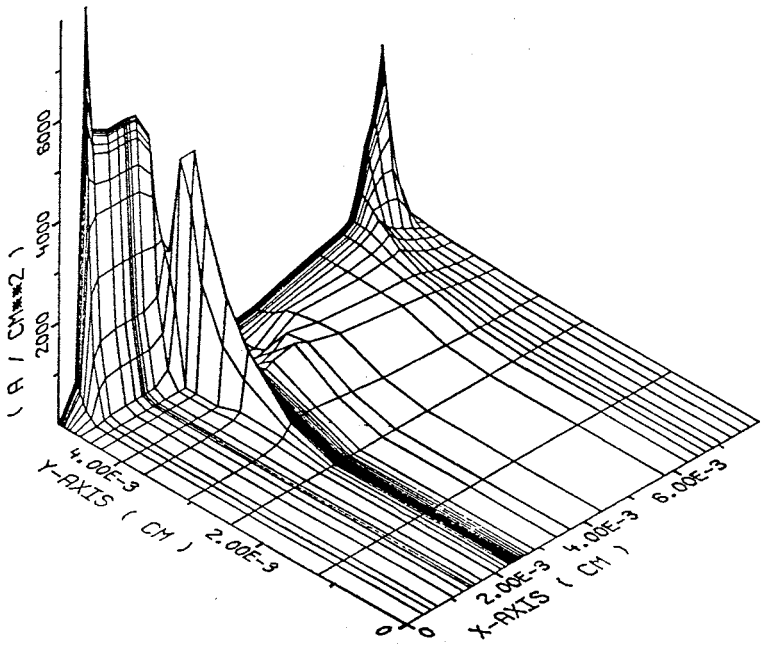

Fig.(2) Current density
with punch-through

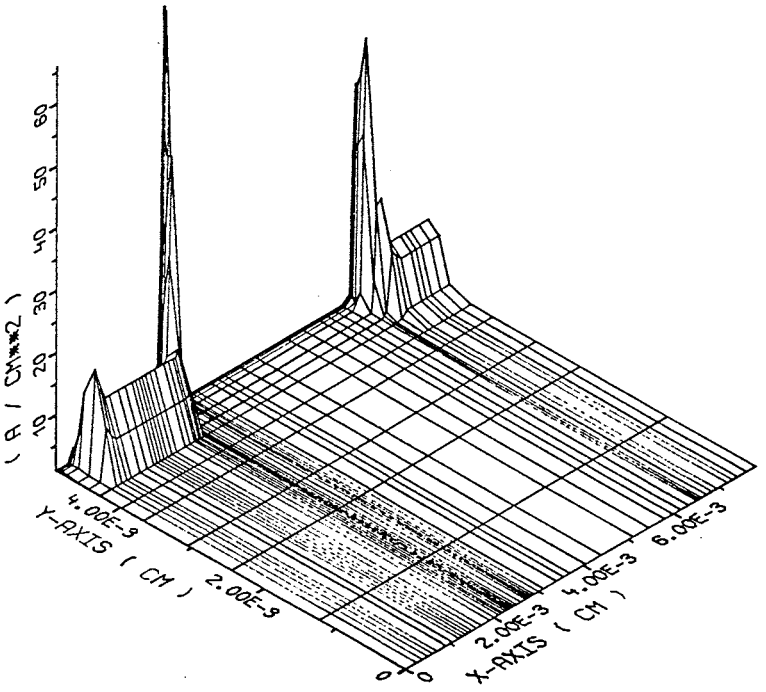

Fig.(3) Current density
without punch-through