

3D MOSFET DEVICE EFFECTS DUE TO FIELD OXIDE

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Abstract – This paper presents 3D effects of MOSFET's due to the nonplanar nature of the field-oxide body. The investigations have been carried out by MINIMOS 5 our fully three-dimensional simulation program. Three-dimensional effects like threshold shift for small channel devices, channel narrowing and the enhanced conductivity at the channel edge have been successfully modeled.

1 Introduction

The shrinking dimensions of the elements of IC's require suitable device models in physics and mathematics for accurate simulation. The usual two-dimensional device simulations describe fairly well the electrical characteristics for wide channel transistors but the advanced VLSI technology led to serious problems in modeling very narrow channel devices and therefore a great demand appeared for 3D simulations. The three-dimensional effects in MOSFET's like the shift of the threshold voltage, enhanced conductivity or the large depletion region near drain at the channel edge caused by the finite channel width are not taken into account by the two-dimensional simulations [1]; the 2D programs are meanwhile state of the art. Accurate investigations of the previously stated effects and the knowledge of increased current densities under certain bias conditions at the channel edge are important not only for studying the electrical device characteristics but also for aging effects [2]–[3]. A realistic physical model and suitable mathematical algorithms have been developed to simulate the previously stated three-dimensional effects.

We shall report in Chapter 2 about the physics and the mathematics on which the simulations are based. In addition we shall present the device structure and a consideration of some aspects of the oxide body of the MOSFET.

The results of our simulations carried out by MINIMOS 5 are reported in Chapter 3 and will be

discussed there, too.

2 Physical and Mathematical Aspects

The basic equations which are implemented in our MINIMOS to describe current flow in silicon differ only slightly from the conventional equations. The Poisson equation and the continuity equations for electrons and holes are 'the' established basic equations which are commonly in use. A derivation of these equations can be found in e.g. [7]. The current relations for electrons and holes are somehow different from the conventional drift-diffusion relations. They include the hot electron transport effect. Detailed information on the 'hot-electron-transport' model can be found in [6,9]. In addition to the well known boundary conditions for the Poisson equation and the continuity equations we have to implement a boundary condition for the mobilities. We set the driving force F as in (1).

$$\vec{F}_n|_{int} = 0 \quad (1)$$

If we neglect this boundary condition we get unrealistic mobilities near the interfaces. For solving the set of differential equations we apply for discretisation the box integration method after Forsythe [10] to deal with the boundary conditions of the nonrectangular simulation region. The linearized equations are solved by the SOR method and the Gauß-elimination [4],[5],[8]. The geometry of the 3D MOSFET model is given in Fig. 1. We implemented an approximation to the complete oxide-volume which can be seen in Fig. 2. The upper plane denotes the interface of the oxide to the contacts and the surrounding volume, respectively. The lower plane denotes the interface of oxide and semiconductor. The definition of the interface is quite general and can be varied in a wide range. The gate contact is filled in the middle of the upper plane, the Source and Drain contacts are on the left and right. In the middle in the gate region the distance of the upper and lower plane equals the gate-oxide thickness. The drain currents calculated by 2D and 3D simulations cannot be compared in a straight forward manner if the field oxide is nonplanar. The oxide reduces gradually the channel width which is given by the mask specifications. Therefore we introduce an effective channel width w_{eff} for the 2D current calculation instead of the given mask width. The effective channel width is calculated by (2)

$$w_{eff} = w - \frac{1}{D_{ch}} \int_0^w fox(z)|_{l/2} dz \quad (2)$$

w is the width specified by the mask, D_{ch} denotes the channel depth, $l/2$ denotes half of the channel length, $fox(z)$ is the function which describes the geometry of the channel in width direction.

3 Results and Discussion

The geometry of the investigated 3D MOSFET is given in Fig. 1: an n-channel MOSFET with an $1\mu m \times 1\mu m$ channel and gate oxide of $15nm$. For demonstrating the effects at the channel edge we select two different bias points. The first is near threshold with $U_S = U_B = 0.0V$, $U_D = 3.0V$, $U_G = 1.0V$ (the threshold voltage for this device is $U_{th} \sim 0.75V$). The potential distribution in channel length and width direction at the semiconductor/gate-oxide interface is shown in Fig. 3. (This plane penetrates into the field oxide near the contact boundary of Source and Drain.) The corresponding minority carrier distribution is given in Fig. 4. A remarkable depletion region at the drain side causes the channel charge to be smaller (under certain bias conditions) than predicted by 2D simulations. The second bias point is far above threshold $U_S = U_B = 0.0V$, $U_D = 1.0V$, $U_G = 3.0V$. The corresponding potential distribution can be seen in Fig. 5. The location of the

plane for which the distribution is drawn, is the same as at the previous bias condition. The high increase of the potential distribution out of the channel is due to the gate contact overlapping the field oxide. Also interesting is the minority carrier distribution (Fig. 6), which shows the enhanced conductivity at the semiconductor field-oxide interface. Note that only one half of the channel width is shown in Fig. 3 – Fig. 6; $-0.5\mu\text{m}$ denotes the middle of the channel width and $0.0\mu\text{m}$ the boundary of Source and Drain contacts. The effect on the device characteristics of these effects depends on the gradient of the bird's beak and the channel width. A high gradient in the field oxide shape results in high parasitic current at the channel edge; this effect is less significant for low gradients. Narrow channel devices with high gradient have much higher currents than predicted by 2D calculations while the agreement with 2D simulations is good for wide channel devices in any case. Using a low gradient in bird's beak we get a very smooth potential distribution compared to a nearly rectangular shape.

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References:

- [1] S.M. Sze, Physics of semiconductor devices, ISBN 0-471-09837-X, John Wiley & sons, 1981
- [2] S.M. Sze, VLSI-Technology, ISBN 0-07-062686-3, McGraw-Hill, 1983
- [3] T. Iizuka, K.Y. Chiu, and J.L. Moll, Double threshold MOSFETs in bird's-beak free structures, IEEE Int. Electron Device Meet., Wash., D.C., 1981, p. 380
- [4] L.A. Hageman, Franklin T. Luk, David M. Young, On the equivalence of certain iterative acceleration methods, SIAM J. NUMER. ANAL., pp 852-873, vol. 17 No. 6, Dec 1980
- [5] R.G. Grimes, D.R. Kincaid, D.M. Young, ITPACK 2A – A fortran implementation of adaptive accelerated iterative methods for solving large sparse linear systems, Report CNA-164, Center for numerical analysis, University of Texas at Austin, 1980
- [6] W. Hänsch, M. Miura-Mattausch, A new current relation for hot electron transport, Proc. NASECODE IV Conf., pp. 311-314, Boole Press, Dublin, 1985.
- [7] S. Selberherr, Analysis and simulation of semiconductor devices, ISBN 3-211-81800-6, Springer, WIEN NEW-YORK, 1984
- [8] O. Axelsson, Solution of linear systems of equations; Iterative methods, Lecture notes in mathematics 574, SMT, 1976
- [9] S. Selberherr, The status of MINIMOS, Proc. Simulation of semiconductor devices and processes, pp 2-15, Swansea, 1986
- [10] G.E. Forsythe, W.R. Wasaw, Finite Difference Methods for Partial Differential Equations. Wiley, NEW-YORK, 1960

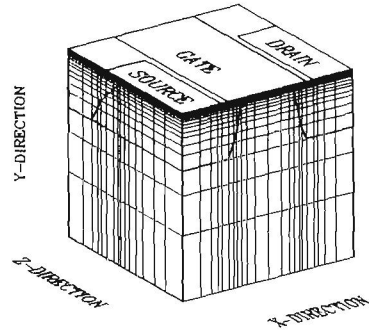


Fig.1: Perspective view of the three-dimensional MOSFET structure.

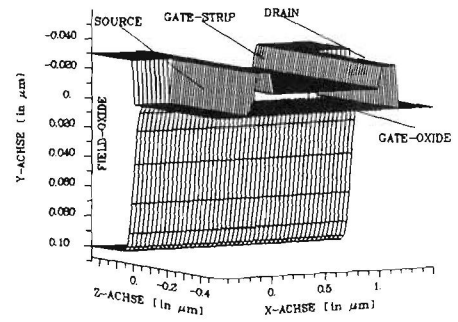


Fig.2: Oxide body of the MOSFET structure (the oxide is between the upper and lower plane).

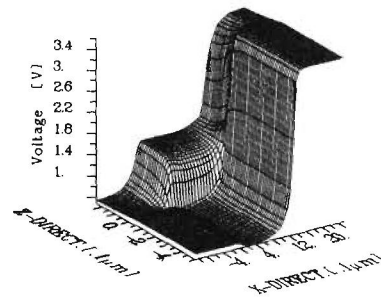


Fig.3: 3D-plot showing a detailed view of the surface potential at the channel edge along the channel length at bias $U_{DS} = 3.0V$, $U_{BS} = 0.0V$, $U_{GS} = 1.0V$.

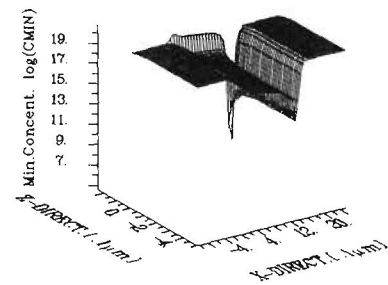


Fig.4: 3D-plot showing a detailed view of the minority carrier density at the channel edge along the channel length at bias $U_{DS} = 3.0V$, $U_{BS} = 0.0V$, $U_{GS} = 1.0V$.

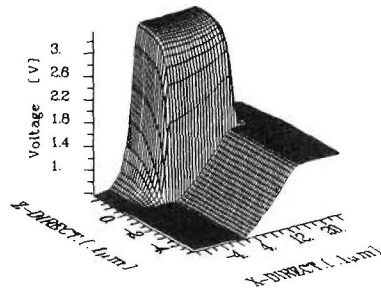


Fig.5: 3D-plot showing a detailed view of the surface potential at the channel edge along the channel length at bias $U_{DS} = 1.0V$, $U_{BS} = 0.0V$, $U_{GS} = 3.0V$.

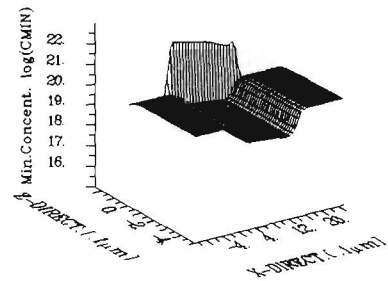


Fig.6: 3D-plot showing a detailed view of the minority carrier density at the channel edge along the channel length at bias $U_{DS} = 1.0V$, $U_{BS} = 0.0V$, $U_{GS} = 3.0V$.