

ON-RESISTANCE AND BREAKDOWN IN RESURF-DEVICES

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Abstract – One key issue for high voltage CMOS structures is the proper design of the output driver devices, which are usually lateral DMOS transistors (LDMOST). We present an analysis of a LDMOST and an ALDMOST (accumulation LDMOST) with respect to ON-resistance, punch-through and avalanche breakdown.

I – INTRODUCTION

In recent years various CMOS structures have been developed as output driver devices [1]. Especially for high voltage applications the proper design of these so called resurf devices is of particular importance.

There is a considerable number of publications about threshold voltage [2] and breakdown behaviour [3] [4] of DMOS transistors comparing experimental data with results from simulations as well as one [5] which proposes a new lateral device with semi-insulating layer to lower the ON-resistance. The aim of this paper is to show, that effects like punch-through and hot carrier induced breakdown cannot be confirmed by approximations from one-dimensional theories and require two dimensional simulations.

Our computations have been carried out with our fully two-dimensional device simulator BAMBI which solves the three semiconductor equations in a totally selfconsistent way utilizing a 'Finite Boxes' grid [6]. Effects of impact ionization are completely taken into account according to the model by Van Overstraeten [7].

We have simulated the behaviour of three different device geometries with various oxide thicknesses and doping profiles.

II – ON-RESISTANCE

The conventional LDMOS transistor has an oxide with a step. A minimum oxide thickness is requested to guarantee the voltage stability by limiting the electrostatic field in

the dielectric. This thickness also strongly influences the threshold voltage. Therefore for conventional LDMOST's a simple reduction of the oxide thickness and the application of an additional semi-insulating layer will significantly change the electrical properties of the device. We have performed a comparison between a LDMOS structure that we have investigated previously [8] and the ALDMOST. The geometry of one of our devices and the voltage distribution along the oxide above the accumulation layer for the ALDMOST in ON and OFF condition can be seen in Fig. 1. We have also analyzed a LDMOST structure assuming a constant oxide thickness of $0.2\mu\text{m}$ keeping all other geometric properties of the device. The result of the simulation has shown that even in the case of an oxide thickness of $0.4\mu\text{m}$ the ON-resistance can be reduced by a factor of about 1.4. This gain of efficiency will of course be increased if a constant oxide thickness of $0.2\mu\text{m}$ is assumed. For this geometry we could observe an improvement of the ON-resistance up to a factor of 2. It should be pointed out that the threshold voltage remains almost unchanged by this modification of geometry. In Fig. 2 and Fig. 3 the total current densities of the LDMOST of the ALDMOST (with a constant oxide thickness of $0.2\mu\text{m}$), respectively, are shown ($V_{\text{Gate}} = 15\text{V}$, $V_{\text{Drain}} = 12\text{V}$). It can clearly be seen how the current density leaks far into the drift region because of the additional bias provided by the semi-insulating layer above the depletion layer.

III – PUNCH THROUGH

We have analyzed various doping profiles as given in Table I (maximum values). The profiles are approximated by Gaussian distribution functions.

Table 1. Maximum values of doping profile

No.	$n^+ [\text{cm}^{-3}]$	$p [\text{cm}^{-3}]$	$n^- [\text{cm}^{-3}]$	$p^- [\text{cm}^{-3}]$
1	$2.0 \cdot 10^{20}$	$5.0 \cdot 10^{16}$	$3.0 \cdot 10^{15}$	$1.2 \cdot 10^{15}$
2	$2.0 \cdot 10^{19}$	$1.2 \cdot 10^{16}$	$3.0 \cdot 10^{15}$	$1.2 \cdot 10^{15}$
3	$2.0 \cdot 10^{19}$	$1.2 \cdot 10^{16}$	$3.0 \cdot 10^{14}$	$1.2 \cdot 10^{14}$
4	$2.0 \cdot 10^{20}$	$5.0 \cdot 10^{16}$	$3.0 \cdot 10^{14}$	$1.2 \cdot 10^{14}$

For the doping profile No.1-3 punch through occurs between 6V and 60V drain voltage depending on the gate voltage, for the the doping profiles No.4 no parasitic channel is build up even at 100V drain voltage. We started the simulation at -1.0V gate voltage (for numerical reasons) successively increasing the drain voltage from 0.0V. Usually a slightly negative bias at the gate contact speeds up the convergence. In this case it does not influence the behaviour of the transistor since the threshold voltage of the transistor

is larger than 6.0V. At a drain voltage of 52.0V the value for the current flow at the drain contact and the source contact raised significantly from 10^{-8} A/cm to 10^{-2} A/cm in spite of an expected breakdown voltage of more than 400.0V [3]. In Fig. 4,5 the onset of the parasitic channel is shown at 53.0V and 55.0V, respectively. One can clearly see how the total current density raises exactly at the curvature of the channel doping. The total current density is rather the same as the electron current density, the hole current flow is negligible all over the device. From one-dimensional approaches for MOSFET's [9] the punch-through could not be explained. In these calculations the space charge regions were still separated from each other. In order to demonstrate the influence of the gate voltage on punch-through the same procedure was repeated for a gate voltage of 0.0V. In this case punch-through occurred at 6.0V drain voltage. These simulations show, that this kind of transistor is highly sensitive to the design of the doping profile.

IV – AVALANCHE BREAKDOWN

We have investigated the effect of high voltage breakdown caused by impact ionization for the LDMOST and the ALDMOST. For this simulations we have varied the oxide thickness between $0.4\mu\text{m}$ and $0.1\mu\text{m}$. The doping profile No.4 was assumed throughout this investigation. Avalanche breakdown occurs in regions with large peaks in the electric field either from the drain contact through the substrate or at the p-n junction from the channel to the drift region. In our device the latter can be observed. The peaks in the electric field are reduced by the additional layer in the ALDMOST because of the uniform voltage distribution at top of the oxide. Furthermore a large amount of drift region charge can be provided, because the bias of the semi-insulating layer enhances the depletion of the drift region from the surface [10]. On the other hand the breakdown voltage will be reduced by the additional bias since the effective distance between the drain and the gate contacts is decreased by the electron accumulation in the drift region near the drain contact [3]. This means that the effective length of the drift region is reduced. From our simulations almost the same breakdown voltages for both devices have been obtained. It is about 470V and nearly independent of the oxide thickness. The difference between the values for both devices is less than 5%. In Fig. 6 and Fig. 7 the hole distributions for the LDMOST at 440V and 470V, respectively, are shown. It can nicely be observed how the hole concentration rises over the whole device, especially in the channel region. This means that the breakdown will occur by avalanching at the p-n junction to the drift region. In Fig. 8 the hole current of the LDMOST at the breakdown is shown for an applied voltage of 480V. There is a significant hole current flow from the drift region through the channel towards the source contact. Fig. 6 and Fig. 7 point out the obvious tendency of the ALDMOST to provide a lower voltage

stability than the LDMOST because the high hole concentration induced by impact ionization at the interface between the oxide under the semi-insulating layer and the semiconductor area leaks far into the drift region. This particularly holds true for an oxide thickness larger than about $0.2\mu\text{m}$. During our simulations it has been observed that this loss of voltage stability will be lowered if the oxide thickness is decreased. This means that the ALDMOST with an oxide thickness less than $0.1\mu\text{m}$ as described by [5] will exhibit almost the same breakdown voltage as the conventional LDMOST [11].

V – CONCLUSION

With respect to the ON-resistance, we have shown that the additional semi-insulating layer of the ALDMOST will indeed reduce the ON-resistance of the device, but this is strongly dependent on the oxide thickness. For structures with an oxide thickness of about $0.2\mu\text{m}$ and $0.4\mu\text{m}$ as they are proposed by S. Colak [3] the advantage will not be as high as expected. However if the oxide thickness is reduced as described in [5] the ON-resistance will be significantly lowered. This should be considered in the design of LDMOST's. If punch-through occurs, the design of the doping profile has to be changed because this type of transistor is very sensitive to it. It has been shown, that even at concentrations taken from recent publications, this effect may occur if the p-n junction – in particular if the curvature is not designed very carefully. The breakdown voltage of an accumulation lateral DMOS transistor will slightly be decreased by the additional semi-insulating layer compared to the LDMOST but according to our results not in a critical way. The lower ON-resistance of the ALDMOST is therefore a real advantage compared to the conventional LDMOST.

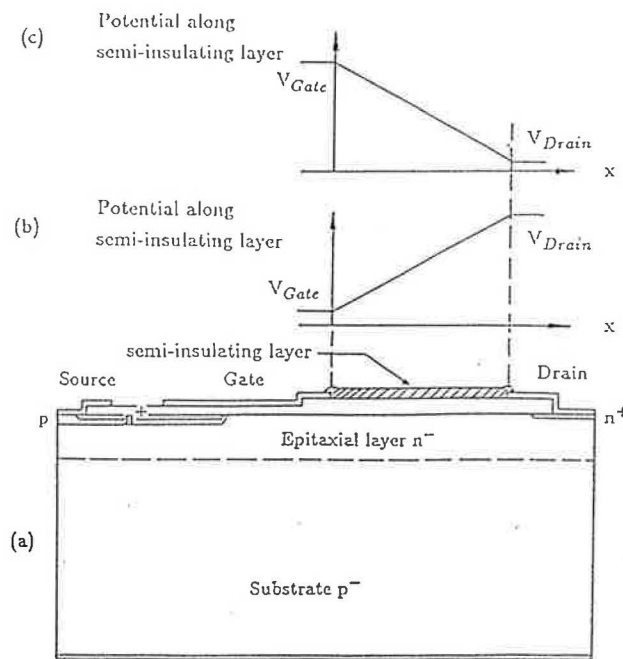
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Acknowledgement

This work has been supported by SIEMENS AG, Villach, Austria, by the SIEMENS AG Research Laboratories at Munich, Germany, by DIGITAL EQUIPMENT CORP. at Hudson, U.S.A., and by the 'Fonds zur Förderung der wissenschaftlichen Forschung', project S43/10. The authors are indebted to Prof. H. Pötl for many helpful discussions.



- (a) Geometry
- (b) Voltage distribution along SIPOS layer in OFF-condition
- (c) Voltage distribution along SIPOS layer in ON-condition

Fig. 1 Geometry

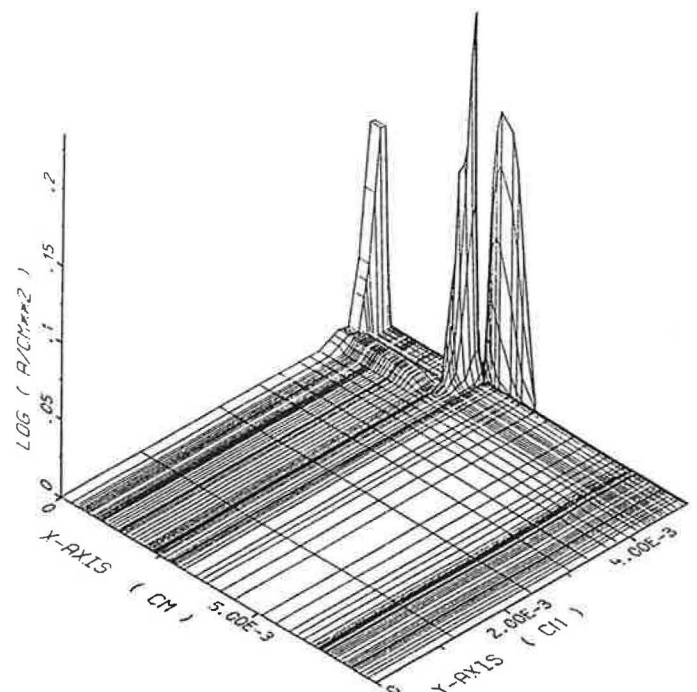


Fig. 8 Hole current density LDMOST

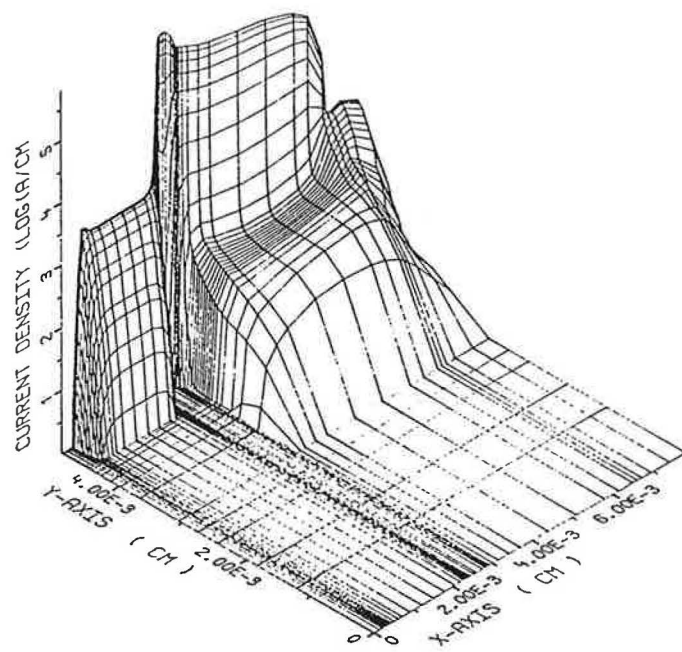
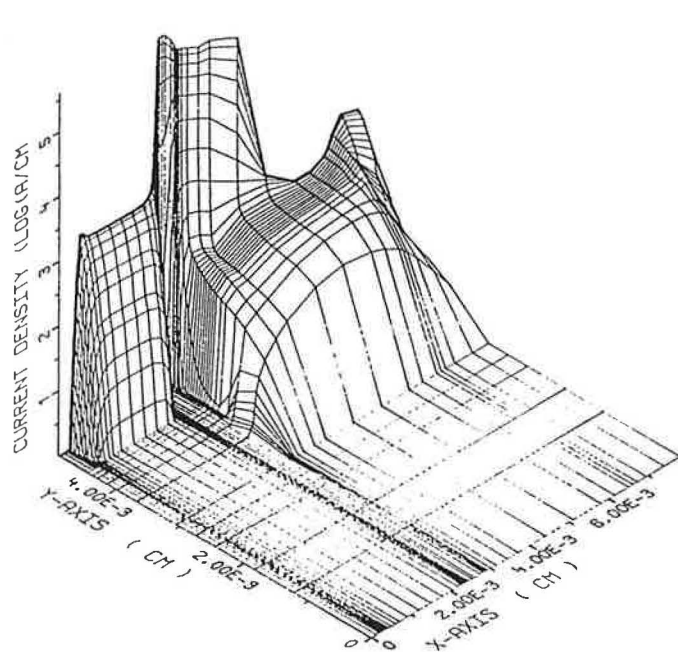


Fig. 2,3 Total current density of the LDMOST and the ALDMOST

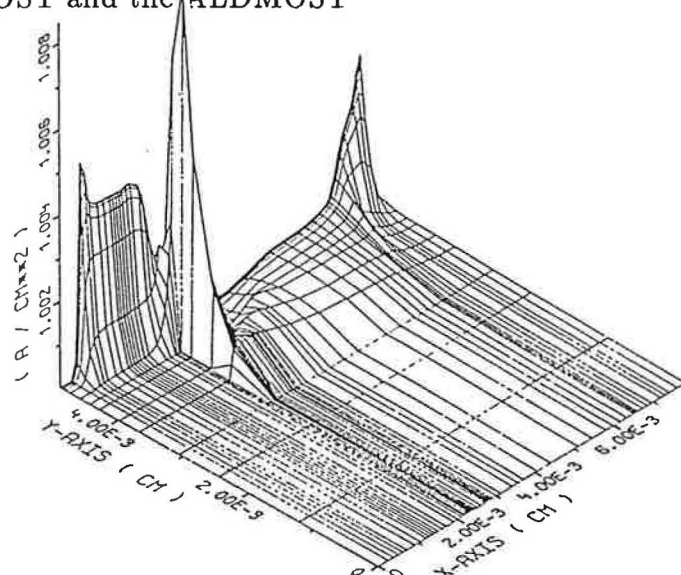
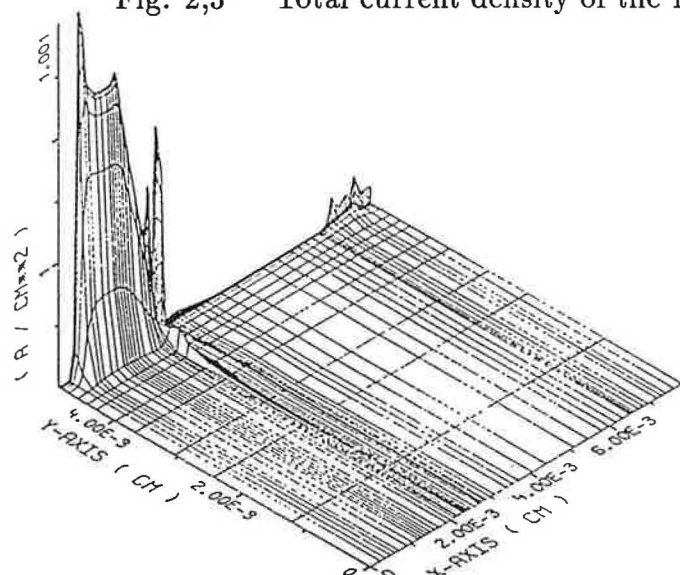


Fig. 4,5 Onset of the parasitic channel of the LDMOST at 53V and 55V

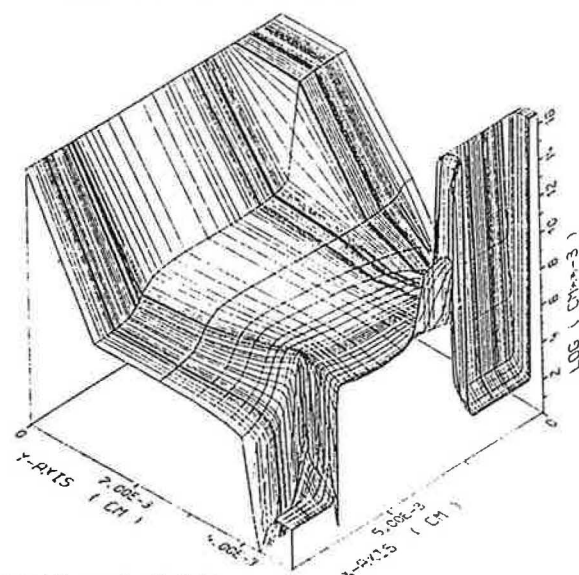
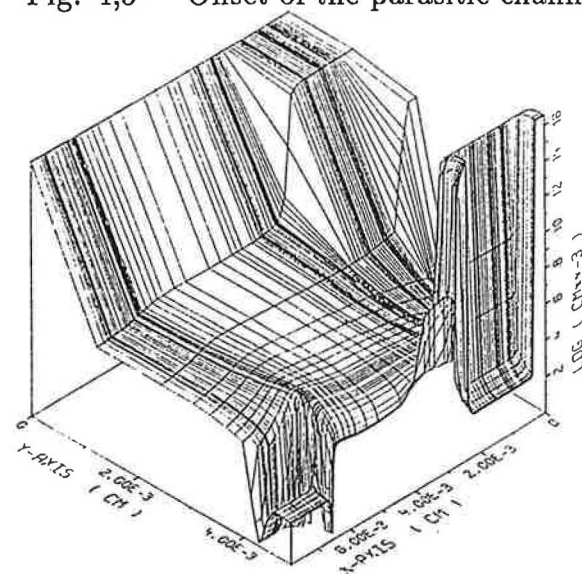


Fig. 6,7 Hole distribution of the LDMOST at 440V and 470V