DEVICE AND PROCESS MODELING

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ABSTRACT

This contribution is intended to present highlights of the state of the art in numerical process and device modeling. Special emphasis will be put on three-dimensional simulation for submicron applications. As one particular example results for ion implantation into a three-dimensional trench are presented. The recent refinements to carrier transport models in semiconductor devices are discussed. As a particular example for three-dimensional device simulation the influence of the shape of the field-oxide in width direction is discussed. Some remarks on the computational requirements are given.

1. INTRODUCTION

In the development of miniaturized devices for integrated circuits and particularly their technology, the demand for models being capable to predict the various processing steps of device fabrication on the one hand and the electrical behavior of devices on the other hand is growing dramatically due to the tight coupling of electrical device effects with the doping profile.

Due to lack of space it is not possible here to give an extensive overview about all internationally successful activities on process and device modeling. Therefore, the paper has been restricted to the description of some interesting and recently performed investigations.

2. PROCESS MODELING

Device fabrication processes can be principally categorized into two groups. Lithographic processes which serve patterning purposes and doping processes which determine for a given structure the electrical properties of the intended semiconductor device. The first group consists of deposition and etching with spatial selectivity in order to enable structuring. It may be viewed as a fixed process which provides flexibility in layout. The second group is composed of ion implantation, diffusion, thermal oxidation and epitaxy.

Ion implantation doubtless is a central point in the fabrication of miniaturized semiconductor devices. Therefore, as one particular example for three-dimensional process modeling, results for ion implantation into a three-dimensional trench are presented in this section. In order to demonstrate the necessity of three-dimensional process

simulation tools additionally the two-dimensional solution is shown as comparison.

The calculations have been performed with a two- and three-dimensional program package for the simulation of ion implantation based on the "Monte Carlo"-method including some additional features to increase computational efficiency [13]. The first step in the development of that software tool was a two-dimensional model of ion implantation which accounted for position dependent lateral moments [14]. With this model the analytical description of ion implantation profiles has been essentially improved by specifying a modification of the Gaussian distribution function. The benefit of the classical concept of using distribution functions lies in the low computer resources required. The enormous drawback is the restriction of the applicability to simple geometries only. To investigate ion implantation in connection with arbitrary geometries a rigorous simulation method has to be applied.

Fig. 1 and Fig. 2 show the geometry of the investigated trench for the two- and three-dimensional case, respectively. The three-dimensional trench has a square cross-section. The substrate material is silicon in which boron ions are implanted with an energy of 25 keV.

Fig. 3 and Fig. 4 show the concentration of dopants in a quasi three-dimensional representation as a result of the two- and three-dimensional simulation, respectively. The result of the three-dimensional simulation (Fig. 4) is displayed for the symmetry plane between front wall and back wall (see Fig. 2). The surface of the wafer is located on the left side of the top of the drawings. The vertical axis denotes the logarithm of the boron concentration divided by the implantation dose. The left axis lies parallel to the shady side of the trench and represents the depth whereas the right axis is parallel to the bottom of the trench and represents the width.

Regarding Fig. 3 one can see the considerable concentration on the shady side which is just about a factor five smaller than the concentration on the sunny side. A comparison between Fig. 3 and Fig. 4 shows on the one hand that the concentrations on the sunny sides are rather the same, but on the other hand the concentrations on the shady side differ about a factor two. Such an inaccuracy of the two-dimensional simulation certainly is not acceptable as small variations of a doping profile persistently influence the electrical behavior of a semiconductor device.
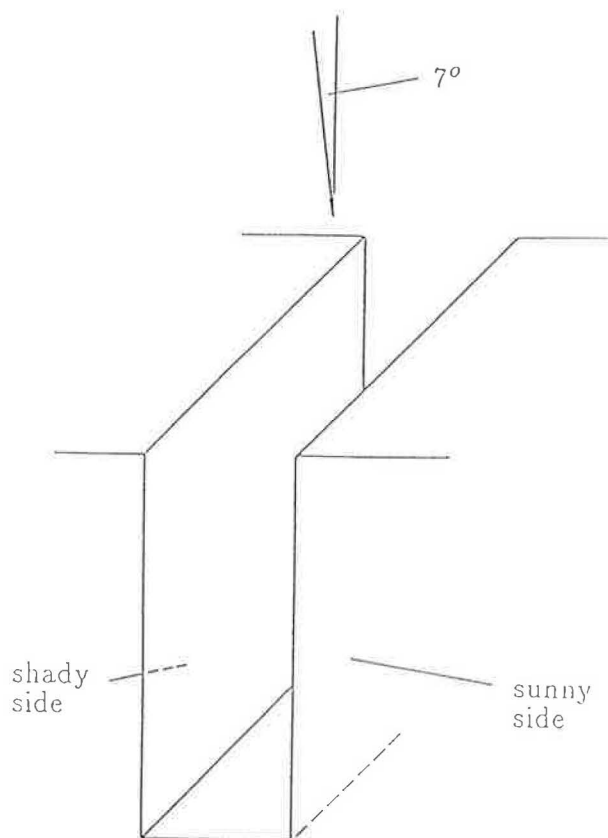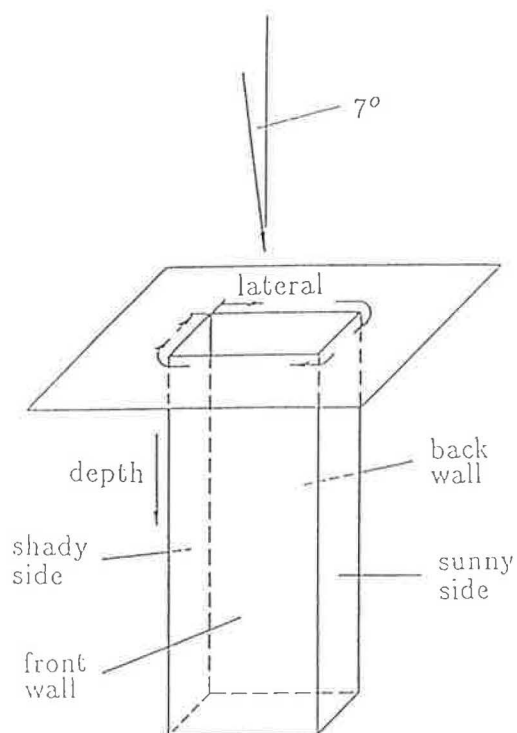
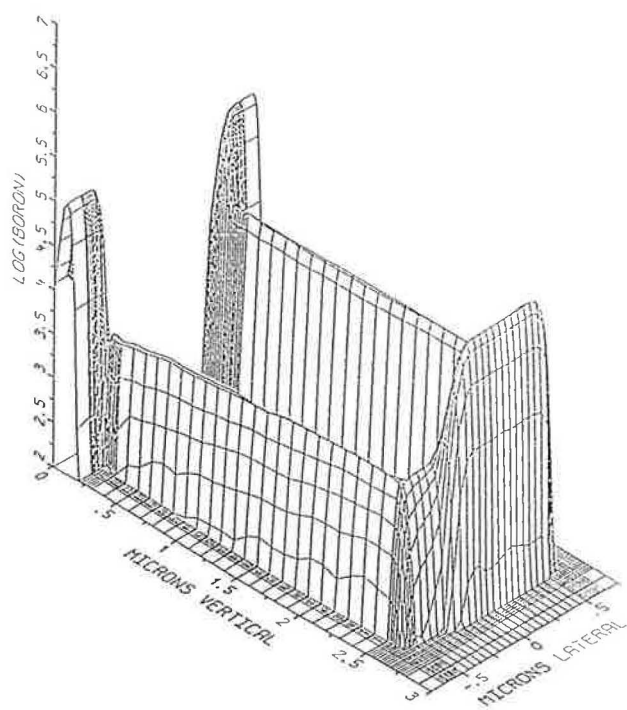Fig.1: Two-dimensional trench

Fig.2: Three-dimensional trench

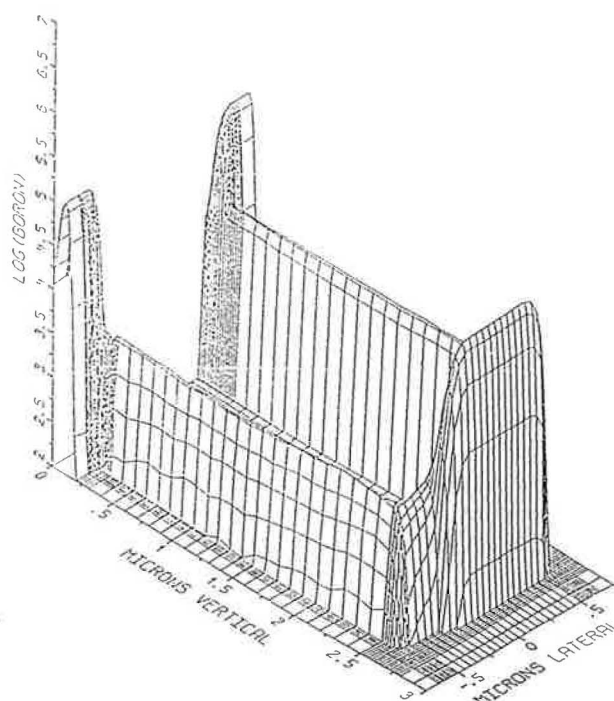Fig.3: Concentration of dopants in the 2-D trench

Fig.4: Concentration of dopants in the symmetry plane of the 3-D trench

3. DEVICE MODELING

Since Silicon VLSI Technology has evolved to a standard that hundreds of thousands transistor devices are integrated in a single chip it has become crucial to understand even second order effects of basic device operation. The application of numerical simulation packages for the development of prototype devices is therefore a basic requirement.

Device Modeling based on the self-consistent solution of the well known fundamental semiconductor equations [22] dates back to the famous work of Gummel in 1964 [10]. Since then numerical device modeling has been applied to nearly all important devices. Today there are ongoing arguments in the scientific community whether the semiconductor equations are adequate to describe transport in submicron devices. Particularly the current relations (1) and (2) which are the most complex equations out of the set of the basic semiconductor equations undergo strong criticism in view of, for instance, ballistic transport [12], [19]. Their derivation from more fundamental physical principles is indeed not at all straightforward. They appear therefore with all sorts of slight variations in the specialized literature and a vast number of papers has been published where some of their subtleties are dealt with. The interested reader is referred for, e.g., [4], [6], [9], [24]. Anyway, recent investigations on ultra short MOSFET's [20] do not give evidence that it is necessary to waive these well established basic equations for silicon devices down to feature sizes in the order of 0,1 microns [25].

$$\vec{J}_n = q \cdot \mu_n \cdot n \cdot \left(\vec{E} + \frac{1}{n} \cdot \mathrm{grad}\left(n \cdot \frac{k \cdot T_n}{q} \right) \right) \quad (1)$$

$$\vec{J}_p = q \cdot \mu_p \cdot p \cdot \left(\vec{E} - \frac{1}{p} \cdot \mathrm{grad}\left(p \cdot \frac{k \cdot T_p}{q} \right) \right) \quad (2)$$

In this section recent refinements to the model of the carrier temperatures are discussed. Furthermore, the influence of the shape of the field-oxide in width direction is presented as a particular example for three-dimensional device simulation.

3.1 MODELING CARRIER TEMPERATURES

To describe carrier heating properly one has to account for local carrier temperatures $T_{n,p}$ in the current relations (1) and (2). This can be achieved by either solving energy conservation equations self consistently with the basic transport equations, or by using a model obtained by series expansions of the solution to the energy conservation equations [11]. We believe that the latter is sufficient for silicon devices. For the electronic voltages we have (3) as an approximation. Confirming theoretical investigations can be found in [1]:

The carrier mobilities $\mu_{n,p}^{LIS}$ in (3) include three scattering mechanisms: lattice scattering [3], [7], [18], ionized impurity scattering [8] and surface scattering [21]. The mobilities $\mu_{n,p}^{LISE}$ additionally take the effect of velocity saturation into account [3], [16], [17]. A detailed model for the carrier mobilities can be found in [23].

$$Ut_{n,p} = \frac{k \cdot T_{n,p}}{q} = Ut_o + \frac{2}{3} \cdot \tau_{n,p}^\epsilon \cdot \left(v_{n,p}^{sat} \right)^2 \cdot \left(\frac{1}{\mu_{n,p}^{LISE}} - \frac{1}{\mu_{n,p}^{LIS}} \right) \quad (3)$$

The energy relaxation times $\tau_{n,p}^\epsilon$ are in the order of 0,5 picoseconds and just weakly temperature dependent [5]. They should however be modeled as functions of the local doping concentration as motivated by the following reasoning. The product of carrier mobility times electronic voltage which symbolizes a diffusion coefficient must be a decreasing function with increasing carrier voltage (see also [5]). Its maximum is attained at thermal equilibrium. Relation (4) must therefore hold.

$$\mu_{n,p}^{LISE} \cdot Ut_{n,p} \leq \mu_{n,p}^{LIS} \cdot Ut_o \quad (4)$$

Note that models for carrier diffusion coefficients are not required in the basic current relations (1), (2). Substituting (3) into (4) and rearranging terms one obtains relation (5) for the energy relaxation times.

$$\tau_{n,p}^\epsilon \leq \frac{3}{2} \cdot Ut_o \cdot \frac{\mu_{n,p}^{LIS}}{\left(v_{n,p}^{sat} \right)^2} \quad (5)$$

In the actual version of MINIMOS [26], the energy relaxation times are modeled on the basis of (5) with a fudge factor γ in the range $[0,1]$ and a default value of 0,8.

$$\tau_{n,p}^\epsilon = \gamma \cdot \frac{3}{2} \cdot Ut_o \cdot \frac{\mu_{n,p}^{LIS}}{\left(v_{n,p}^{sat} \right)^2} \quad (6)$$

For vanishing doping one obtains the maximum energy relaxation times which are at 300K $\tau_n^\epsilon = 4,44 \cdot 10^{-13}$s, $\tau_p^\epsilon = 2,24 \cdot 10^{-13}$s and at liquid nitrogen temperature $\tau_n^\epsilon = 8,82 \cdot 10^{-13}$s, $\tau_p^\epsilon = 8,68 \cdot 10^{-13}$s.

3.2 MOSFET SIMULATION

This section presents three-dimensional effects of MOSFET's due to the nonplanar nature of the field-oxide body. The investigations have been carried out by MINIMOS 5 [26] which accounts for all three spatial dimensions. Three-dimensional effects like threshold shift for small channel devices, channel narrowing and the enhanced conductivity at the channel edge have been successfully modeled. Similar investigations leading to matching results have been performed in [2], [15].
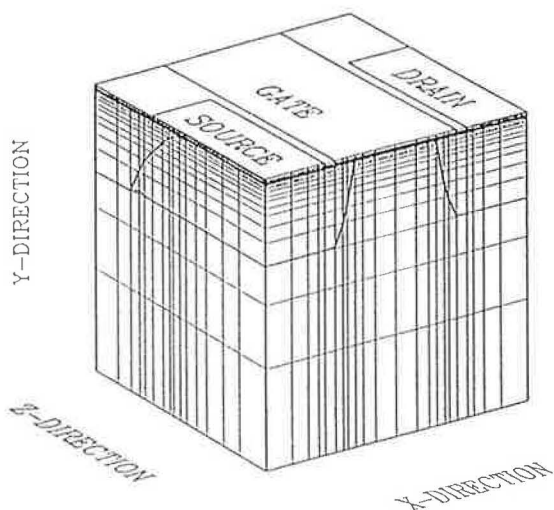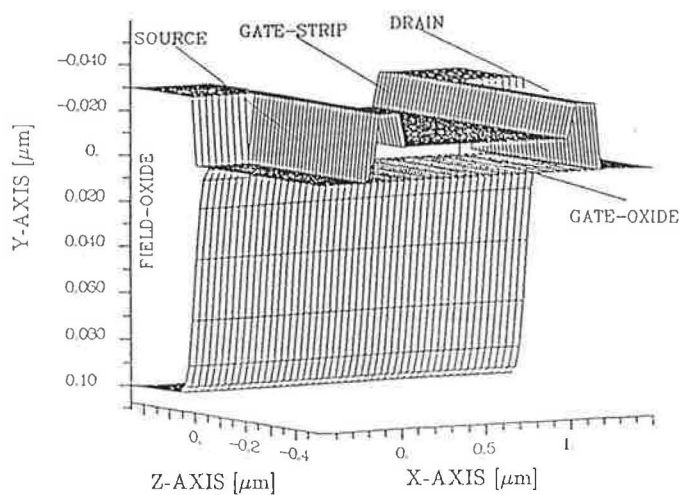
Fig.5: 3-D MOSFET structure

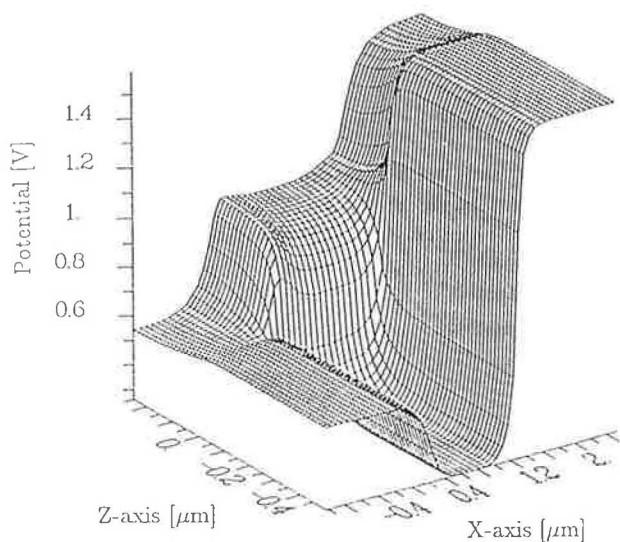Fig.6: Oxide body of the structure

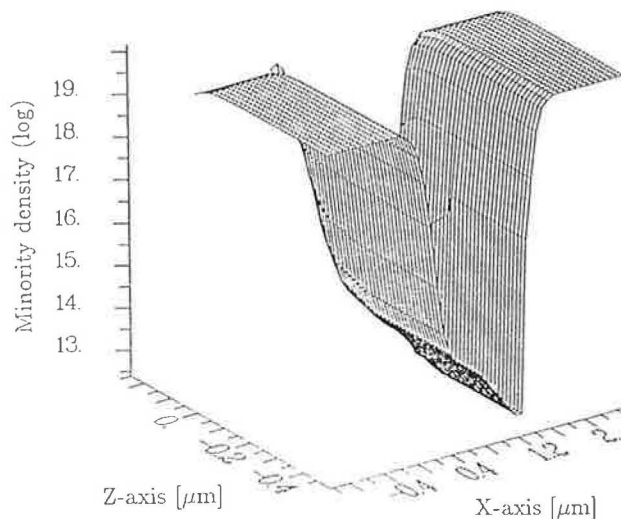Fig.7: Detailed view of the surface potential at bias $U_{GS} = 0.5$V

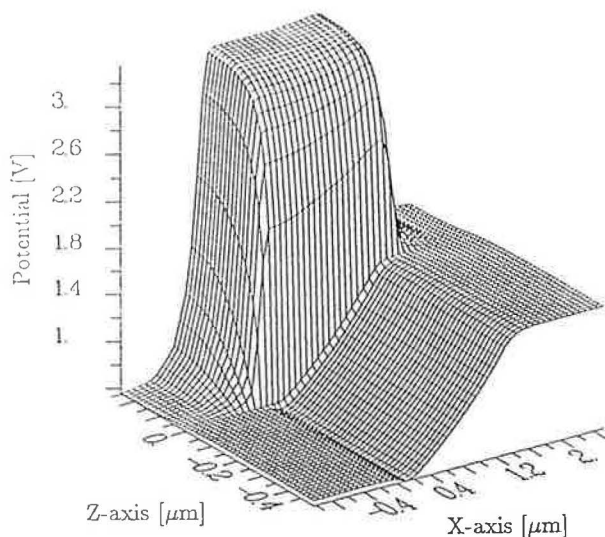Fig.8: Detailed view of the minority carrier density at bias $U_G = 0.5$V

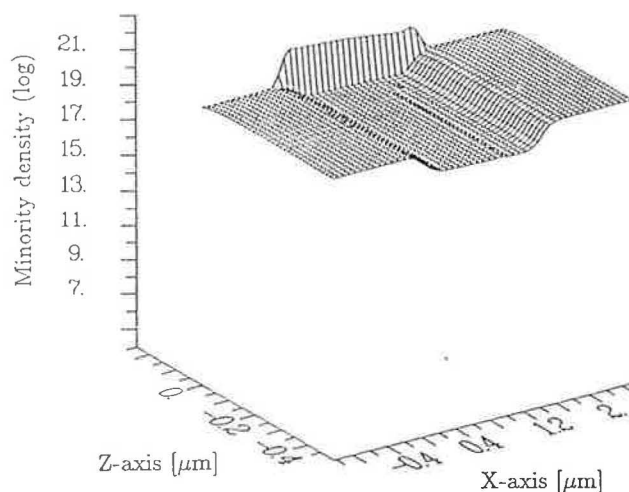Fig.9: Detailed view of the surface potential at bias $U_{GS} = 3.0$V

Fig.10 Detailed view of the minority carrier density at bias $U_G = 3.0$V

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The geometry of the investigated 3-D MOSFET is given in Fig. 5: an n–channel with an $1\mu m$ x $1\mu m$ channel and gate oxide of 15nm. The oxide body of the analyzed structure can be seen in Fig. 6 (note that the oxide is between the upper and the lower plane).

In order to demonstrate the effects at the channel edge we select two different bias points. The first is near threshold with $U_S = U_B = 0.0V$, $U_{DS} = 1.0V$, $U_{GS} = 0.5V$ (the threshold voltage for this device is $U_{th} \sim 0.75V$). The potential distribution in channel length and width direction at the semiconductor/gate-oxide interface is shown in Fig. 7. (This plane penetrates into the field-oxide near the contact boundary of source and drain.) The corresponding minority carrier distribution is given in Fig. 8. A remarkable depletion region at the drain side causes the channel charge to be smaller (under certain bias conditions) than predicted by 2-D simulations.

The second bias point is far above threshold $U_S = U_B = 0.0V$, $U_{DS} = 1.0V$, $U_{GS} = 3.0V$. The corresponding potential distribution can be seen in Fig. 9. The location of the plane which the distribution is drawn for, is the same as at the previous bias condition. The high increase of the potential distribution out of the channel is due to the gate contact overlapping the field-oxide. Also interesting is the minority carrier distribution (Fig. 10) which shows the enhanced conductivity at the semiconductor field-oxide interface. Note that only one half of the channel width is shown in Fig. 7 – Fig. '10; $-0.5\mu m$ denotes the middle of the channel width and $0.0\mu m$ the boundary of source and drain contacts. The consequence on the device characteristics of these effects depends on the gradient of the "bird's beak" and the channel width. A high gradient in the field-oxide shape results in high parasitic current at the channel edge; this effect is less significant for low gradients. Narrow channel devices with high gradient have much higher currents than predicted by 2-D calculations while the agreement with 2-D simulations is good for wide channel devices in any case. Using a low gradient in bird's beak yields a very smooth potential distribution compared to a nearly rectangular shape.
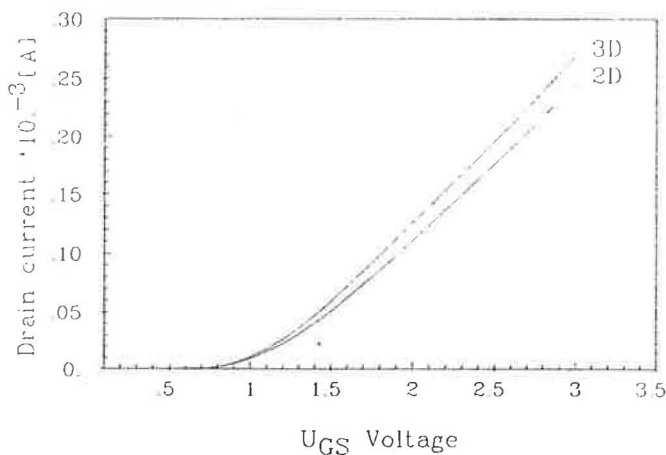

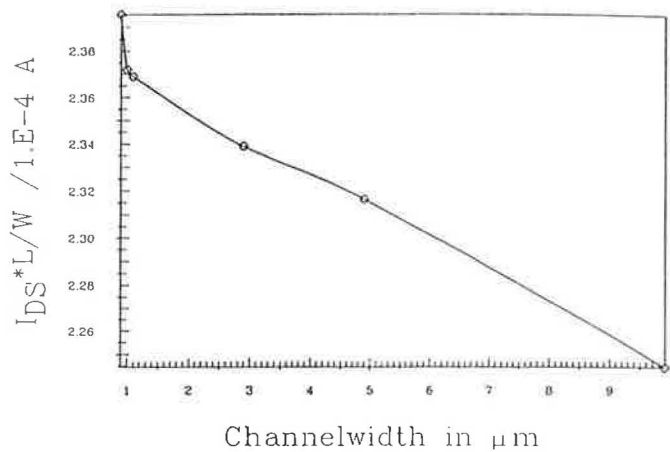Fig.12: Measured dependence of the drain current

Fig. 11 shows a comparison of two-dimensional and three-dimensional characteristics for $U_{DS} = 1V$ and a rectangular approximated field-oxide.

The dependence of the drain current of n-channel devices with weak field implantation on the channel width is shown in Fig. 12. The marked points indicate the measured transistors which have been investigated at the same bias conditions where the enhanced conductivity can be seen.

4. CONCLUSION

The shrinking dimensions of the elements of integrated circuits require suitable process and device models in physics and mathematics for accurate simulation. Although two-dimensional software tools are adequate for many questions the advanced VLSI technology leads to serious problems which can be investigated rigorously by fully three-dimensional simulations only.

One important drawback of three-dimensional process and device modeling is the enormous amount of required computer resources. The calculations presented in this paper have been carried out on a host computer with 64 MB core memory capable of one million floating point operations per second (DIGITAL VAX 8800). In order to obtain the results of the ion implantation into the trench (section 1) about 10^8 particles had to be investigated. The two-dimensional simulation took 0.8 CPU-hours while the three-dimensional one required about 5 CPU-hours. A straight forward Monte Carlo simulation, i.e. without the special acceleration methods implemented, would have used about 800 CPU-hours. The situation for three-dimensional device modeling is rather similar: the three-dimensional simulation of a MOSFET at difficult bias conditions may require up to 100 CPU-hours. These demands on computational resources are only acceptable if — as is the case — results can be deduces which cannot be gained by cheaper investigations. Furthermore, one should keep in mind the enormous improvement of the price/performance ratio in computing, which can presently be estimated by a factor of 1000 per 9 years.

Fig.11: 2-D and 3-D characteristic at bias $U_{DS} = 1.0V$

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