GaAs–MESFET Simulation with MINIMOS

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ABSTRACT

This paper presents the implementation of models allowing the simulation of GaAs MESFETs with MINIMOS 5 – an integrated 2D and 3D device simulator for silicon MOSFETs. Models for the Schottky contact and possible device geometries are shown. As a result a simulation of a T–gate MESFET is presented.

INTRODUCTION

GaAs devices have become of increasing importance for high speed analog and digital circuits since their introduction in 1970. GaAs FET amplifiers, oscillators, mixers, etc. are widely used in microwave applications whereas very fast digital circuits have been developed based on GaAs MESFET logic. Because of the physical properties of GaAs, the MESFET is the mostly used device for those applications. Moreover, MESFET offer some advantages over MOSFETs. Mobilities are higher, since carriers are transported deep in the bulk and no minority carrier storage effects take place, which results in faster switching speeds. Furthermore, MESFETs are less radiation sensitive, because of the missing gate oxide.

With the increasing relevance of MESFETs the need for efficient simulation of these devices has become apparent. Using the framework and capabilities of MINIMOS 5 which is our integrated two– and three–dimensional device simulator for silicon MOSFETs with transient and small signal analysis capabilities we implemented models allowing the simulation of MESFETs and models for GaAs as substrate material.

BASIC EQUATIONS

MINIMOS 5 solves the basic semiconductor equations in two or three space dimensions. The set of equations consists of the Poisson equation (1) and the continuity equations for electrons (2) and holes (3):

$$div\ grad\ \psi = \frac{q}{\varepsilon} \cdot (n - p - C) \tag{1}$$

$$div\ J_n = q \cdot R \tag{2}$$

$$div\ J_p = -q \cdot R \tag{3}$$

The current relations for electrons and holes differ slightly from the classical formulations, which can be found in [1]:

$$J_n = q \cdot \mu_n \cdot n \cdot (-grad\ \psi + \frac{1}{n} \cdot grad\ (U_{t_n} \cdot n)) \tag{4}$$

$$J_p = q \cdot \mu_p \cdot p \cdot (-grad\ \psi - \frac{1}{p} \cdot grad\ (U_{t_p} \cdot p)) \tag{5}$$

In equation (4) and (5) the second term accounts for carrier heating effects by field dependent modelling of the carrier temperatures. Detailed information about the derivation of these formulations can be found in [2]. These equations have proven to work well for silicon MOSFETs and MESFETs

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with gate length down to 0.1 microns. For GaAs devices the classical drift–diffusion approach has proven to be suitable only for relatively long devices whereas for very small feature sizes non-stationary transport effects can become apparent which are usually claimed to be properly modelled by either Monte Carlo methods or hydrodynamic equations based on higher moments of the Boltzmann equation [3]. We have evidence that our current relations (4) and (5) in connection with appropriate models for the carrier voltages U_{tn} and U_{tp} push the limit of applicability of these enhanced drift-diffusion equations significantly towards smaller feature sizes. Final investigations which give a sound proof will have to be carried out.

BOUNDARY CONDITIONS

To allow the simulation of MESFETs with MINIMOS a boundary condition for the Schottky gate contact had to be implemented.

A Dirichlet boundary condition is used for the potential ψ

$$\psi = \psi_{app} - \psi_s \tag{6}$$

where ψ_{app} is the applied voltage and ψ_s is the surface potential at the interface. ψ_s depends on the barrier height ϕ_B in the following way

$$\psi_s = \phi_B - \frac{E_g}{2} - \frac{kT}{2q} \cdot ln\left(\frac{N_v}{N_c}\right) \tag{7}$$

where the barrier height is allowed to change in case of large reverse bias

$$\Delta\phi_B = \sqrt{\frac{qE}{4\pi\varepsilon_s}} \tag{8}$$

to account for the image force lowering. ε_s is the permittivity of the semiconductor, E the electric field at the interface, E_g the bang gap of the semiconductor and N_c and N_v the density of states of the conduction and the valence band.

Implicit boundary conditions are implemented for the carrier densities n and p by using boundary conditions for the current densities J_n and J_p perpendicular to the interface.

$$J_n = -q \cdot v_n \cdot (n - n_0) \tag{8}$$

$$J_p = q \cdot v_p \cdot (p - p_0) \tag{9}$$

n_0 and p_0 are the equilibrium carrier concentrations at the surface defined by

$$n_0 = n_i \cdot exp\left(-\frac{\psi_s}{U_T}\right) \tag{10}$$

$$p_0 = n_i \cdot exp\left(\frac{\psi_s}{U_T}\right) \tag{11}$$

The surface recombination velocities v_n and v_p are modeled current dependent.

$$v_{n,p} = v_d + \sqrt{\frac{2\,k\,T}{m^*_{n,p}\,\pi\,\eta_{n,p}}} \cdot \frac{exp\left(-v_d^2\left(\frac{m^*_{n,p}\,\eta_{n,p}}{2\,k\,T}\right)\right)}{1 + erf\left(v_d\sqrt{\frac{m^*_{n,p}\,\eta_{n,p}}{2\,k\,T}}\right)} \tag{12}$$

Here m^* is the effective mass for either electrons or holes, $\eta_{n,p}$ is an 'non-ideality' factor, which accounts for changes in the band structure at the interface and v_d is the drift velocity defined by

$$v_d = \frac{J_{n,p}}{q \cdot (n,p)} \tag{13}$$

Equation (12) is bounded from above by the saturation velocity of the semiconductor v_{sat} which limits v_d and from below by the condition $v_d = 0$ which gives

$$v_{n,p} = \sqrt{\frac{2\,k\,T}{m^*_{n,p}\,\pi\,\eta_{n,p}}} \tag{14}$$

This formulation gives a higher recombination velocity at large forward biased Schottky contacts which avoids an unrealistic accumulation of carriers and so leads to better results in those cases. A detailed derivation of this model can be found in [4].

PROCESS MODELS

To provide user-friendly use of MINIMOS for GaAs simulation various process parameters like implantation statistics and diffusion coefficients for various dopants have been implemented based on Monte Carlo calculations with PROMIS [5].

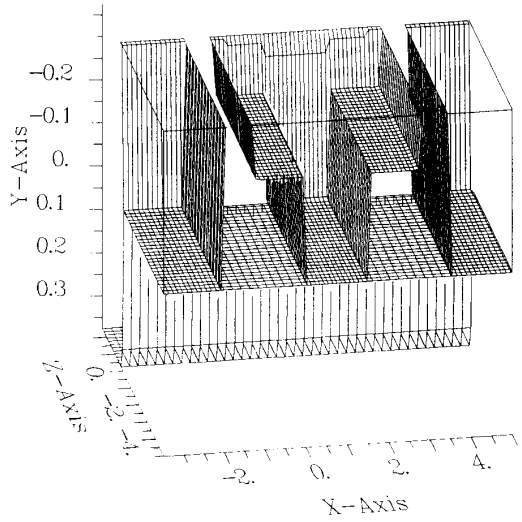

Fig. 1

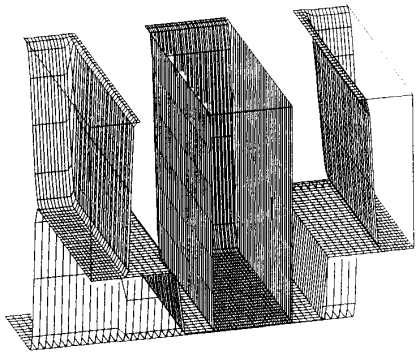

Fig. 2

These parameters can easily set by the user via the input deck, to define source/drain and/or channel implantation.Moreover, the user has the possibility to use one- or two-dimensional data from a process simulator.

DEVICE GEOMETRIES

For an efficient simulation of GaAs devices it is necessary to simulate different nonplanar geometries like recessed gate or T-gate MESFETs. Various enhancements had to be made to allow the simulation of these nonplanarities with MINIMOS 5 which was able to simulate nonplanar MOS structures [6]. Fig. 1 shows shape of the source, the gate and the drain contact of a T-gate MESFET whereas one can see a recessed gate device with the recessed semiconductor surface in Fig. 2. The figures are not on the same scale in all three space dimensions.

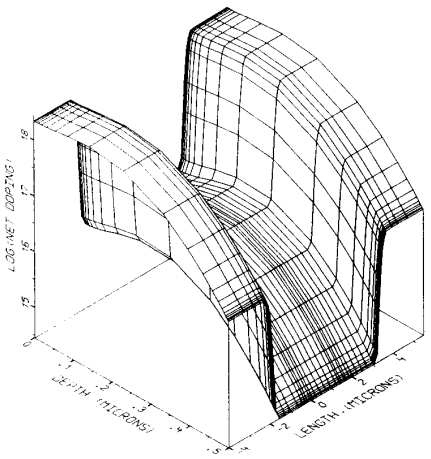

Fig. 3

RESULTS

As an example an n-channel T-gate MESFET with 1.5 micron gate length was simulated. The shape of contacts with the dimensions of the T-gate is shown in Fig. 1. The thickness of the semiconductor layer is 0.5 micron. The Schottky barrier height is 0.6 V. The device is biased with -0.2 V on gate and 1.5 V on drain. The device has a source/drain implantation with a peak concentration of $2 \cdot 10^{18}$ and a channel implantation with a peak of 10^{16}, which is shown in Fig. 3. In Fig. 4 one can see the potential distribution in the device. In front the shape of the T-gate can be seen. The electron concentration of the transistor is shown in Fig. 5. The depletion region reaches 0.2 microns into the layer. Deeper in the bulk one can see a considerable channel with a carrier concentration in the order of 10^{16}. The drain current in this case is 0.36 mA for 10.0 microns gate width.

ACKNOWLEDGEMENT

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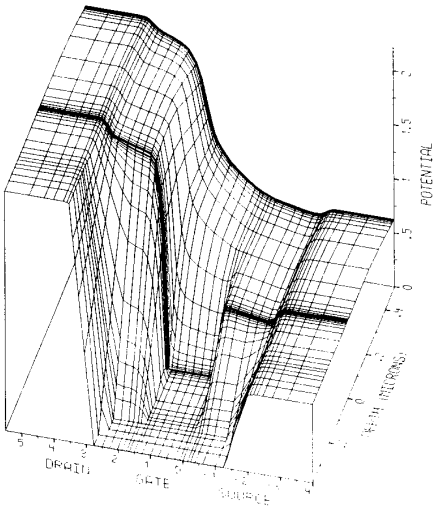

Fig. 4

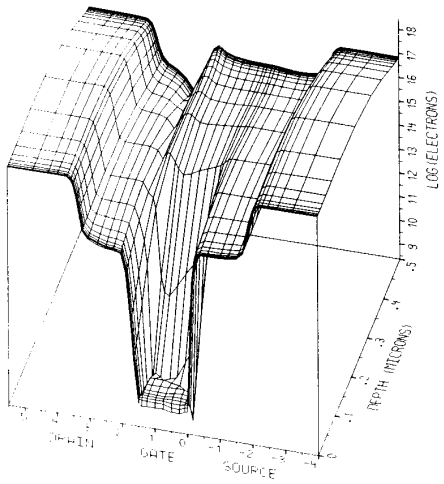

Fig. 5