LOW TEMPERATURE MOS DEVICE MODELING

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ABSTRACT

The state of the art in self-consistent numerical low temperature MOS modeling is reviewed. The physical assumptions which are required to describe carrier transport at liquid nitrogen temperature are discussed. Particular emphasis is put on the models for space charge (impurity freeze-out), carrier mobility (temperature dependence of scattering mechanisms at a semiconductor-insulator interface) and carrier generation-recombination (impact ionisation). The differences with regard to the numerical methods required for the solution of low temperature models compared to room temperature models are explained. Typical results obtained with the simulator MINIMOS 4 are presented.

INTRODUCTION

Device Modeling based on the self-consistent solution of fundamental semiconductor equations dates back to the famous work of Gummel in 1964. However, the first application of this rigorous style of modeling for problems at low ambient temperature (usually liquid nitrogen temperature) has first been carried out by Gaensslen et al. about twelve years later in 1976 [9]. The main reason for this delay cannot only be seen in the lesser demands for low temperature simulation. Today not only supercomputers are made for operation at liquid nitrogen temperature, like the ETA-10 [8], but also microprocessors, cf. [7]. The primary reason for the fairly poor status in fully numerical low temperature device modeling stems from considerably increased difficulties regarding physical assumptions and implementation for the numerical solution.

PHYSICAL ASPECTS

The model for hot carrier transport used in any numerical device simulation is based on the well known fundamental semiconductor equations (1)-(5). There are ongoing arguments in the scientific community whether these equations are adequate to describe transport in submicron devices. Particularly the current relations (4) and (5) which are the most complex equations out of the set of the basic semiconductor device equations undergo strong criticism in view of, for instance, ballistic transport [13], [17]. Their derivation from more fundamental physical principles is indeed not at all straightforward. They appear therefore with all sorts of slight variations in the specialized literature and a vast number of papers has been published where some of their subtleties are dealt with. Anyway, recent investigations on ultra short MOSFET's [18] do not give evidence that it is necessary to waive these well established basic equations for silicon devices down to feature sizes in the order of 0.1 microns [23].

$$\mathrm{div}(\varepsilon \cdot \mathrm{grad}\,\psi) = -\rho \tag{1}$$

$$\mathrm{div}\,\vec{J_n} - q \cdot \frac{\partial n}{\partial t} = q \cdot R \quad , \qquad \mathrm{div}\,\vec{J_p} + q \cdot \frac{\partial p}{\partial t} = -q \cdot R \tag{2),(3}$$

$$\vec{J_n} = q \cdot \mu_n \cdot n \cdot \left(\vec{E} + \frac{1}{n} \cdot \mathrm{grad}\left(n \cdot \frac{k \cdot T_n}{q}\right)\right) \tag{4}$$

$$\vec{J_p} = q \cdot \mu_p \cdot p \cdot \left(\vec{E} - \frac{1}{p} \cdot \mathrm{grad}\left(p \cdot \frac{k \cdot T_p}{q}\right)\right) \tag{5}$$

These equations include a set of parameters which have to be appropriately modeled in order to describe the various transport phenomena qualitatively and quantitatively correctly.

Poisson's equation (1) requires a model for the space charge ρ which makes use of only the dependent variables ψ, n, p and material properties. The well established approach for this model is to sum up the concentrations with the adequate charge sign multiplied with the elementary charge:

$$\rho = q \cdot (p - n + N_D^+ - N_A^-) \tag{6}$$

Here the first difference between room temperature and low temperature simulation becomes apparent. The doping concentration is usually assumed to be fully ionized at room temperature which intuitively does not hold for low temperature analysis. The classical way to describe partial ionization is based on the formulae (7).

$$N_D^+ = \frac{N_D}{1 + 2 \cdot \exp\left(\frac{E_{fn} - E_D}{k \cdot T}\right)} \quad , \quad N_A^- = \frac{N_A}{1 + 4 \cdot \exp\left(\frac{E_A - E_{fp}}{k \cdot T}\right)} \tag{7}$$

E_D and E_A are the ionization energies of the respective donor and acceptor dopant. A quite complete list of values can be found in [25]. These ionization energies are recommended to be modeled doping dependent in [6], however, it seems not to be important for MOSFET's regarding our experience. The Fermi levels E_{fn} and E_{fp} have to be appropriately related to the dependent variables.

$$\frac{E_{fn} - E_D}{k \cdot T} = G_{1/2}\left(\frac{n}{N_c}\right) + \frac{E_c - E_D}{k \cdot T} \quad , \quad \frac{E_A - E_{fp}}{k \cdot T} = G_{1/2}\left(\frac{p}{N_v}\right) + \frac{E_A - E_v}{k \cdot T} \tag{8}$$

$G_{1/2}(x)$ is the inverse Fermi function of order 1/2 defined with

$$G_{1/2}\left(\frac{2}{\sqrt{\pi}} \cdot \int_0^\infty \frac{\sqrt{y}}{1 + e^{y-x}} \cdot dy\right) = x \tag{9}$$

N_c and N_v are the density of states in the conduction band and the valence band, respectively. The ratio of the density of states depends only on the ratio of the effective masses of electrons and holes. The product can be fitted to measured data of the intrinsic concentration requiring only models, e.g. [9], for the effective masses and the energy gap. With these two relations it is straightforward to compute the numerical values for the density of states. A full derivation of this partial ionization model can be found in [22].

The next set of physical parameters to be considered carefully for low temperature simulation consists of the carrier mobilities μ_n and μ_p in (4) and (5). The temperature dependence of the various scattering effects is reviewed in [12], [21], [22]. Particular emphasis has to be put on surface scattering which we model with an expression suggested by Seavey [20]:

$$\mu_{n,p}^{LIS} = \frac{\mu_{n,p}^{ref} + (\mu_{n,p}^{LI} - \mu_{n,p}^{ref}) \cdot (1 - F(y))}{1 + F(y) \cdot \left(\frac{S_{n,p}}{S_{n,p}^{ref}}\right)^{\alpha_{n,p}}} \tag{10}$$

$$\mu_n^{ref} = 638 \frac{\text{cm}^2}{\text{Vs}} \cdot \left(\frac{T}{300\text{K}}\right)^{-1.19} \quad , \quad \mu_p^{ref} = 160 \frac{\text{cm}^2}{\text{Vs}} \cdot \left(\frac{T}{300\text{K}}\right)^{-1.09}$$

$$F(y) = \frac{2 \cdot \exp\left(-\left(\frac{y}{y^{ref}}\right)^2\right)}{1 + \exp\left(-2 \cdot \left(\frac{y}{y^{ref}}\right)^2\right)} \quad , \quad S_n = \max\left(0, \frac{\partial \psi}{\partial y}\right) \quad , \quad S_p = \max\left(0, -\frac{\partial \psi}{\partial y}\right)$$

S_n^{ref} is assumed to be $7 \cdot 10^5 \frac{\text{V}}{\text{cm}}$; S_p^{ref} is $2.7 \cdot 10^5 \frac{\text{V}}{\text{cm}}$ and y^{ref} is 10nm.

The formulae for surface scattering are definitely not the ultimate expressions. They just fit quite reasonably experimental observations. Other approaches with the same claim can be found in, e.g., [3], [14], [16]. A u-shaped mobility behavior as found in [4] has not been synthesized because we believe in a different origin than surface scattering for this experimental observation.

To describe carrier heating properly one has to account for local carrier temperatures $T_{n,p}$. This can be achieved by either solving energy conservation equations self consistently with the basic transport equations, or by using a model obtained by series expansions of the solution to the energy conservation equations [11]. We believe that the latter is sufficient for silicon devices, cf.[1]. The energy relaxation times $\tau_{n,p}^{\epsilon}$ are in the order of 0.5 picoseconds and just weakly temperature dependent [5]. They should be modeled as functions of the local doping concentration with (11). In MINIMOS γ is a fudge factor in the range [0, 1] and a default value of 0.8.

$$\tau_{n,p}^{\epsilon} = \gamma \cdot \frac{3}{2} \cdot Ut_o \cdot \frac{\mu_{n,p}^{LIS}}{\left(v_{n,p}^{sat}\right)^2} \tag{11}$$

A comment should be made on the model for the impact ionization rate. It still seems, though under heavy dispute of the scientific community, that the old Chynoweth formulation of impact ionization can be used quite satisfactorily for device simulation. Our model with temperature dependent coefficients is given in [22].

NUMERICAL ASPECTS

Almost none of the many device simulation programs which have proven their usefulness for room temperature simulations can be directly applied to low temperature applications. The primary reason for this is the scaling of carrier concentrations with all thereby induced consequences. Briefly sketched: to scale as frequently performed the intrinsic carrier concentration to unity, which contributes to change the basic semiconductor equations into a dimensionless form very convenient for computer implementation. Due to the fact that the intrinsic carrier concentration at liquid nitrogen temperature is in the order of 10^{-20}cm^{-3} it is obviously not applicable for scaling in this case, since for instance an impurity concentration of 10^{20}cm^{-3} would then be scaled to 10^{40}. To scale the maximum impurity concentration to unity as recommended in, e.g., [15] is also not feasible, since the scaled intrinsic concentration would be in the order of 10^{-40}. A way out of this dilemma is to use the concentration C_s defined by (12) for scaling.

$$C_s = \sqrt{4.8 \cdot 10^{22}\text{cm}^{-3} \cdot n_i} \tag{12}$$

The magic concentration in (12) is the number of silicon atoms per cubic centimeter. It serves as an absolute upper limit for the maximum possible concentration of any type. At 300K temperature $C_s = 2.58 \cdot 10^{16}\text{cm}^{-3}$, at 77K temperature $C_s = 3.51 \cdot 10^{1}\text{cm}^{-3}$. This scaling equilibrates the relevant concentrations and thus is optimal for avoiding fatal floating point underflow or overflow exceptions.

A GLIMPSE OF RESULTS

Results of investigations with MINIMOS 4 about submicron n-channel enhancement mode MOSFET's at room and liquid nitrogen ambient temperature are presented. A single drain technology designed with a 3/4 micron coded channel length (0.39 micron metallurgical channel length) has been analyzed where the geometric channel length has been shrunk to 0.51 micron (0.15 micron metallurgical channel length). The gate oxide thickness is 9nm. Similar investigations for a lightly doped drain technology can be found in [22].

Fig.1 shows the simulated subthreshold characteristics for two different drain biases (UD=0.1V, UD=2V, UB=0V) at room and liquid nitrogen temperature. The subthreshold slope is obviously much steeper at liquid nitrogen temperature with about 25mV/decade compared to 95mV/decade at room temperature. The improvement of the slope is almost as good as 3.9 the ratio of 300K/77K. The shift of the subthreshold characteristics

between low and high drain bias due to primarily drain induced surface barrier lowering is about 50mV larger at 77K. A larger influence of drain induced barrier lowering at lower temperature is in contradiction with the sound results of [27].

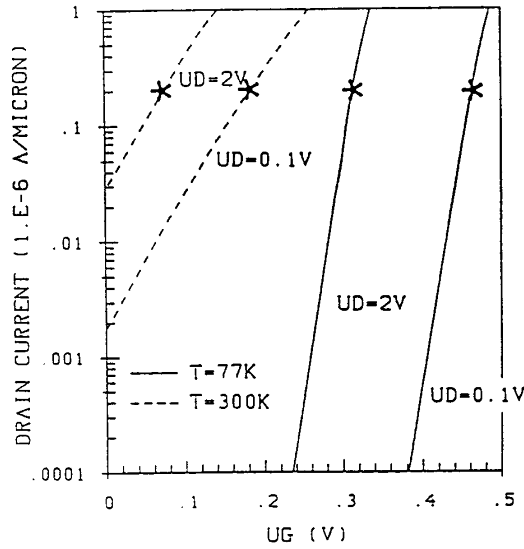

Fig.1: Simulated Subthreshold Characteristics. The asterisks indicate the respective threshold voltages.

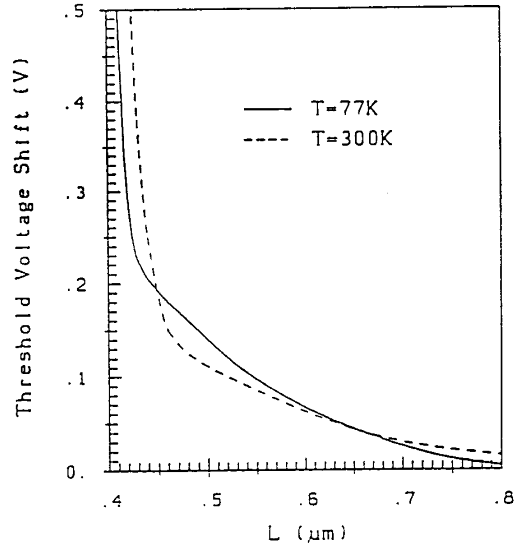

Fig.2: Drain Bias Induced Threshold Voltage Shift Versus Gate Length

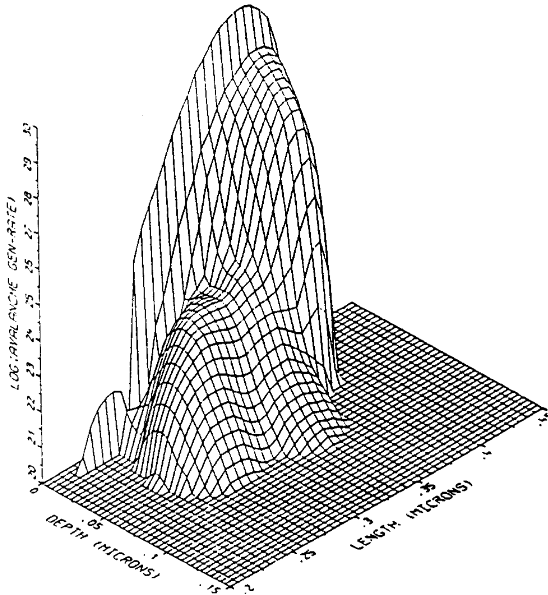

Fig.3: Impact Ionization Rate at 77K

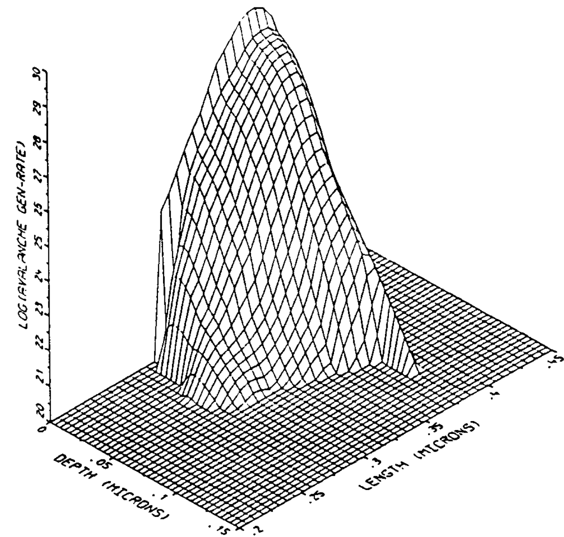

Fig.4: Impact Ionization Rate at 300K

To get insight the drain bias induced threshold voltage shift has been computed as a function of channel length (Fig.2). One can nicely see that the functional behavior is caused by two overlapping phenomena with a knee at a channel length of 0.43μm at 77K and 0.46μm at 300K. Detailed investigations have brought up several interacting causes. One is partial freeze-out of acceptors in the bulk below the channel which leads to an increase of built-in potential and thus to increasing depletion widths with decreasing temperature [10], [26]. The second cause is the formation of a sort of parasitic channel by impact ionization which has also been reported in [19].

Taking current output for the same gate drive as measure of device quality, the low temperature operation resulted in approximately 50% improvement. Similar results have been experimentally obtained (cf.[24]). This improvement decreases with shrinking channel length as observed in [18].

The impact ionization rates at a bias of UG=2V, UD=2V are shown in Fig.3 and Fig.4. The peak concentration which occurs in both cases at the surface is almost two orders of magnitude higher for low temperature operation. The substrate current to drain current ratio is increased by a factor of 5.2 which is fairly high for n-channel devices [2].

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