Measurement and simulation of degradation effects in high voltage DMOS devices

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Abstract — One of the main constraints for the long-term stability of any kind of integrated circuit technology consists in device degradation. The effect of hot electron induced degradation is a threat to MOSFET reliability when scaling to submicron dimensions. Nevertheless this effect has to be taken into account in high voltage analog MOS circuits as used in telecommunications as well. Various measurements and simulations have been performed in order to improve the behavior of n-channel high voltage DMOS transistors and to analyze the effects responsible for the degradation of these devices.

Introduction

The power supply in most VLSI circuits is 5 Volt. Scaling down the device feature sizes to submicron dimensions, the electric fields will increase to very high values. This may result in breakdown and degradation effects. Degradation effects play an important role also in high voltage devices as used in telecommunication equipment. Especially in n-channel transistors hot electrons are injected into the oxide and cause device degradation.

We present a comparison of measurements and simulations. The simulated results have been obtained with the two-dimensional device simulator BAMBI which can account for fixed charges in the insulator.

Hot electron and hole generation takes place in high field regions particularly in connection with steep doping gradients [1]. Oxide charges generated by hot carriers [2] influence the current flow in the drift region of the device [3]. The distribution of carriers trapped by oxide defects depends on the previous biasing of the device. Oxide charges are time variant in position and maximum value. Thereby they result in time variant I-V curves changing the device characteristics.

Degradation of n-channel DMOS transistors

The results of the analysis of submicron MOS transistors are not directly applicable to high voltage n-channel DMOS devices. In Fig. 1 a slightly idealized DMOS structure is shown, the measured real device is too complex for efficient 2D simulation.

For some experiments symmetric device structures must be used [4]. Thus the effects of fixed charges near drain or source (in case of reverse biasing) cannot be observed. For simplicity reasons fast interface states and mobility degradation near the interface between silicon and insulator are not included in our simulations, because the influence of these effects is negligible compared to the oxide charges [1], [5].

In Fig. 2 the measured I-V curve is shown. The measurements from 0V to 40V have

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been performed before stress, the measurements from 0V to 100V after stress becoming stable after 10 minutes of operating.

The device is designed for a maximum voltage of 120V. This means that the applied voltages should not really provide stress to the structure. Applying a gate voltage of -30V for 12 hours with 90V at drain the electrical behavior changes again as it can be seen in Fig. 3 (lines up to 100V are before applying the high negative gate voltage). Applying again a high negative gate voltage (-40V) the I-V characteristic changes again slightly as it can be seen in Fig. 4 (I-V curves with higher drain current represent the initial condition). In Fig. 5 changes in the characteristics can be observed applying a high positive gate voltage (+30V) with 40V at drain and limiting the drain current to 10μA. The curves up to 100V are the "stable" degraded initial conditions. This means that the carrier distribution in the oxide changes again. Additional electrons are injected into the insulator even for low drain voltages so under normal operating conditions all these effects makes the device unfit for use.

Due to the special geometry the measurement of substrate currents is impossible. In comparison to standard MOS structures [6] no threshold voltage shift can be observed. Thereby it can be concluded that no electrons are injected from the channel region into the oxide. The results of our two-dimensional simulations show high electric fields at the beginning of the drift region. The peak of the field ($3.5 \cdot 10^6$ V/cm) in Fig. 6 indicates that the geometry layout is not appropriate. Degradation occurs because obviously the carriers in this region have enough energy to cross the energy barrier to the oxide. In a modified geometry the values of the field are lowered significantly (Fig. 7). This improvement has been achieved by reducing the overlap of the drain metallization and the drift region. Simulations as proposed by [1] verify the presence of trapped electrons as additional charges in the oxide. Contrarily to MINIMOS we have assumed a two-dimensional Gaussian charge distribution. The maximum of this function lies at the beginning of the drift region. The change of the carrier mobility is not investigated.

In Fig. 8 and Fig. 9 the current densities are shown without and with additional oxide charges, respectively. There is a significant difference in the drift region between these two simulations, the current flow in Fig. 8 is located near the interface. In Fig. 9 the current flow is forced away from the interface by the oxide charges.

In Fig. 10 different simulated I-V curves without charges and with two different peak values of the Gaussian charge distribution in the oxide are shown. These calculated results have essentially qualitative character because only little information is available about the values and the distribution of the oxide charges. For the simulation of hot electron injection no accurate models are available [3], [4].

Conclusion

We have measured and simulated the behavior of a high voltage DMOS device to identify the regions where hot electrons are injected into the insulator. The simulated results provide information where to improve the layout of these devices in order to avoid high electric fields near the oxide. Our analysis shows that it is possible to locate critical regions of devices even without simulating the degradation mechanisms itself [2], [5].

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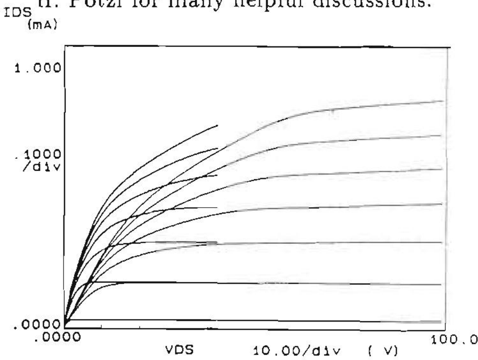

Fig.2 I-V curve with and without (up to 40V) degradation

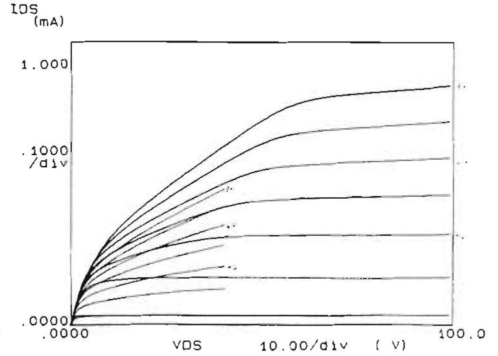

Fig.3 I-V curve before and after 12 hours with −30V at gate

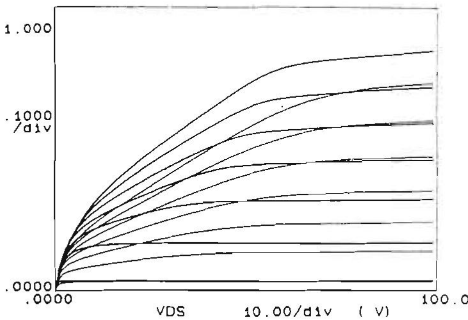

Fig.4 12 hours with $V_{GS}=-40V$, $V_{DS}=90V$

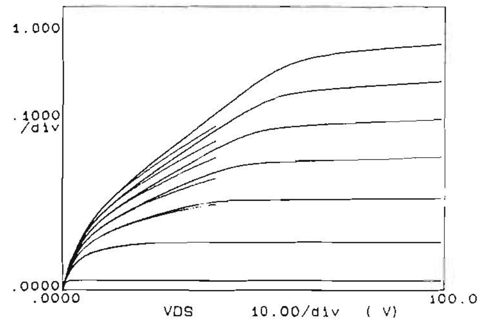

Fig.5 30 minutes with $V_{GS}=+30V$, $I_{DS} = 10\mu A$

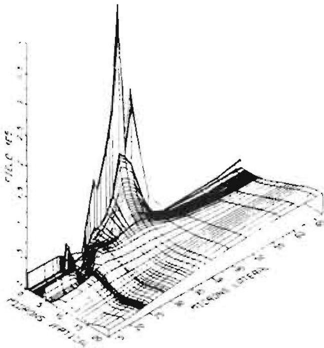

Fig.6 Field distribution of a DMOS transistor

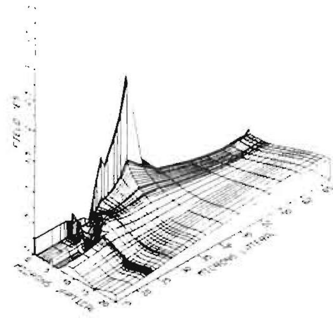

Fig.7 Field distribution of a DMOS transistor with improved geometry

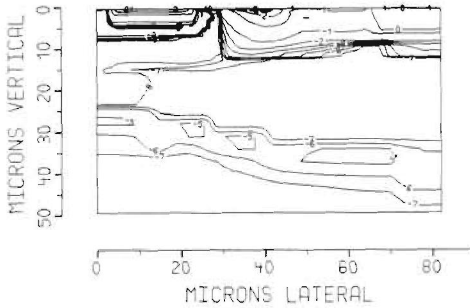

Fig.8 Current density without oxide charges

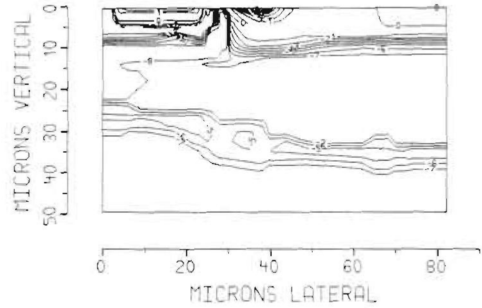

Fig.9 Current density with oxide charges

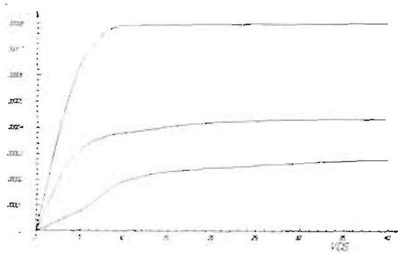

Fig.10 Simulated I-V curve with different oxide charges

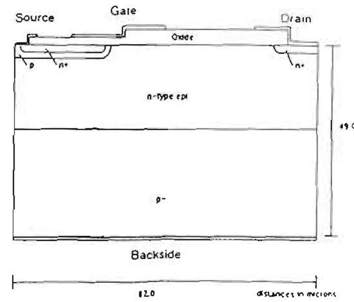

Fig.1 simplified geometry of a DMOS transistor

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