

SIMULATION OF GaAs POWER AND LOW NOISE MICROWAVE DEVICES WITH MINIMOS

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Abstract

In this paper the current status of GaAs MESFET simulation using an enhanced version of the device simulator MINIMOS is summarized. An overview of the physical models for the carrier mobilities, the Schottky contact, the semi-insulating substrate and the different generation/recombination mechanisms is given. Furthermore, the built-in process models, which allow an easy determination of the active doping profiles, are outlined. The applicability of this program to the development and optimization of modern GaAs MESFETs is shown by comparing experimental and simulated data.

1 Introduction

Today GaAs devices are used in a wide field of integrated circuits ranging from high frequency amplifiers in private satellite TV receivers to applications in digital circuits of next generation supercomputers (CRAY-3) [11]. The development of such complicated circuits requires the use of simulation programs at all stages from the fabrication processes to the layout design of the integrated circuit. In this respect the physical simulation of electrical properties of the single transistor plays a key role in reducing both cost and time in designing prototype devices.

Using the framework of MINIMOS 5 [23], a program which was originally developed as a two-dimensional simulator for planar silicon MOSFETs [17], physical models allowing the simulation of GaAs MESFETs were implemented. The comparison of measurements and simulations of both ion-implanted MESFETs fabricated using a SIEMENS SAGFET process [6] and recessed gate types based on epitaxially grown substrates revealed the most critical physical effects which have to be taken into account for successful simulations [13].

2 Physical Models

The carrier transport model in MINIMOS is based on the well known fundamental semiconductor equations:

$$\operatorname{div}(\epsilon \operatorname{grad} \psi) = -\rho \quad (1)$$

$$-q \cdot \frac{\partial n}{\partial t} + \operatorname{div} \vec{J}_n = q \cdot R \quad (2)$$

$$q \cdot \frac{\partial p}{\partial t} + \operatorname{div} \vec{J}_p = -q \cdot R \quad (3)$$

$$\vec{J}_n = q \cdot \mu_n \cdot n \left(-\operatorname{grad} \psi + U_t \cdot \frac{1}{n} \cdot \operatorname{grad} n \right) \quad (4)$$

$$\vec{J}_p = q \cdot \mu_p \cdot p \left(-\operatorname{grad} \psi - U_t \cdot \frac{1}{p} \cdot \operatorname{grad} p \right) \quad (5)$$

Using proper models [18] for the space charge ρ , the generation/recombination mechanisms R and the carrier mobilities for electrons and holes $\mu_{n,p}$ this model has proven to be adequate for the multidimensional simulation of a multitude of devices. Models for these quantities, which are suitable to describe the electrical behaviour of GaAs MESFETs, will be described in the following sections.

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	μ^0 [cm^2/Vs]	μ^{min} [cm^2/Vs]	C^{ref} [cm^{-3}]	α
n	8000	0	$1 \cdot 10^{17}$	0.5
p	380	50	$3.23 \cdot 10^{17}$	0.4956

Table 1: Mobility parameters for GaAs

2.1 Carrier Mobilities in GaAs

The model of the carrier mobilities $\mu_{n,p}$, which are the basic transport parameters in (1)–(5), has to take into account several scattering mechanisms. Lattice scattering ($\mu_{n,p}^L$), which can be modelled by a simple power law with $\gamma_n = 1$ and $\gamma_p = 2$ at room temperature [15], and ionized impurity scattering ($\mu_{n,p}^{LI}$) are the two most important mechanism, which determine the electrical conductivity of the active layer in the device at low fields. These two mechanism can be fitted very well to experimental data using the following formulae

$$\mu_{n,p}^L = \mu_{n,p}^0 \left(\frac{T}{300K} \right)^{-\gamma_{n,p}}; \quad \mu_{n,p}^{LI} = \mu_{n,p}^{\text{min}} + \frac{\mu_{n,p}^L - \mu_{n,p}^{\text{min}}}{1 + \left(\frac{C}{C_{n,p}^{\text{ref}}} \right)^{\alpha_{n,p}}} \quad (6)$$

where C denotes the total number of ionized impurities. The default values for the parameters in MINIMOS are shown in Tab. 1.

Electron velocity saturation in GaAs is usually modelled by empirical formulae [18][24], which reproduce the characteristic shape of the velocity-field curve with its peak and the region of negative differential mobility. However, we use a more physically motivated model, a reduced twoband formulation, which was first suggested by Käsweber and Hänsch [7][10]. A detailed derivation of this model can be found in [7] and [13].

The effect of velocity saturation on the hole mobility μ_p^{LIF} can be described by

$$\mu_p^{LIF} = \frac{\mu_p^{LI}}{1 + \frac{\mu_p^{LI} \cdot F}{v_p^{\text{sat}}}}; \quad F = \left| \text{grad } \psi + U_t \cdot \frac{1}{p} \cdot \text{grad } p \right| \quad (7)$$

where F denotes the driving force. The value of the saturation velocity v_p^{sat} is $1.5 \cdot 10^7$ cm/s [14], which results in noticable velocity saturation at fields in the order of several 10 kV/cm.

2.2 Schottky Boundary Conditions

A Schottky contact is modelled by applying a Dirichlet boundary condition for the potential ψ . Implicit boundary conditions for the carrier concentrations n and p at the contact are introduced by modelling the current densities $J_{n,p}$ perpendicular to the surface [12]. The model for the Schottky gate plays a crucial role in cases where the gate current is not negligible compared to the drain current. In particular, for enhancement mode devices, operating conditions with a forward biased gate contact are important. In analytical diode models [22] an ideality factor n_{ID} is used to describe the deviations of real diode characteristics from an ideal diode at forward bias. This ideality factor can easily be obtained from measurements and is mostly known for a given technology. By reformulating the boundary condition for the current densities as in (8), one can include the ideality factor, which results in a very accurate quantitative description of the forward biased gate diode, as will be shown in the result section.

$$J_n = -q \cdot v_r \cdot \left[n \cdot \exp \left(-m \cdot \frac{\psi_{app}}{U_T} \right) - n_0 \right]; \quad m = 1 - \frac{1}{n_{ID}} \quad (8)$$

Here ψ_{app} and v_r denote the applied potential and the surface recombination velocity at the contact. n_0 is the equilibrium carrier concentration at the contact.

2.3 Surface and Substrate

In GaAs MESFETs surface and substrate properties strongly affect the effective thickness of the conducting channel. The presence of surface states tends to pin the fermilevel in the middle of the bandgap. This results in the formation of a depletion layer and therefore reduces the effective channel thickness. Moreover this depletion layer plays an important role in determining the onset of avalanche breakdown

as has been shown in [2]. This effect is accounted for by including fixed charges at the semiconductor surface into the simulation [2].

Modern GaAs technologies use semi-insulating material as substrate, which exhibits a resistivity that is high enough to achieve a good device isolation and low parasitic capacitances. This semi-insulating material is usually obtained by the compensation of residual shallow dopants by the intrinsic deep levels (EL2) or by the addition of extrinsic deep level dopants (e.g. Chromium). These deep levels in the substrate strongly affect the potential barrier at the active layer – substrate interface and therefore the electron concentration in the substrate [13]. In the stationary case the fraction of occupied traps f_T of a given trap concentration N_T with energy level E_T can be modelled by [9][19]:

$$f_T = \frac{\tau_p n + \tau_n p_r}{\tau_p (n + n_r) + \tau_n (p + p_r)} \quad (9)$$

$\tau_{n,p}$ are the electron and hole lifetimes at the deep trap level which are calculated by

$$\tau_{n,p} = \frac{1}{\sigma_{n,p} \cdot v_{th,n,p} \cdot N_T} \quad (10)$$

where $\sigma_{n,p}$ denote the capture cross sections of electrons and holes at the deep trap level and $v_{th,n,p}$ are the thermal velocities of electrons and holes. The reference concentrations n_r and p_r are defined by

$$n_r = N_c \cdot \exp\left(\frac{E_T - E_c}{kT}\right); \quad p_r = N_v \cdot \exp\left(\frac{E_v - E_T}{kT}\right) \quad (11)$$

The recombination rate due to the deep level is calculated by

$$R_T = \frac{n p - n_i^2}{\tau_p (n + n_r) + \tau_n (p + p_r)} \quad (12)$$

The electrically active trap concentration must be included in the calculation of the space charge ρ in the Poisson equation (1) and the recombination due to the deep level gives a contribution to the net generation/recombination rate R in both continuity equations (2) and (3). Considering both a deep donor trap (N_{dD}, f_{dD}, R_{dD}) and a deep acceptor trap (N_{dA}, f_{dA}, R_{dA}), the space charge is calculated by

$$\rho = q \cdot [(p - n) + (N_D^+ - N_A^-) + (N_{dD} \cdot (1 - f_{dD}) - N_{dA} \cdot f_{dA})] \quad (13)$$

where N_D^+ and N_A^- denote the concentration of shallow donors and acceptors.

2.4 Generation/Recombination

Models for several generation and recombination mechanisms, which are in particular important to describe high field phenomena in power devices, are implemented in MINIMOS. The most important generation mechanism is impact ionisation which is modelled by the Chynoweth formulation [4]

$$R^{II} = -\alpha_n \cdot \frac{|\vec{J}_n|}{q} - \alpha_p \cdot \frac{|\vec{J}_p|}{q} \quad (14)$$

where the ionisation coefficients

$$\alpha_{n,p} = \alpha_{n,p}^\infty \cdot \exp\left(-\frac{E_{n,p}^c(y)}{E_{n,p}^{||}}\right)^{\beta_{n,p}} \quad (15)$$

depend on the electric field in the direction of the current flow $E_{n,p}^{||} = \vec{E} \cdot \frac{\vec{J}_{n,p}}{|\vec{J}_{n,p}|}$. The possible depth dependence of the critical field

$$E_{n,p}^c(y) = E_{n,p}^{c,0} \cdot \left(1 + F_{n,p} \cdot \exp\left(-\frac{y}{y_{n,p}^c}\right)\right) \quad (16)$$

has been suggested for modelling impact ionisation in silicon[20]. However, to our knowledge no data for the parameters $F_{n,p}$ and $y_{n,p}^c$ in GaAs exist at present.

Recombination at the semiconductor surface R^{SF} can be included by specifying surface recombination velocities $v_{n,p}^*$. This mechanism is then modelled by

$$R^{SF} = \frac{n \cdot p - n_i^2}{\frac{1}{v_p^*} \cdot (n + n_i) + \frac{1}{v_n^*} \cdot (p + n_i)} \cdot \delta(y) \quad (17)$$

	n	p	
α^∞	$3.5 \cdot 10^5$	$3.5 \cdot 10^5$	$1/cm$
$E^{c,0}$	$6.85 \cdot 10^5$	$6.85 \cdot 10^5$	V/cm
β	2	2	—
v^r	100	100	cm/s
C^{AU}	$5 \cdot 10^{-31}$	$5 \cdot 10^{-31}$	cm^6/s

Table 2: Generation/recombination parameters for GaAs

Direct recombination between conduction and valence band, the Auger recombination R^{AU} can also be included in the simulation.

$$R^{AU} = (C_n^{AU} \cdot n + C_p^{AU} \cdot p) \cdot (n \cdot p - n_i^2) \quad (18)$$

Tab. 2 shows the default values for generation/recombination parameters used in MINIMOS. The net generation/recombination rate R is then calculated by

$$R = R^{II} + R^{SF} + R^{AU} + R_{dD} + R_{dA} \quad (19)$$

3 Process Models

To provide a user-friendly way to determine the active doping profiles for ion implanted MESFETs the following models are implemented in MINIMOS:

- Gaussian distribution function for the ion implantation of B, P, As, O, Be, Si und Mg using data for the projected range R_p and the standard deviation σ_p from [5] and from Monte Carlo calculations [8].
- Diffusion using the solution of a twodimensional diffusion equation with constant coefficients [18]. The diffusion length $L_d = \sqrt{Dt}$ can directly be specified or is calculated by using built-in diffusion coefficients with specified diffusion temperature and time.
- The activation of the dopants can be accounted for by using an empirical activation formulation, which fits experiments after [16]:

$$C_{act} = a \cdot \frac{C_{tot}}{1 + \frac{C_{tot}}{C_{ref}}} \quad C_{ref} = 10^{18} cm^{-3} \quad a \leq 1 \quad (20)$$

C_{act} and C_{tot} denote the active and the total dopand concentration, a is a fit factor, which can be specified.

A more detailed description of these models can be found in [13]. Although this model contains some grave simplifications, it has proven to be even very useful for the determination of more complex doping profiles.

4 Results

To show the applicability of MINIMOS in the development of modern GaAs microwave FETs, a typical device, which was fabricated using a SIEMENS SAGFET process [6], has been simulated. Fig. 1 shows the structure and the doping profile of the device which was studied. The doping profile was calculated using the built-in process models and verified by comparing measured and simulated data of the sheet resistances after the different implantation steps. A EL2 concentration of $10^{16} cm^{-3}$ in the substrate was also included in the simulation.

Measured and simulated gate and transfer characteristics are shown in Fig. 2. As can be seen in Fig. 2(a), using an ideality factor of $n_{ID} = 1.5$, which was obtained from the measured data, gives precise agreement of the measured and the simulated gate characteristics at forward bias. The importance of an accurate description of the gate diode can also be seen in Fig. 2(b). The simulated transfer curve using an ideal gate model shows a distinct roll-off, if the gate voltage approaches the barrier height, which was 0.55 V in this case.

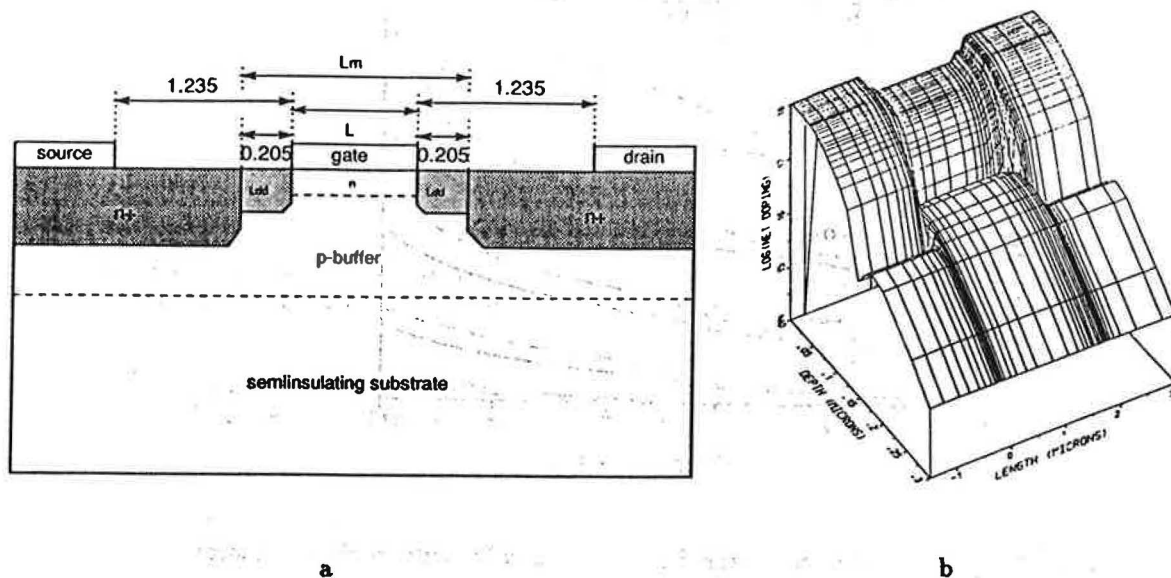


Fig. 1: Geometry (a) and doping profile (b) of the investigated device. The gatelength was $1.53 \mu\text{m}$.

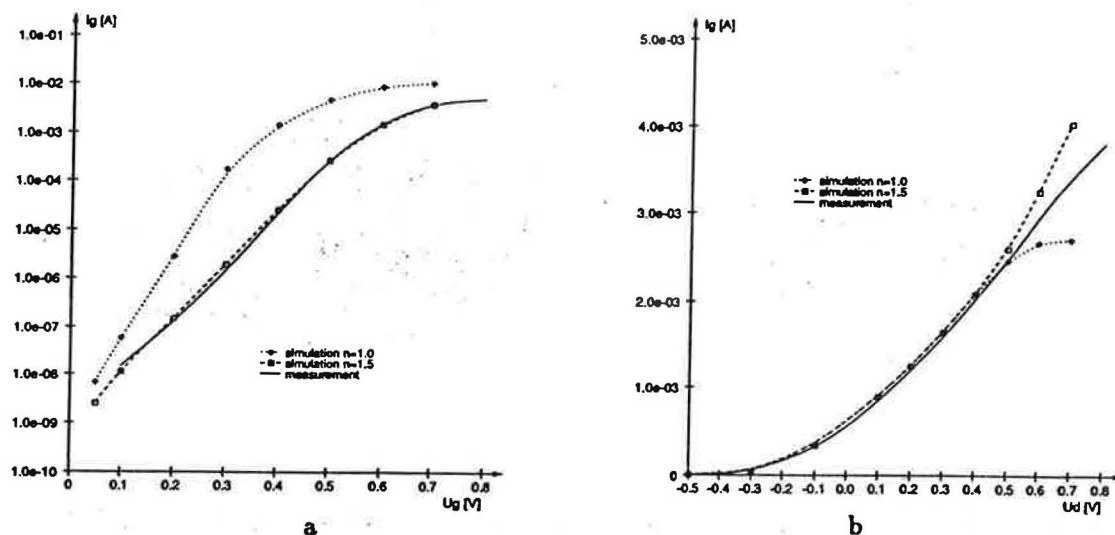


Fig. 2: Comparison between measured and simulated gate characteristics (a) and transfer characteristics ($V_{ds} = 1.2 \text{ V}$) (b).

Fig. 3 compares measured and simulated output characteristics of the device including the breakdown region. A good qualitative and a reasonable quantitative agreement has been obtained. The deviations between simulation and experimental data can partly be attributed to the uncertainty of the ionisation coefficients in (15) [3][21]. However, the program proved to be very valuable in determining the nature and location of avalanche breakdown in modern power FETs. Fig. 4 shows the avalanche generation rate at two different bias conditions in a power FET. The simulated device is a planar MESFET with $0.7 \mu\text{m}$ gatelength using an asymmetric contact implant. All other implants used in the FET processing (LDD and a buried p-layer) were also included in the simulation. Fig. 4(a) shows that for an open channel breakdown occurs at the interface between channel and n+ implant in the region between gate and drain. Under pinch-off conditions breakdown originates directly at the gate edges at the surface, as can be seen in Fig. 4(b). These simulation results, which could be experimentally verified by high-resolution emission microscopy [1], can be used for optimizing the device structure.

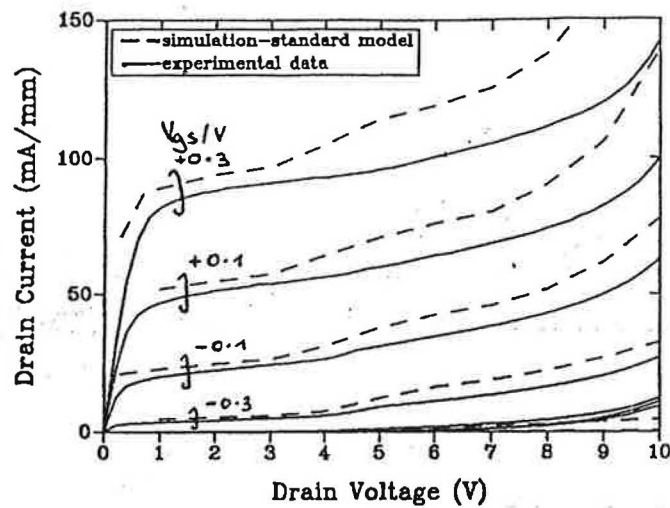


Fig. 3: Comparison between measured and simulated breakdown characteristics.

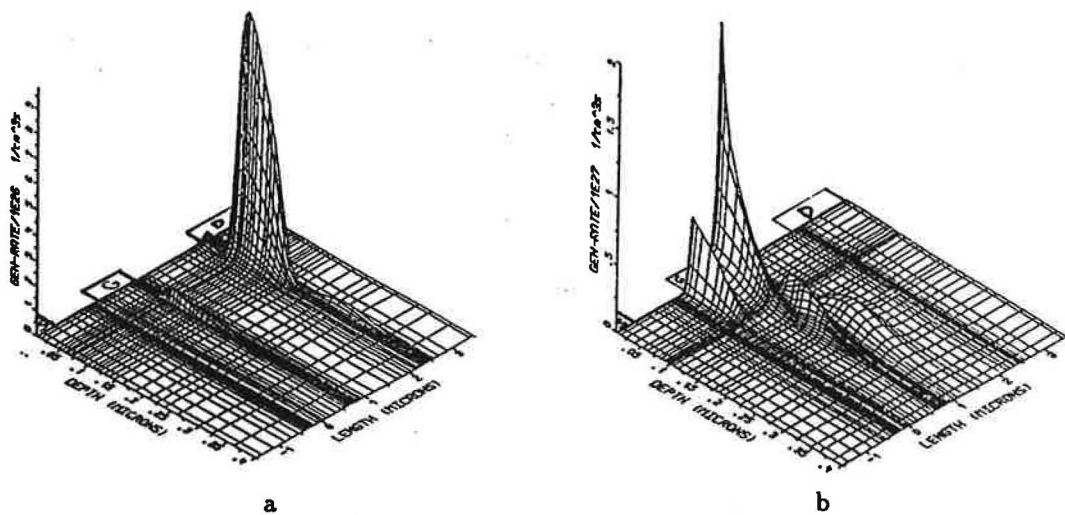


Fig. 4: Avalanche generation rate in a planar power FET for open channel $V_{gs} = 0$ V (a) and at threshold $V_{gs} = -3.5$ V (b).

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