Three-Dimensional Effects Due to the Field Oxide in MOS Devices Analyzed with MINIMOS 5

MARTIN THURNER, MEMBER, IEEE, AND SIEGFRIED SELBERHERR, SENIOR MEMBER, IEEE

***Abstract*—State of the art two-dimensional simulation programs cannot take into account any width effects for present ULSI MOSFET devices. Therefore, MINIMOS has been extended to a three-dimensional simulation program in order to investigate the parasitic effects at the channel edge on the MOSFET device characteristics. The box integration method after Forsythe has been applied for discretization. This method is excellently suitable for nonplanar interfaces. The most important nonplanar interface occurs at the transition of the gate oxide to the field oxide, which is commonly called "bird's beak." Approximating this interface as a rectangular shape leads to unrealistic results as will be shown in this paper. The oxide-body is defined by analytical functions, so it is easy to investigate a wide range of applications. An automatic grid refinement algorithm is used to generate the specific grid. Our simulation shows that the influence of the channel edge is not negligible for channel widths less than 2 μm. The total drain current for narrow channel MOSFET's is either increased or decreased by parasitic three-dimensional effects compared to wide channel (two dimensional) MOSFET's depending on the bias conditions.**

I. Introduction

The shrinking dimensions of the elements of integrated circuits require suitable device models in view of physics and mathematics for accurate simulation. The usual two-dimensional device simulations describe fairly well the electrical characteristics for wide channel transistors, but advanced VLSI technology has led to serious problems in modeling narrow channel devices, and therefore, a great demand for three-dimensional simulations has appeared ([22], [25]). Three-dimensional effects in MOSFET's caused by the finite channel width are, e.g., the shift of the threshold voltage, enhanced conductivity or the large depletion region near the drain at the channel edge. State of the art two-dimensional simulation programs cannot take into account these effects, and therefore, the use of the programs without the knowledge of the previously stated effects may led to serious problems. Accurate investigations of these effects and the knowledge of increased current densities under certain bias conditions at the channel edge are important not only for studying the electrical device characteristics but also for aging effects [9], [30].

A realistic physical model and suitable mathematical algorithms have been developed to simulate the previously stated three-dimensional effects. We shall report in Section II on the physics and in Section III on the mathematics that the simulations are based on. In addition, we shall present the device structure and discuss some aspects of the oxide body of the MOSFET. Some results of our simulations carried out by MINIMOS 5 are reported in Section IV and we will conclude with some discussions in Section V.

II. The Physical Model

The basis of most device simulation programs are (2.1)–(2.3), which are derived essentially from the Maxwellian equations, together with standard expressions for the electron and hole current. The following set of (2.4)–(2.11) as used in MINIMOS 5 differ from the conventional model. Utilizing the momentum method for the Boltzmann equation the approach focuses on the self-consistency in the four lowest moments (n, $\vec{J}_n$, ϵ, v_ϵ) of the distribution functions ([18]). The equations result from series expansions using the singular perturbation method [19] applied to the more general set of equations including the energy conservation equation. The standard drift-diffusion approximation can be obtained by cutting the expansion after the first-order moment. The relation between the standard and the extended (used in MINIMOS 5) drift-diffusion approximation is made by using for the energy $\epsilon = (3/2)q \cdot n \cdot U_T$. The standard drift-diffusion approximation is justified for small electric fields. The rapid developments of semiconductor technology lead to smaller device dimensions while the applied biases are not decreased accordingly. Thus it becomes extremely important to include high field effects and energy relaxation effects in semiconductor device simulation:

$$\mathrm{div}(\epsilon \ \mathrm{grad}\ \psi) = \rho \tag{2.1}$$

$$\mathrm{div}\ \vec{J}_n = -q \cdot R \tag{2.2}$$

$$\mathrm{div}\ \vec{J}_p = +q \cdot R \tag{2.3}$$

$$\vec{J}_n = -q \cdot \mu_n \cdot (n \ \mathrm{grad}\ \psi - \mathrm{grad}(n \cdot Ut_n)) \tag{2.4}$$

Manuscript received February 13, 1989; revised September 14, 1989. This work was supported by SIEMENS AG, Munich, Germany, the Digital Equipment Corporation, and by the "Fonds zur Förderung der wissenschaftlichen Forschung," under Project S43/10. This paper was recommended by Associate Editor M. Vanzi.

M. Thurner was with the Institut für Mikroelektronik, Technische Universität Wien, Austria. He is now with the Digital Equipment Corporation, Gesellschaft m.b.H., A-1040 Vienna, Austria.

S. Selberherr is with the Institut für Mikroelektronik, Technsiche Universität Wien, A-1040 Wien, Austria.

IEEE Log Number 9036168.

0278-0070/90/0800-0856$01.00 © 1990 IEEE

$$\vec{J}_p = -q \cdot \mu_p \cdot (p \text{ grad } \psi + \text{grad}(p \cdot Ut_p)). \quad (2.5)$$

The space charge ρ is modeled as $(n - p + N_D - N_A)$ at room temperature. Models for ρ suitable for simulation at liquid nitrogen temperature is also included in MINIMOS 5. The interested reader is referred to, e.g., [12], [13], [21], [27]. The electronic voltages $Ut_{n,p}$ are modeled as

$$Ut_n = \frac{k \cdot T_n}{q} = Ut_0 + \frac{2}{3} \cdot \tau_n^{\epsilon} \cdot (v_n^{\text{sat}})^2 \cdot \left(\frac{1}{\mu_n^{LISF}} - \frac{1}{\mu_n^{LIS}}\right) \quad (2.6)$$

$$Ut_p = \frac{k \cdot T_p}{q} = Ut_0 + \frac{2}{3} \cdot \tau_p^{\epsilon} \cdot (v_p^{\text{sat}})^2 \cdot \left(\frac{1}{\mu_p^{LISF}} - \frac{1}{\mu_p^{LIS}}\right). \quad (2.7)$$

The derivation of these equations and of the expression for the carrier mobilities $\mu_{n,p}$ (2.8), (2.9) are described in detail in [28]. $v_{n,p}^{\text{sat}}$ denotes the saturation velocities, $\tau_{n,p}^{\epsilon}$ the energy relaxation times. For detailed information about modeling the energy relaxation times see [28]:

$$\mu_n^{LISF} = \frac{2 \cdot \mu_n^{LIS}}{1 + \sqrt{1 + \left(\frac{2 \cdot \mu_n^{LIS} \cdot F_n}{v_n^{\text{sat}}}\right)^2}} \quad (2.8)$$

$$\mu_p^{LISF} = \frac{\mu_p^{LIS}}{1 + \left(\frac{\mu_p^{LIS} \cdot F_p}{v_p^{\text{sat}}}\right)} \quad (2.9)$$

$\mu_{n,p}^{LIS}$ denotes the mobility influenced by lattice, ionized impurities, and surface scattering (cf. [1], [6]). The driving forces $F_{n,p}$ are given by (2.10), (2.11). A discussion of this information can be found in [20]:

$$F_n = \left|\text{grad } \psi - \frac{1}{n} \text{grad } (n \cdot Ut_n)\right| \quad (2.10)$$

$$F_p = \left|\text{grad } \psi + \frac{1}{p} \text{grad}(p \cdot Ut_p)\right|. \quad (2.11)$$

For further information about modeling specific properties the interested reader is referred to [4]–[8], [12], [13], [28].

III. The Numerical Treatment of the Basic Equations

The physical model for the simulation has been characterized in the previous section. The basic semiconductor equations cannot be solved explicitly in general. Therefore, the solution must be calculated by means of numerical approaches. Dividing the domain and the simulation region into a finite number of subdomains, in which the solution can be approximated easily ([10], [24]), we use the classical finite difference grid for the three dimensions (x, y, z). The coupled nonlinear difference equations that are the basic semiconductor equations are solved with essentially Gummel's iterative method [16]. Finally the set of linearized equations with the huge amount of unknowns arising from the discretization scheme are solved with an iterative method (SOR) in the case of Poisson's equation and with a direct solver (Gauss elimination with alternating diagonal checkerboard ordering) in the case of the continuity equations. For detailed information on numerical aspects for solving large systems of linear equations the interested reader is referred to [14], [15], [17], [36].

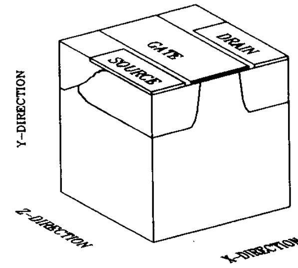

Fig. 1. Perspective view of the three-dimensional MOSFET structure.

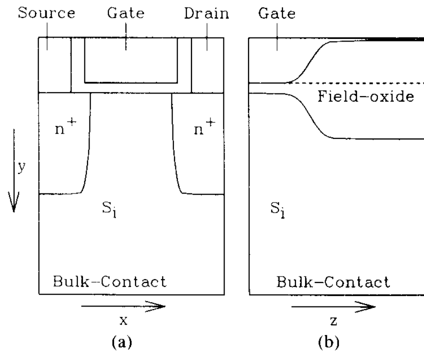

Fig. 2. Cross-sectional views of a MOSFET. (a) Cross section in channel length (x) and depth (y) direction. (b) Cross section in channel width (z) and depth (y) direction.

3.1. Geometry

The geometry of the three-dimensional MOSFET model is given in Fig. 1. The total simulation volume is divided into various subregions (semiconductor, oxide, contacts). In Fig. 2 the well-known cross section (channel length and depth) of the two-dimensional simulation and the cross section in the third dimension (channel width and depth) are shown to give a more detailed information on the device structure. The dashed line in Fig. 2(b) shows the gate contact as approximated in our simulations. The set of semiconductor equations has to be solved in the semiconductor region, therefore, we have to specify suitable boundary conditions for the numerical simulation. Specifying boundary conditions is quite easy in case of rectangular geometry of simulation domain and subdomain [26]. The "domain" is defined here as the whole simulation region including the insulating regions, the

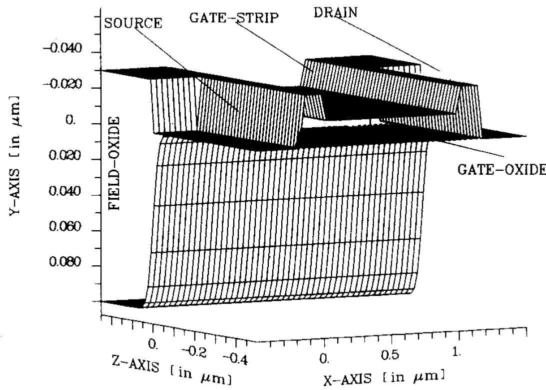

Fig. 3. Oxide body of the MOSFET structure (the oxide is between the upper and lower plane).

semiconductor region and the contact regions. A "subdomain" is defined as one particular region consisting of only one material (oxide, semiconductor, or contact). In a more realistic three-dimensional simulation we have to take into account nonrectangular subdomains (curved interfaces) as shown in Figs. 1-3. The most important nonplanar interface occurs at the transition of the gate oxide to the field oxide, which commonly is called "bird's beak" (see Fig. 2(b)). Approximating this interface as a rectangular shape leads to unrealistic results as will be shown in this paper.

We implemented an approximation to the complete oxide body as shown in Fig. 3. The upper plane denotes the interface of the oxide to the contacts and the surrounding volume, respectively. The lower plane denotes the interface of the oxide and the semiconductor. The definition of the interface in the program is quite general and can be varied in a wide range. Since we approximate the interfaces by analytical functions the shapes can be varied by a set of parameters. The gate contact is filled in the middle of the upper plane; the source and drain contacts are on the left and the right, respectively. In the middle of the gate region the distance of the upper and the lower plane is equal to the gate-oxide thickness as specified by the user.

3.2. Grid

It is not practicable to specify a suitable *a priori* grid for any given simulation problem. Therefore, MINIMOS generates the required grid automatically. The initial grid is set up using information about the geometry as defined by the user. An automatic grid refinement algorithm generates the specific grid. The adaption of the x-y grid is determined by the current flow of the minority carriers. The criterion for the adaption of the grid in the z-direction is derived from the potential difference between two discretization planes. If the maximum potential difference between two grid planes is larger than a specified potential difference ($\Delta \psi_{\text{ref}}$), a plane is inserted. The reference potential is defined in each subregion separately.

3.3. Discretization

For discretization we apply the box integration method after Forsythe [11] to deal with the boundary conditions of the nonrectangular interfaces. The boundary conditions for the interfaces are given by (3.1)-(3.3).

$$\epsilon_{\text{ins}} \left. \frac{\partial \psi}{\partial \vec{n}} \right|_{\text{ins}} = \epsilon_{\text{sem}} \left. \frac{\partial \psi}{\partial \vec{n}} \right|_{\text{sem}} - \sigma_{\text{int}} \tag{3.1}$$

$$\vec{J}_n \cdot \vec{n} = -q \cdot R^{\text{surf}} \tag{3.2}$$

$$\vec{J}_p \cdot \vec{n} = +q \cdot R^{\text{surf}}. \tag{3.3}$$

The discretization of the Dirichlet boundary conditions for the contact regions and the Neumann boundary conditions for the artificial boundaries is straightforward and can be found in, e.g., [26]. We shall discuss the discretization method for the nonrectangular interface boundary conditions (3.1)-(3.3) in detail, since by now nonplanar interfaces have been implemented only in simulation programs using finite elements. A point close to the interface is shown in Fig. 4. The surrounding finite integration volume is divided into two parts; one below the interface (hatched in this figure) representing the semiconductor region and one above the interface representing the oxide region. In this figure we can also see the discretization grid and the neighboring points. The integration areas F (as used in the following equations) denote the boundaries of the finite integration volume and the indexes sem and ins denote the parts in the semiconductor and the insulator, respectively. The indexes $(1 \cdots 6)$ of the integration areas define the position and the orientation in the following way: F_1 denotes the area perpendicular to the z-axis in the middle of the grid lines (k) and $(k-1)$, F_2 denotes the area perpendicular to the y-axis in the middle of the grid lines (j) and $(j-1)$, F_3 denotes the area perpendicular to the x-axis in the middle of the grid lines (i) and $(i-1)$, F_4 denotes the area perpendicular to the x-axis in the middle of the grid lines (i) and $(i+1)$, F_5 denotes the area perpendicular to the y-axis in the middle of the grid lines (j) and $(j+1)$, F_6 denotes the area perpendicular to the z-axis in the middle of the grid lines (k) and $(k+1)$. The integration area F_{int} is the interface element. Integrating (3.1) over the interface element we obtain

$$\begin{aligned} \int_{F_{\text{int}}} \epsilon_{\text{sem}} \frac{\partial \psi}{\partial \vec{n}} \, do &= \int_{F_{\text{int}}} \epsilon_{\text{sem}} \operatorname{grad} \psi \big|_{\text{sem}} \cdot \vec{n} \, do \\ &= \int_{F_{\text{int}}} \epsilon_{\text{ins}} \operatorname{grad} \psi \big|_{\text{ins}} \cdot \vec{n} \, do \\ &\quad + \int_{F_{\text{int}}} \sigma_{\text{int}} \, do. \end{aligned} \tag{3.4}$$

For each point at the interface we can write the Poisson equation in the semiconductor and the Laplace equation in the insulating material. Both equations are integrated over the respective volume (V_{sem}, V_{ins}).

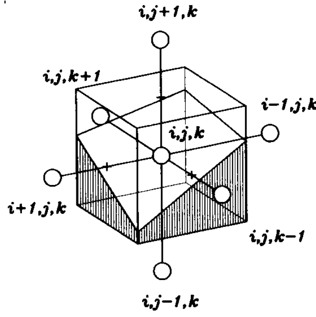

Fig. 4. Perspective view of a discretization point at the interface, e.g., oxide-semiconductor interface (hatched part denotes the volume in the semiconductor).

In the semiconductor region we obtain

$$\int_{V_{sem}} \text{div}\,(\epsilon_{sem} \cdot \text{grad}\,\psi)\,dv = \int_{V_{sem}} \rho\,dv. \quad (3.5)$$

In the insulating region we obtain

$$\int_{V_{ins}} \text{div}\,(\epsilon_{ins} \cdot \text{grad}\,\psi)\,dv = 0. \quad (3.6)$$

Using the law of Gauß and splitting the surface integral into its components (remembering the discretization grid) we can rewrite (3.5) and (3.6):

$$\oint_{O_{sem}} (\epsilon_{sem} \cdot \text{grad}\,\psi)\,\vec{do} = \sum_{k=1}^{6} \int_{F_{k_{sem}}} (\epsilon_{sem} \cdot \text{grad}\,\psi)\,\vec{do} + \int_{F_{int}} (\epsilon_{sem} \cdot \text{grad}\,\psi)\,\vec{do} = \int_{V_{sem}} \rho\,dv \quad (3.7)$$

$$\oint_{O_{ins}} (\epsilon_{ins} \cdot \text{grad}\,\psi)\,\vec{do} = \sum_{k=1}^{6} \int_{F_{k_{ins}}} (\epsilon_{ins} \cdot \text{grad}\,\psi)\,\vec{do} + \int_{F_{int}} (\epsilon_{ins} \cdot \text{grad}\,\psi)\,\vec{do} = 0. \quad (3.8)$$

Using (3.7) and (3.8) we can now substitute the gradients of ψ perpendicular to the interface in (3.4) and thus we obtain

$$\int_{V_{sem}} \rho\,dv + \int_{F_{int}} \sigma_{int}\,do = \epsilon_{sem} \cdot \sum_{k=1}^{6} \int_{F_{k_{sem}}} \text{grad}\,\psi\,\vec{do} + \epsilon_{ins} \cdot \sum_{k=1}^{6} \int_{F_{k_{ins}}} \text{grad}\,\psi\,\vec{do}. \quad (3.9)$$

The discretization of the terms in the equation above is quite simple, suitable approximations can be found in, e.g., [26], [31], and we can write the discretized equation in a more formal way by

$$\begin{aligned} &\psi_{i,j,k-1} \cdot (A_{sem} \cdot \epsilon_{sem} + A_{ins} \cdot \epsilon_{ins}) \cdot \frac{1}{n_{k-1}} \\ &+ \psi_{i,j-1,k} \cdot (B_{sem} \cdot \epsilon_{sem} + B_{ins} \cdot \epsilon_{ins}) \cdot \frac{1}{m_{j-1}} \\ &+ \psi_{i-1,j,k} \cdot (C_{sem} \cdot \epsilon_{sem} + C_{ins} \cdot \epsilon_{ins}) \cdot \frac{1}{l_{i-1}} \\ &- \psi_{i,j,k} \cdot (G_{sem} \cdot \epsilon_{sem} + G_{ins} \cdot \epsilon_{ins}) \\ &+ \psi_{i+1,j,k} \cdot (D_{sem} \cdot \epsilon_{sem} + D_{ins} \cdot \epsilon_{ins}) \cdot \frac{1}{l_i} \\ &+ \psi_{i,j+1,k} \cdot (E_{sem} \cdot \epsilon_{sem} + E_{ins} \cdot \epsilon_{ins}) \cdot \frac{1}{m_j} \\ &+ \psi_{i,j,k+1} \cdot (F_{sem} \cdot \epsilon_{sem} + F_{ins} \cdot \epsilon_{ins}) \cdot \frac{1}{n_k} \\ &= (\rho_{ijk} \cdot V_{sem} + \alpha_{i,j,k} \cdot A_{int}). \end{aligned} \quad (3.10)$$

A, B, C, D, E, F correspond to the areas F_1, F_2, F_3, F_4, F_5, F_6, and the coefficient G is the sum of the coefficients A/n_{k-1}, B/m_{j-1}, C/l_{i-1}, D/l_i, E/m_j, F/n_k, where l, m, n are the distances to the neighboring points in x, y, and z direction, respectively (see Fig. 4). The indexes sem and ins denote the parts of the areas in the semiconductor and the insulator, respectively. ϵ is the permittivity, σ is the interface charge, ρ is the space charge, and A_{int} is the interface area.

In an analogous way we obtain the discretized boundary condition for the continuity equations. For the electrons we integrate the boundary condition (3.2) over the interface element F_{int} and obtain:

$$\int_{F_{int}} \vec{J}_n \cdot \vec{do} = \int_{F_{int}} \vec{J}_n \cdot \vec{n}\,do = \int_{F_{int}} -q \cdot R^{surf}\,do \quad (3.11)$$

Furthermore, the continuity (2.2) must hold in the semiconductor region at the interface. So we can evaluate the volume integral:

$$\int_{V} \text{div}\,\vec{J}_n\,dv = \int_{V_{sem}} \text{div}\,\vec{J}_n\,dv = \int_{V_{sem}} -q \cdot R\,dv. \quad (3.12)$$

Using Gauß's law and remembering the discretization grid we can write:

$$\int_{V_{sem}} \text{div}\,\vec{J}_n\,dv = \oint_{O_{sem}} \vec{J}_n\,\vec{do} = \sum_{k=1}^{6} \int_{F_{k_{sem}}} \vec{J}_n\,\vec{do} + \int_{F_{int}} \vec{J}_n\,\vec{do} = \int_{V_{sem}} -q \cdot R\,dv. \quad (3.13)$$

The integration areas F and their indexes have been described previously. The discretization of the currents penetrating the areas F_1 to F_6 can be found in, e.g., [26], [31]. Thus we can substitute (3.13) into (3.11) and obtain

$$\sum_{k=1}^{6} \int_{F_{k_{sem}}} \vec{J}_n \, d\vec{o} = \int_{V_{sem}} -q \cdot R \, dv + \int_{F_{int}} q \cdot R^{surf} \, do. \tag{3.14}$$

Using a suitable discretization for the current densities we can write the discretized boundary condition at the semiconductor oxide interface by

$$\begin{aligned} & n(x_i, y_j, z_{k+1}) \cdot \frac{\mu_n(x_i, y_j, z1)}{\xi_{z1}} \cdot B(\eta_{z1} \cdot \xi_{z1}) \cdot A_{sem} + \\ & n(x_i, y_j, z_{k-1}) \cdot \frac{\mu_n(x_i, y_j, z0)}{\xi_{z0}} \cdot B(\eta_{z0} \cdot \xi_{z0}) \cdot B_{sem} + \\ & n(x_{i+1}, y_j, z_k) \cdot \frac{\mu_n(x1, y_j, z_k)}{\xi_{x1}} \cdot B(\eta_{x1} \cdot \xi_{x1}) \cdot C_{sem} + \\ & n(x_{i-1}, y_j, z_k) \cdot \frac{\mu_n(x0, y_j, z_k)}{\xi_{x0}} \cdot B(\eta_{x0} \cdot \xi_{x0}) \cdot D_{sem} + \\ & n(x_i, y_{j+1}, z_k) \cdot \frac{\mu_n(x_i, y1, z_k)}{\xi_{y1}} \cdot B(\eta_{y1} \cdot \xi_{y1}) \cdot E_{sem} + \\ & n(x_i, y_{j-1}, z_k) \cdot \frac{\mu_n(x_i, y0, z_k)}{\xi_{y0}} \cdot B(\eta_{y0} \cdot \xi_{y0}) \cdot F_{sem} - \\ & n(x_i, y_j, z_k) \cdot \left(\frac{\mu_n(x_i, y_j, z1)}{\xi_{z1}} \cdot B(-\eta_{z1} \cdot \xi_{z1}) \cdot A_{sem} \right. \\ & \quad + \frac{\mu_n(x_i, y_j, z0)}{\xi_{z0}} \cdot B(-\eta_{z0} \cdot \xi_{z0}) \cdot B_{sem} \\ & \quad + \frac{\mu_n(x1, y_j, z_k)}{\xi_{x1}} \cdot B(-\eta_{x1} \cdot \xi_{x1}) \cdot C_{sem} \\ & \quad + \frac{\mu_n(x0, y_j, z_k)}{\xi_{x0}} \cdot B(-\eta_{x0} \cdot \xi_{x0}) \cdot D_{sem} \\ & \quad + \frac{\mu_n(x_i, y1, z_k)}{\xi_{y1}} \cdot B(-\eta_{y1} \cdot \xi_{y1}) \cdot E_{sem} \\ & \quad \left. + \frac{\mu_n(x_i, y0, z_k)}{\xi_{y0}} \cdot B(-\eta_{y0} \cdot \xi_{y0}) \cdot F_{sem} \right) \\ & = -R(x_i, y_j, z_k) \cdot V_{sem} \\ & \quad + R^{SURF}(x_i, y_j, z_k) \cdot A_{int}. \end{aligned} \tag{3.15}$$

V_{sem} is the part of the integration volume in the semiconductor, R^{SURF} denotes the surface recombination rate, and A_{int} is the interface element. The coefficients ξ_{x0}, ξ_{x1}, ξ_{y0}, ξ_{y1}, ξ_{z0}, ξ_{z1}, and η_{x0}, η_{x1}, η_{y0}, η_{y1}, η_{z0}, η_{z1} include the dependence on the potential ψ and the electronic voltage Ut_n of the carriers [31]. A fully analogous expression can be found for the continuity equation of the holes.

3.4. Current Integration

The geometry in the width direction is usually not defined for two-dimensional MOSFET simulations nor are idealistic assumptions made. Therefore, the computed drain currents from two-dimensional simulations are essentially not comparable to the three-dimensional currents for narrow channel devices. We shall describe briefly the current integration method and discuss two modifications to get a better agreement between two- and three-dimensional simulation results.

The current of the drain contact can be calculated by

$$I_D = \int_{A_k} (\vec{J}_n + \vec{J}_p) \cdot d\vec{a}. \tag{3.16}$$

A_k denotes the contact area and J_n and J_p are the electron and the hole current penetrating the contact area. For numerical reasons we extend the integral of (3.16) to the total semiconductor surface using the function F:

$$I_D = \oint_{O_{sem}} F \cdot (\vec{J}_n + \vec{J}_p) \cdot d\vec{o} \tag{3.17}$$

with

$$F = \begin{cases} 1, & \text{at the drain contact,} \\ 0, & \text{at all other contacts,} \\ 0 < F < 1, & \text{elsewhere.} \end{cases} \tag{3.18}$$

Using the law of Gauβ and $(\vec{J}_n + \vec{J}_p) = \vec{J}$, we can write:

$$I_D = \int_{V_{sem}} \text{grad } F \cdot \vec{J} \, dv. \tag{3.19}$$

For the two-dimensional simulation the z-component is assumed to be zero, and the simulation volume is limitated by the channel width. Thus (3.19) reduces in common to (3.20):

$$I_{D_2} = w \int_A \text{grad } F \cdot \vec{J} \, da \tag{3.20}$$

where w denotes the channel width. If we use in the two-dimensional simulation the width specified by the process mask, we obviously do not get currents comparable to the currents computed with three-dimensional simulation. As shown in Fig. 5 the total channel is reduced by the hatched area, and therefore, we have to take into account this reduced volume with the current integration. We shall demonstrate two methods that compute the current from two-dimensional simulations taking into account the reduced channel width. The first method is to compute an effective channel width specified by the geometry as given with

$$w_{eff} = w_{mask} - \frac{1}{D_{ch}} \cdot \int_0^{w_{mask}} fox(z) \Big|_{l/2} dz \tag{3.21}$$

where w_{mask} is the channel width specified by the process, D_{ch} denotes the channel depth at the channel edge (Fig. 5), and $fox(z)_{l/2}$ is the function that describes the geometry of the channel in width direction in the middle of the

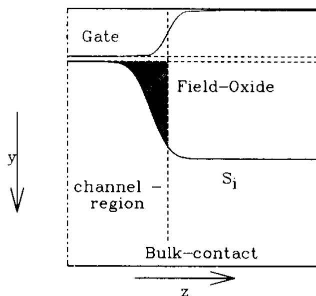

Fig. 5. Cross section in channel width (z) and depth (y) direction (hatched area shows the reduction of the channel due to field oxide).

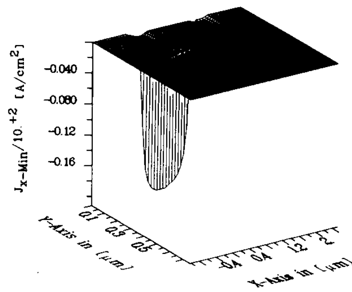

Fig. 6. Typical current density distribution of a MOSFET in channel length (x) and depth (y) direction.

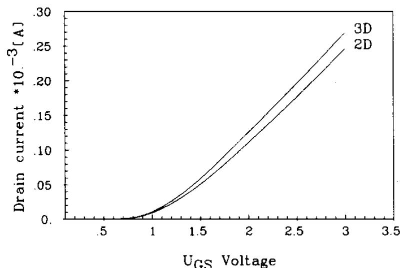

Fig. 7. Characteristic of drain current over gate voltage.

channel length. Substituting this expression of w_{eff} for w in (3.20) we obtain a better, but not satisfactory, agreement for two- to three-dimensional calculation results. The reason for the disagreement is based on the highly nonequidistributed current densities with respect to depth (cf. Fig. 6). Thus we propose the formulation given by (3.22) for the current integration with the two-dimensional simulation:

$$I_{D_2} = \int_A w \cdot \text{grad}\, F \cdot \vec{J}\, da \tag{3.22}$$

where w is no more a constant value but a function of the channel depth. This definition has proven to be appropriate because of the nonequidistributed current densities. Obviously we cannot describe three-dimensional effects by (3.22), but we can detect the differences in the drain current due to increased or decreased current densities at the channel edge. Fig. 7 shows the comparison of two-

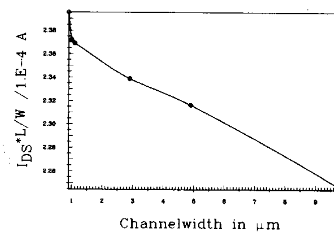

Fig. 8. Experimental characteristics of the normalized drain current over channel width.

and three-dimensional characteristics for $U_{DS} = 1$ V and a rectangular approximated field-oxide. Fig. 8 shows the measured characteristic of an n-channel device with weak field implantation at nearly the same bias conditions where the enhanced conductivity can be seen. Practical investigations on the behavior of the characteristics with different field implantations can be found in [9].

IV. Some Results

This section is dedicated to the results of our three-dimensional simulations. The geometries of the three investigated MOSFET's are given with Fig. 9(a)–(c); they differ in the field-oxide semiconductor interface. The oxide body (limitated by the interfaces) can be specified by parameters, thus a large range of applications can very easily be investigated. The approximation for the oxide body is made mainly by "error functions," which seem to be appropriate for the interfaces. The cross-sectional views are drawn in Fig. 10.

Transistor 1 has a transition length of 0.25 μm from gate oxide to full field oxide thickness (the transition length = BEAKL is defined in Fig. 10). The gate oxide is extended straight into the third direction for transistor 2 (no transition). This device geometry is chosen to make a comparison with the classical theoretical investigations on the threshold behavior for narrow channel devices [29]. The third transistor has a rectangular shaped approximation for the field oxide. The three devices are n-channel MOSFET's with a 1.5 μm by 1 μm channel mask specification and a gate oxide thickness of 15 nm. The threshold voltages for these devices are about 0.75 V without the channel width effects.

4.1. Subthreshold Behavior of the MOSFET

The quantities ψ, n, $J_{x_{min}}$, $J_{y_{min}}$ at $y = 0$ (position of the gate oxide-semiconductor interface) of the three investigated devices for these bias conditions ($U_{GS} = 0.5$ V, $U_{DS} = 1.0$ V, $U_{SB} = 0.0$ V) are shown in Figs. 11(a)–(d)–13(a)–(d). Fig. 11(a)–(d) presents the quantities of transistor 1, Fig. 12(a)–(d) for transistor 2, and Fig. 13(a)–(d) for transistor 3. The indexes a, b, c, d correspond to the quantities (a for the potential, b for the minorities, c for the current densities of the minorities in x-direction, and d for the current densities of the minorities in y-direction).

A comparison of the potential distribution of transistor 1 (Fig. 11(a)) and 3 (Fig. 13(a)) shows clearly the differ-

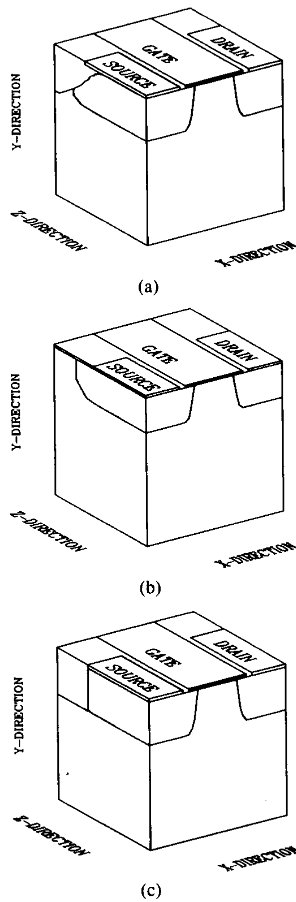

Fig. 9. (a) Geometry of transistor 1 (graded transition of gate oxide thickness to field oxide thickness). (b) Geometry of transistor 2 (gate oxide thickness equals field oxide thickness). (c) Geometry of transistor 3 (rectangular transition of gate oxide thickness to field oxide thickness).

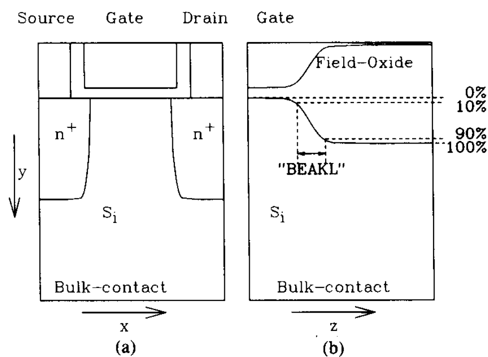

Fig. 10. Cross-sectional views of a MOSFET showing the definition of the "bird's beak" length. (a) Cross section in channel length (x) and depth (y) direction. (b) Cross section in channel width (z) and depth (y) direction.

ent gradients in the region of the field-oxide-semiconductor interfaces. The length of the transition is about 0.3 μm for transistor 1 and about 0.1 μm for transistor 3. The transition is calculated from 10 to 90% of the increase of

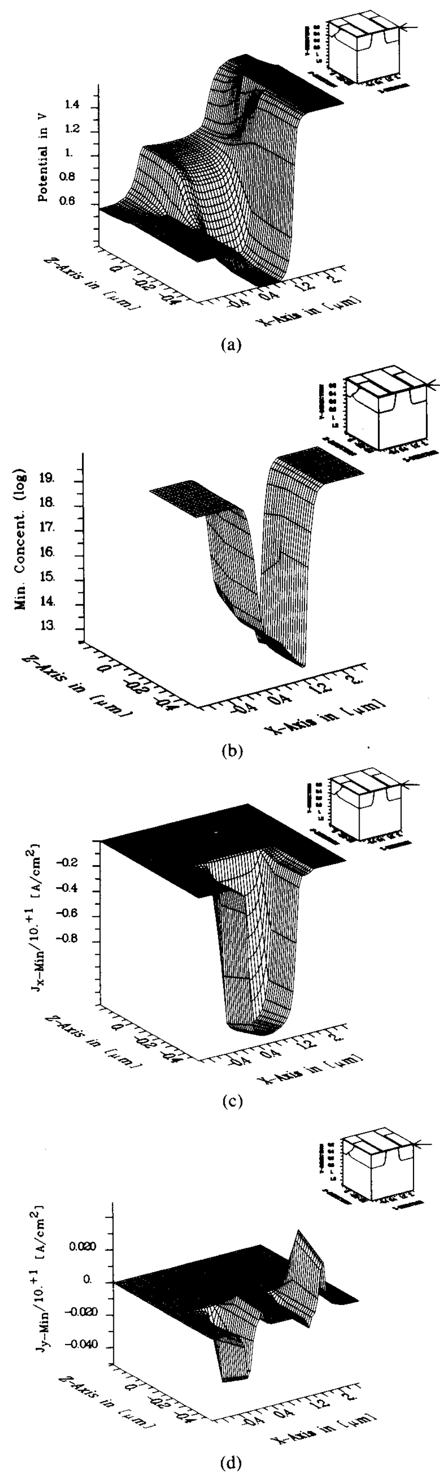

Fig. 11. (a) Potential distribution of transistor 1 at $U_{GS} = 0.5$ V, $U_{DS} = 1.0$ V, $U_{SB} = 0.0$ V. (b) Minority carrier distribution of transistor 1 at $U_{GS} = 0.5$ V, $U_{DS} = 1.0$ V, $U_{SB} = 0.0$ V. (c) Current density component in x-direction of the minority carriers of transistor 1 at $U_{GS} = 0.5$ V, $U_{DS} = 1.0$ V, $U_{SB} = 0.0$ V. (d) Current density component in y-direction of the minority carriers of transistor 1 at $U_{GS} = 0.5$ V, $U_{DS} = 1.0$ V, $U_{SB} = 0.0$ V.

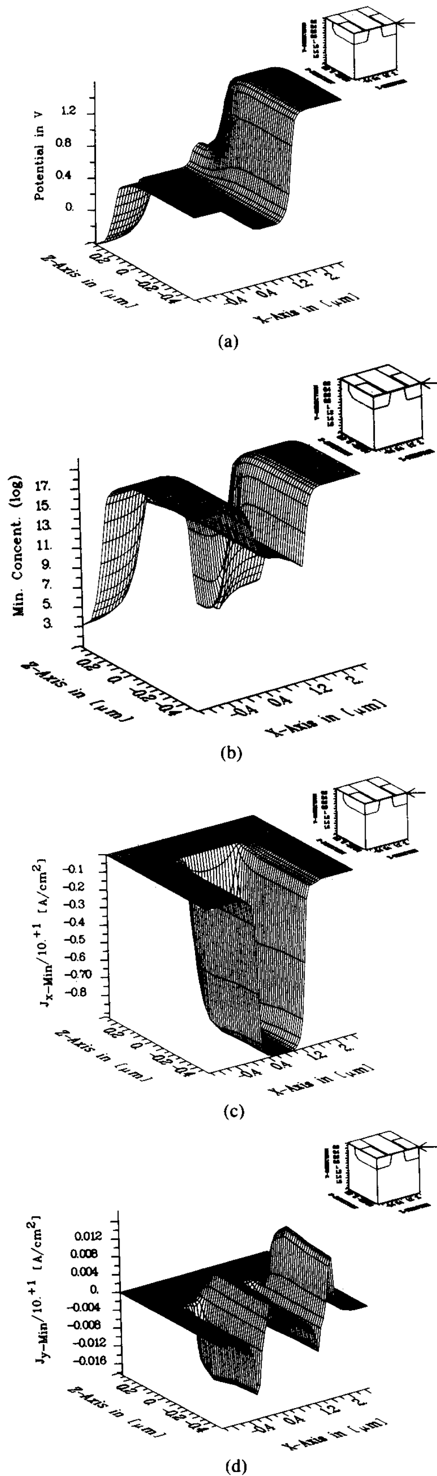

Fig. 12. (a) Potential distribution of transistor 2 at U_{GS} = 0.5 V, U_{DS} = 1.0 V, U_{SB} = 0.0 V. (b) Minority carrier distribution of transistor 2 at U_{GS} = 0.5 V, U_{DS} = 1.0 V, U_{SB} = 0.0 V. (c) Current density component in x-direction of the minority carriers of transistor 2 at U_{GS} = 0.5 V, U_{DS} = 1.0 V, U_{SB} = 0.0 V. (d) Current density component in y-direction of the minority carriers of transistor 2 at U_{GS} = 0.5 V, U_{DS} = 1.0 V, U_{SB} = 0.0 V.

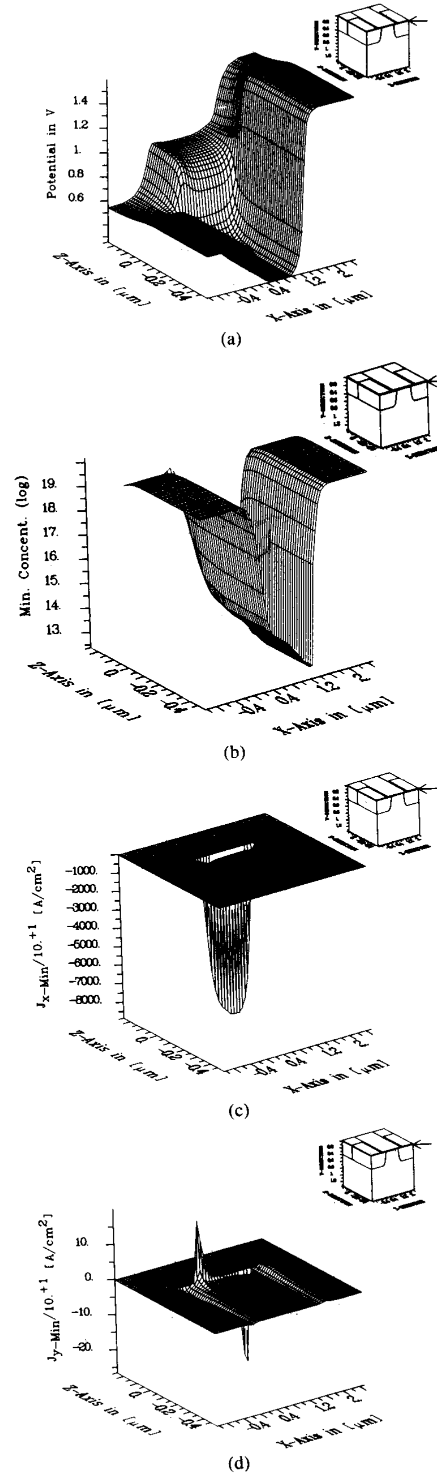

Fig. 13. (a) Potential distribution of transistor 3 at U_{GS} = 0.5 V, U_{DS} = 1.0 V, U_{SB} = 0.0 V. (b) Minority carrier distribution of transistor 3 at U_{GS} = 0.5 V, U_{DS} = 1.0 V, U_{SB} = 0.0 V. (c) Current density component in x-direction of the minority carriers of transistor 3 at U_{GS} = 0.5 V, U_{DS} = 1.0 V, U_{SB} = 0.0 V. (d) Current density component in y-direction of the minority carriers of transistor 3 at U_{GS} = 0.5 V, U_{DS} = 1.0 V, U_{SB} = 0.0 V.

TABLE I
TWO- AND THREE-DIMENSIONAL DRAIN CURRENTS FOR THE THREE TRANSISTORS

Transistor	I_{D_2}/A	I_{D_3}/A
1	$1,49 \cdot 10^{-10}$	$1,59 \cdot 10^{-10}$
2	$2,53 \cdot 10^{-10}$	$1,71 \cdot 10^{-10}$
3	$2,53 \cdot 10^{-10}$	$1,16 \cdot 10^{-08}$

the potential distribution in the middle of the channel length. Extremely high differences are observed in the distributions of carriers and the current densities (Fig. 11(b)–(d) and Fig. 13(b)–(d)).

Since the classical investigations on the threshold behavior due to the channel limitation [29] have been made without field oxide and field implantation, we present some results of the investigation of transistor 2. As expected the distributions (Fig. 12(a)–(d)) show no discontinuities near the channel edge.

The two- and three-dimensional drain currents at the bias point are listed in Table I. The applied voltages for this biaspoint are: $U_{GS} = 0.5$ V, $U_{DS} = 1.0$ V, $U_{SB} = 0.0$ V.

I_{D_2} and I_{D_3} are the currents calculated by two- and three-dimensional simulations, respectively. The current of transistor 2 calculated by three-dimensional simulations is smaller than the current calculated by two-dimensional simulations as predicted by theoretical investigations [30] (see Table I). Due to the field oxide an increased drain current for the transistors 1 and 3 can be observed (cf. [2], [3], [23], [32]–[35]). Including any field implantation the device characteristics change under certain conditions into their opposite (see [9]). Investigations on this topic are planned for the future.

4.2. Above Threshold Behavior of the MOSFET

The different quantities of the three investigated devices for the bias conditions $U_{GS} = 3.0$ V, $U_{DS} = 1.0$ V, $U_{BS} = 0.0$ V are shown in Figs. 14(a)–(d)–16(a)–(d). Fig. 14(a)–(b) presents the quantities of transistor 1, Fig. 15(a)–(d) for transistor 2, and Fig. 16(a)–(d) for transistor 3. The indexes a, b, c, d correspond to the quantities as described above.

The investigated bias point is characterized by high gate-source but low drain-source voltages. Due to the high gate voltage we can see the increasing potential in the field oxide (cf. Fig. 14(a), Fig. 16(a)). A comparison of the potential distributions of transistors 1 and 3 show the different gradients in width direction. These transitions show the same behavior as the shape of the field oxide: high gradients correspond to rectangular shape, low gradients correspond to the smooth transition of gate-oxide to field-oxide. The high voltage at the semiconductor-field oxide interface leads to an accumulation of the mobile carriers nearby (Fig. 14(b), 16(b)). As shown in Figs. 14(c), (d) and 16(c), (d), these increased carrier densities result in enhanced conductivities. This behavior has not been reported before but can be easily observed experimentally (Fig. 12).

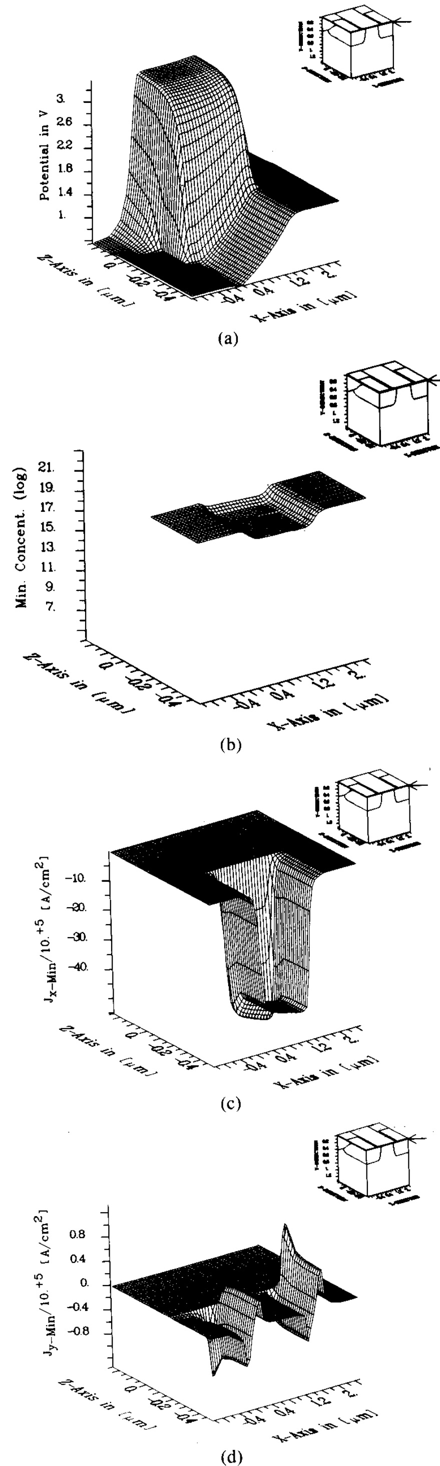

Fig. 14. (a) Potential distribution of transistor 1 at $U_{GS} = 3.0$ V, $U_{DS} = 1.0$ V, $U_{SB} = 0.0$ V. (b) Minority carrier distribution of transistor 1 at $U_{GS} = 3.0$ V, $U_{DS} = 1.0$ V, $U_{BS} = 0.0$ V. (c) Current density component in x-direction of the minority carriers of transistor 1 at $U_{GS} = 3.0$ V, $U_{DS} = 1.0$ V, $U_{BS} = 0.0$ V. (d) Current density component in y-direction of the minority carriers of transistor 1 at $U_{GS} = 3.0$ V, $U_{DS} = 1.0$ V, $U_{BS} = 0.0$ V.

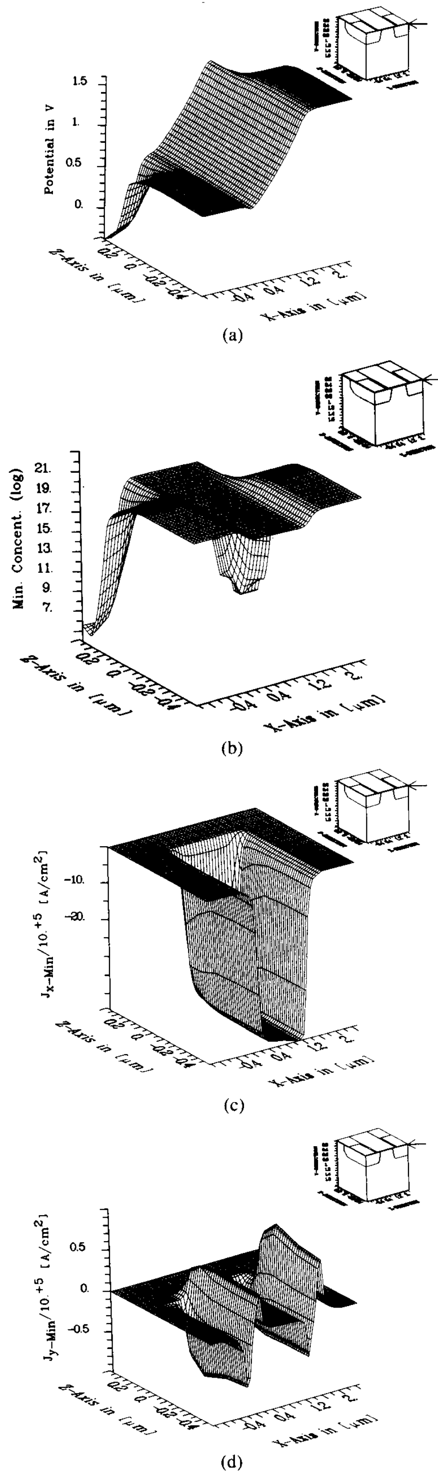

Fig. 15. (a) Potential distribution of transistor 2 at U_{GS} = 3.0 V, U_{DS} = 1.0 V, U_{BS} = 0.0 V. (b) Minority carrier distribution of transistor 2 at U_{GS} = 3.0 V, U_{DS} = 1.0 V, U_{BS} = 0.0 V. (c) Current density component in x-direction of the minority carriers of transistor 2 at U_{GS} = 3.0 V, U_{DS} = 1.0 V, U_{BS} = 0.0 V. (d) Current density component in y-direction of the minority carriers of transistor 2 at U_{GS} = 3.0 V, U_{DS} = 1.0 V, U_{BS} = 0.0 V.

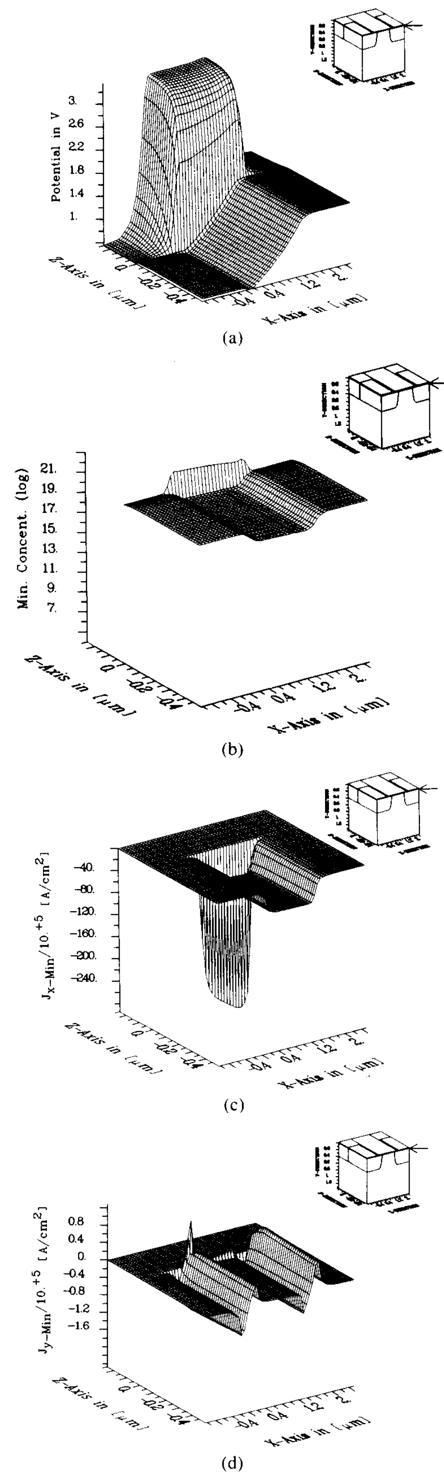

Fig. 16. (a) Potential distribution of transistor 3 at U_{GS} = 3.0 V, U_{DS} = 1.0 V, U_{BS} = 0.0 V. (b) Minority carrier distribution of transistor 3 at U_{GS} = 3.0 V, U_{DS} = 1.0 V, U_{BS} = 0.0 V. (c) Current density component in x-direction of the minority carriers of transistor 3 at U_{GS} = 3.0 V, U_{DS} = 1.0 V, U_{BS} = 0.0 V. (d) Current density component in y-direction of the minority carriers of transistor 3 at U_{GS} = 3.0 V, U_{DS} = 1.0 V, U_{BS} = 0.0 V.

TABLE II
TWO- AND THREE-DIMENSIONAL DRAIN CURRENTS FOR THE THREE TRANSISTORS

Transistor	I_{D_2}/A	I_{D_3}/A
1	$5,26 \cdot 10^{-5}$	$5,30 \cdot 10^{-5}$
2	$8,48 \cdot 10^{-5}$	$7,68 \cdot 10^{-5}$
3	$8,48 \cdot 10^{-5}$	$8,98 \cdot 10^{-5}$

For transistor 2 the gate oxide is extended straight into the width direction, thus we have no field oxide. Therefore, the potential distribution shows no changing behavior at the channel edge (Fig. 15(a)). We do not have an increasing potential transition and thus we cannot see any accumulation region (Fig. 15(b)). The previously described parasitic current at the channel edge does not appear in this device (Fig. 15(c), (d)). The current densities of transistor 2 decrease continuously in contrast to transistor 1 and 3. In spite of this moderate behavior, this device type is not practicable since we do not have any limitations for the channel, neither by a field oxide nor by a field implantations. Thus the active channel region could extend over the defined channel width and the isolation to the neighboring devices is not guaranteed.

The two- and three-dimensional drain currents at the bias point are listed in Table II. The applied voltages for this biaspoint are: $U_{GS} = 3.0$ V, $U_{DS} = 1.0$ V, $U_{BS} = 0.0$ V. I_{D_2} and I_{D_3} are the currents calculated by two- and three-dimensional simulations, respectively.

V. Conclusion and Discussion

The influence of the semiconductor-field oxide interface with different shape and bias conditions is described in this paper. We have demonstrated that the well-known effect responsible for the shift of the threshold voltage at small channel devices changes into its opposite at certain conditions. The influence of these effects on the device characteristics depends on the gradient of the bird's beak and the channel width. A high gradient in the field oxide shape results in high parasitic current at the channel edge; this effect is less significant for low gradients. Narrow channel devices with high gradients have much higher currents than predicted by two-dimensional calculations while the agreement with two-dimensional simulations is good for wide channel devices in any case. Using a low gradient in bird's beak we get a very smooth potential distribution compared to a nearly rectangular shape.

Acknowledgment

The authors are indebted to Prof. H. Pötzl for many helpful discussions.

References

[1] N. Ahmad and V. K. Arora, "Velocity-field profile of n-silicon: A theoretical analysis," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 1075-1077, 1986.

[2] L. A. Akers, "Characterization of the inverse narrow width effect," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 2476-2484, 1987.

[3] —, "Inverse narrow width effects," *IEEE Trans. Electron Devices*, vol. EDL-7, pp. 419-421, 1986.

[4] N. D. Arora and S. G. Gildenblad, "A semi-empirical model of the MOSFET inversion layer mobility for low temperature operation," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 89-93, 1987.

[5] N. D. Arora, J. R. Hauser, and D. J. Roulston, "Electron and hole mobilities in silicon as a function of concentration and temperature," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 292-295, 1982.

[6] G. Baccarani and M. R. Wordeman, "A investigation of steady-state velocity overshoot in silicon," *Solid-State Electron.*, vol. 28, pp. 407-416, 1985.

[7] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 52, pp. 2192-2193, 1967.

[8] P. Ciampolini, A. Gnudi, R. Guerrieri, M. Rudan, and G. Baccarani, "3D simulation of a narrow-width MOSFET," in *ESSDERC Proc.*, Bologna, 1987, pp. 413-416.

[9] J. L. Coppee, E. Figueras, B. Goffin, D. Gloesener, and F. Van De Wiele, "Narrow channel effect on n- and p-channel devices fabricated with the SILO and BOX isolation techniques," in *ESSDERC Proc.*, Montpellier, 1988, pp. 749-752.

[10] A. DeMari, "An accurate numerical steady-state one-dimensional solution of the P-N junction," *Solid-State Electron.*, vol. 11, pp. 33-58, 1968.

[11] G. E. Forsythe and W. R. Wasaw, *Finite Difference Methods for Partial Differential Equations*. New York: Wiley, 1960.

[12] F. H. Gaensslen, R. C. Jaeger, and J. J. Walker, "Low-temperature threshold behavior of depletion mode devices," in *IEDM Proc.*, 1976, pp. 520-524.

[13] F. H. Gaensslen, V. L. Rideeout, E. J. Walker, and J. J. Walker, "Very small MOSFET's for low temperature operation," *IEEE Trans. Electron Devices*, vol. ED-24, pp. 218-229, 1977.

[14] G. H. Golub and R. S. Varga, "Chebyshev semi-iterative methods, successive over-relaxation methods, and second order Richardson iterative methods," *Num. Math.*, vol. 3, pp. 147-168, 1961.

[15] R. G. Grimes, D. R. Kincaid, and D. M. Young, "ITPACK 2A—A FORTRAN implementation of adaptive accelerated iterative methods for solving large sparse linear systems," Rep. CNA-164, Center for Numerical Analysis, Univ. Texas, Austin, 1979.

[16] H. K. Gummel, "A self-consistent iterative scheme for one-dimensional steady-state transistor calculations," *IEEE Trans. Electron Devices*, vol. ED-11, pp. 455-465, 1964.

[17] L. A. Hageman, Franklin T. Luk, and D. M. Young, "On the equivalence of certain iterative acceleration methods," *SIAM J. Numer. Anal.*, vol. 17, no. 6, pp. 852-873, Dec. 1980.

[18] W. Hänsch and M. Miura-Mattausch, "A new current relation for hot electron transport," in *Proc. NASECODE IV Conf.*, Dublin, 1985, pp. 311-314.

[19] W. Hänsch and C. Schmeiser, "Hot electron transport in semiconductors," to appear in *ZAMP*, 1989.

[20] W. Hänsch and S. Selberherr, "MINIMOS 3: A MOSFET simulator that includes energy balance," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 1074-1078, 1987.

[21] A. K. Henning, N. Chan, and J. D. Plummer, "Substrate current in N-channel and P-channel at cryogenic temperatures: Measurement and a two-dimensional model for CMOS technology," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 64-74, 1987.

[22] A. Husain and S. G. Chamberlain, "3D simulation of VLSI MOSFET's: The 3D simulation program WATMOS," *IEEE Trans. Solid-State Circuits*, vol. SC-17, pp. 261-268, 1982.

[23] K. K. Hsueh, J. J. Sanchez, T. A. DeMassa, and L. A. Akers, "Invers-narrow-width effects and small-geometry MOSFET threshold voltage model," *IEEE Trans. Electron Devices*, vol. 35, pp. 325-338, 1988.

[24] P. A. Markowich, *The Stationary Semiconductor Device Equations*. New York: Springer, 1986.

[25] S. Onga, N. Shigyo, M. Yoshimi, and K. Taniguchi, "Analysis of submicron MOS device characteristics using a composite full three-dimensional process/device simulation system," in *Proc. Symp. on VLSI Technology*, San Diego, 1986, pp. 15-16.

[26] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. New York: Springer, 1984.

[27] —, "Low temperature MOS device modeling," in *Proc. Symp. Electr. Society on Low Temperature Electronics*, 1987.

[28] —, "MOS Device modeling at 77K," *IEEE Trans. Electron Devices*, *IEEE Trans. Electron Devices*, vol. 36, pp. 1464-1474, 1989.

[29] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981.

[30] —, *VLSI Technology*. New York: McGraw-Hill, 1983.

[31] M. Thurner, "Dreidimensionale Modellierung von MOS Transistoren," Ph.D. dissertation, Technische Universität Wien, 1988.

[32] M. Thurner and S. Selberherr, "The extension of MINIMOS to a 3D simulation program," in *Proc. NASCODE V*, Dublin, 1987, pp. 327-332.
[33] —, "Comparison of long- and short-channel MOSFET's carried out by 3D-MINIMOS," in *ESSDERC Proc.*, Bologna, 1987, pp. 409-412.
[34] —, "3D MOSFET device effects due to field oxide," in *ESSDERC Proc.*, Montpellier, 1988, pp. 245-248.
[35] M. Thurner, P. Lindorfer, and S. Selberherr, "Numerical treatment of nonrectangular field-oxide for 3D MOSFET simulation," in *SISDEP Proc.*, Bologna, 1988, pp. 375-381.
[36] R. S. Varga, *Matrix Iterative Analysis*. Englewood Cliffs, NJ: Prentice-Hall, 1962.

*

Martin Thurner (S'86-M'89) received the degree of "Diplomingenieur" in telecommunication engineering from the Technical University of Vienna in 1984.

In 1985 he worked for the Federal Research and Test Institute, Vienna, Austria, where he was mainly concerned with the safety and reliability of devices and systems. He joined the Institut für Allgemeine Elektrotechnik and Elektronik at the Technical University of Vienna in 1985. His main goal was to extend the two-dimensional device simulator MINIMOS in the third dimension. In 1988 he joined Digital Equipment Corporation, Vienna, Austria, where he is currently working in the field of device modeling.

*

Siegfried Selberherr (M'79-M'84) received the degree of "Diplomingenieur" in control theory and industrial electronics from the Technical University of Vienna, Austria, in 1978 and the Ph.D. degree in 1981.

In 1978, he joined the Institut für Allegemeine Elecktrotechnik und Elektronik, Technical University of Vienna, as a professor. He has been the Head of the Institut für Mikroelektronik, Technical University of Vienna, since 1988. He has authored and co-authored more than 100 papers and is the author of the book *Analysis and Simulation of Semiconductor Devices*. He is also the editor of *The Transactions of the Society for Computer Simulation, Elecktrosoft*, and *Mikroelektronik*. His interests include modeling and simulation of problems for microelectronics engineering.

Dr. Selberherr received the Dr. Ernest Fehrer Award in 1985, the "hachrichtentechnische Gesellscaft Award in 1986, and the Heinz Zemanek Award in 1987. He is a member of ACM, the Society of Industrial and Applied Mathematics, and Verband deutscher Elektrotechniker.