ANALYSIS OF THE DEGRADATION OF N-CHANNEL LDD MOSFET'S BY NUMERICAL SIMULATION OF THE CHARGE-PUMPING EXPERIMENT

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ABSTRACT

The charge-pumping characteristics of LDD MOSFET's before and after hot-carrier stress is discussed. A two-dimensional transient numerical model of the charge-pumping experiment is used in the study. The contribution of the different regions in the LDD device to the charge-pumping curve is analyzed in detail. Time evolution of the spatial trap distribution in the device while stressing is extracted from the experimental charge-pumping data. For the extracted distributions the charge-pumping characteristics is calculated numerically, and compared with the experiment; the obtained agreement confirms the accuracy of the spatial trap distributions.

INTRODUCTION

Hot-carriers in device produce the interface (volume) traps, trapped charge in the oxide and the additional oxide traps, which could change the device characteristics. How the characteristics is degraded depends on the amount, location and the nature of the damage. It is quite difficult to extract the parameters of the damaged region from the device static characteristics like threshold voltage and transconductance. The methods proposed in the literature for extraction of the amount and the spatial distribution of interface traps (and fixed oxide charge) are based on the drain–bulk gated-diode generation and recombination current at reverse bias [1] and forward bias [2,3], the gated-diode tunneling current [4] and the charge-pumping techniques [5,6]. Note that by the gated-diode generation-recombination current only the contribution of the mid-gap levels can be measured, and that the amount of the extracted traps is directly dependent on the corresponding capture cross-sections. In this study we will extract the spatial trap distribution by applying the conventional charge-pumping technique with the constant amplitude ΔU_G, rise t_r and fail t_f times, and variable gate top/base-levels U_{GH},U_{GL}. In this technique the emission times [7] are kept constant for all traps [6].
As device dimensions shrink the charge-pumping current I_{cp} becomes significantly influenced by several 2D effects [8,9]. Considering in particular the non-uniform hot carrier stress, the damaged region is located near and within the drain and source junctions, where 2D effects directly occur. In order to calculate quantitatively the contribution to I_{cp} from these regions we developed and implemented in MINIMOS a rigorous 2D transient model for the charge pumping experiment, which enables us to account properly for relevant effects [9]. In our approach, the dynamical-equations for energy- and space-discretized traps are coupled with the basic semiconductor equations in a self-consistent manner. This approach has been applied to study the geometric I_{cp} component in MOSFET's and SOI devices in [9] and to examine and improve the present techniques for the extraction of the spatial trap distribution in [6].

CHARGE-PUMPING CHARACTERISTICS OF LDD DEVICE'S

Fig.1 shows the comparison between numerically calculated charge-pumping characteristics $I_{cp}(U_{GL})$ and experiment for an n-channel LDD MOSFET before stress. There are two characteristic tails in I_{cp} for virgin LDD devices compared to conventional devices. We found for the first tail, which is located near the charge-pumping threshold ($-8.7V < U_{GL} < -7V$), that it originates from the whole LDD subdiffusion (gate/LDD overlap), while for the second small and long tail in the deep subthreshold region ($U_{GL} < -8.7V$) that it is produced by pumping the LDD region due to gate-edge electric field-fringing, Fig.2. For the first tail, the difference between the calculation and experiment could be either due to a non-uniform trap distribution in the subdiffusion region, or, most likely, due to an inaccuracy in the lateral doping profile obtained by process simulation. Although

we can reproduce the second long tail due to fringing effect the quantitative agreement has not been achieved for this region. While stressing n-channel LDD devices exhibit a continuous build up of traps in time, Fig.3. Traps are generated in the whole LDD subdiffusion region due to injection from the 'conventional field peak'. However, many more traps are generated in the LDD region near the gate edge under the LDD spacer

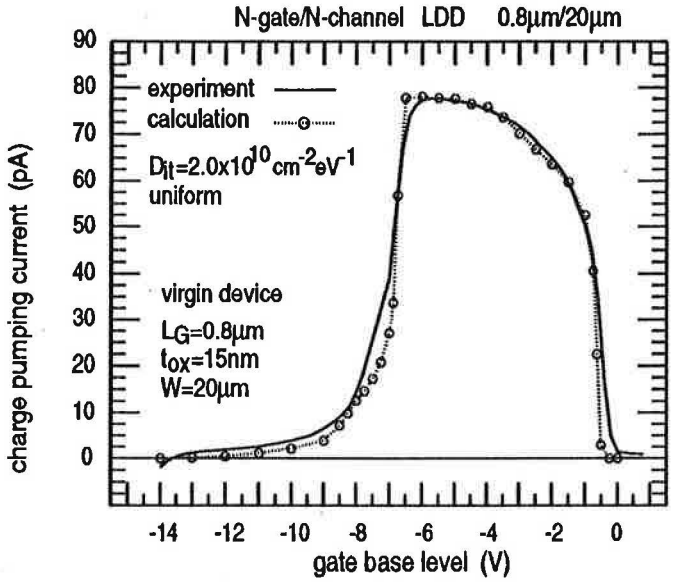

Figure 1: Comparison between experimental and numerically calculated charge-pumping curve for n-channel LDD MOSFET before stress (virgin device). Uniform spatial trap distribution is assumed. Trap density D_{it} is obtained by matching the current at $U_{GL} = -5.5V$. The geometric mean value of the capture cross-sections is extracted by the triangular-pulse method [7]: $\sqrt{\sigma_n \sigma_p} = 1.8 \times 10^{-16} cm^2$. Impurity distribution in device is calculated by process simulation. Note that no additional fitting has been performed. Pulse parameters: duty-cycle 50%, $f = 200$kHz, $t_{r,f} = 100$ns, $\Delta U_G = 7V$, $U_r = 0V$.

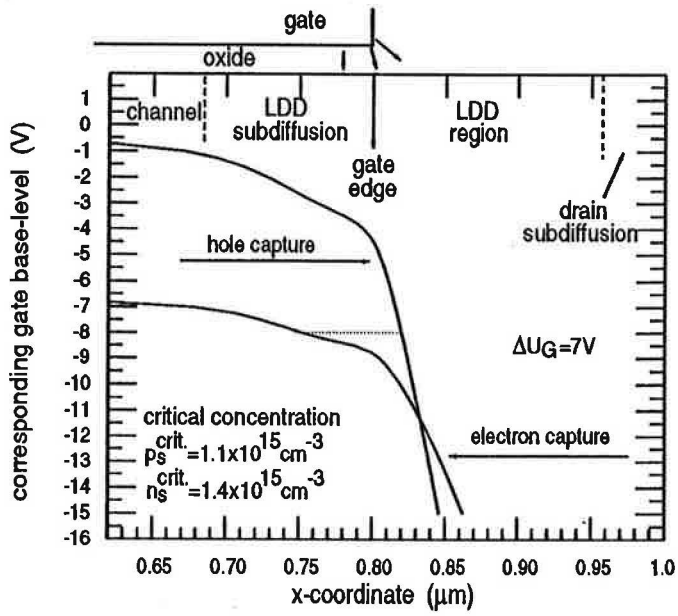

Figure 2: Edges of the area for the total capture of electrons (during the top pulse-level) and holes (during the base pulse-level) in virgin LDD device, which correspond to Fig.1. These edges are determined by a critical carrier concentration $n_s^{crit.}$, $p_s^{crit.}$ which is sufficient to refill all traps during the top(base) level $t_{H(L)}$ ([8]):

$$n(p)_s^{crit.} = \left(v_{thn(p)} \cdot \sigma_{n(p)} \cdot t_{H(L)}/3\right)^{-1}.$$

For a given gate base-level (e.g. $-8V$) the area between two calculated curves will completely contribute to the charge-pumping current (dotted line). Note that the electron-capture curve is shown with respect to the gate base-level, but it has been calculated for the top-level $U_{GH} = U_{GL} + \Delta U_G$.

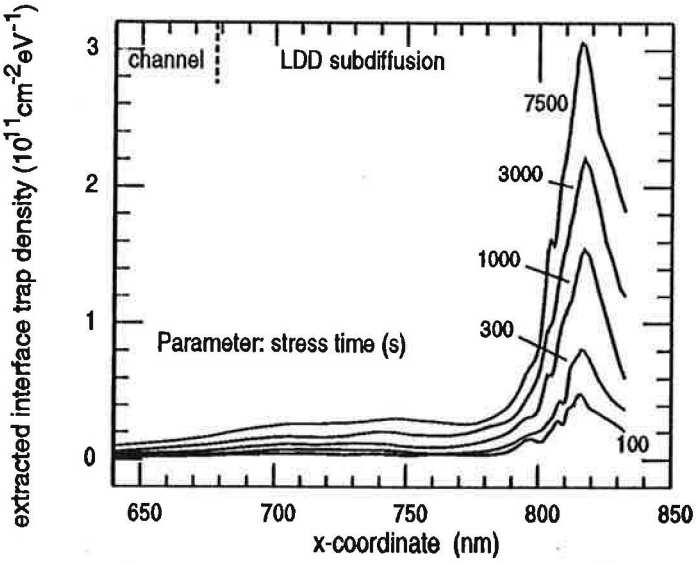

Figure 3: Extracted trap distribution in n-channel LDD device with stress time as parameter. Distributions from the channel to 810nm have been directly recalculated from the differential I_{cp} curves for $U_{GL} > -6.5V$; Fig.4. In this interval the distributions are less dependent on the uncertainness in the lateral doping profile and the local oxide thickness. Unlikely, the part from 810nm towards the drain is very sensitive to the device parameters involved in the gate-edge/LDD-region field-fringing. The calculated I_{cp} agree well with the experiment in the interval $U_{GL} > -8.7V$ (Fig.4), which confirms that the distributions are reasonable accurate for $x < 820$nm.

due to the contribution of the 'LDD field peak' [10], Fig.5. This fact has particular consequences on the reliability issue.

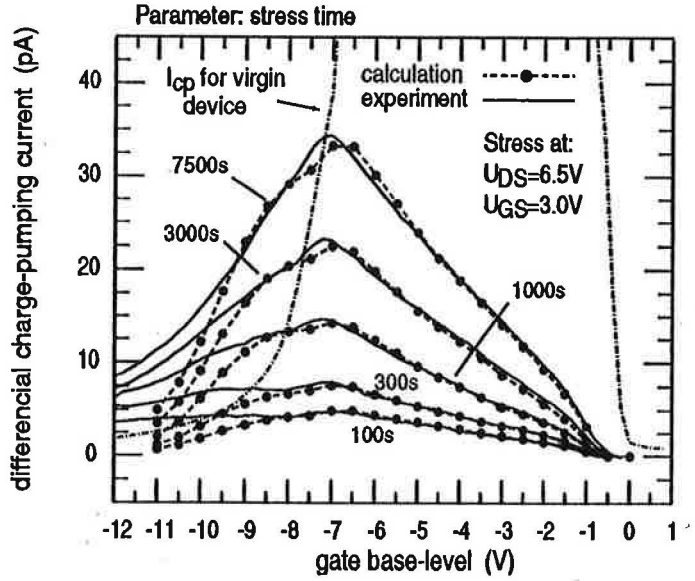

Figure 4: Numerically calculated difference between the charge-pumping current for stressed and virgin device (Fig.1) versus experiment. Parameter is stress time. Spatial trap distributions used in the calculation are given in Fig.3. For $U_{GL} > -4.5V$ the gate/LDD overlap contributes to the characteristics only. In the interval $-8.7V < U_{GL} < -4.5V$ both the gate/LDD overlap and the gate-edge/LDD fringing contribute to I_{cp}, while for $U_{GL} < -8.7V$ solely the gate-edge/LDD fringing effect produces the charge-pumping current. The parameters of the gate pulse used in the numerical simulation are given in Fig.1.

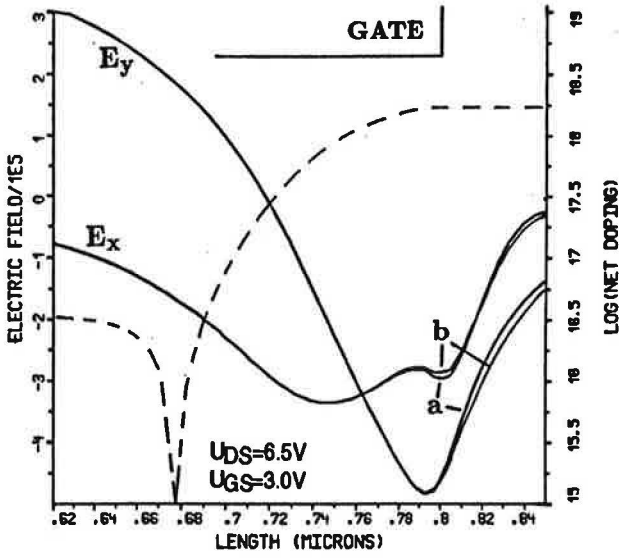

Figure 5: Lateral and tangential field distribution at the stress bias; a: before stress, b: after stress. Left broad peak is the conventional field peak, while the right peak close to the gate edge is the characteristic LDD field-peak. Due to a low generated trap density in the subdiffusion region (Fig.3) the shift of the conventional field peak towards the LDD region (as introduced in [11]) is negligible in the analyzed case. However, there is a small lowering of the LDD field peak. Dashed curve shows the lateral doping profile in the LDD region and the subdiffusion (gate/LDD overlap).

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REFERENCES

1. P.Speckbacher, A.Asenov, M.Bollu, F.Koch and W.Weber; IEEE Electron Dev. Lett. 11 (2) 95 (1990).
2. A.Asenov, J.Berger, W.Weber, M.Bollu and F.Koch; Proc. ESSDERC, 445 (1991).
3. A.Asenov, J.Berger, P.Speckbacher, F.Koch and W.Weber; Proc. INFOS, 247 (1991).
4. A.Acovic, M.Dutoit and M.Ilegems, IEEE Trans. Electron Dev. 37 (6) 1467 (1990).
5. M.G.Ancona, N.S.Saks and D.McCarthy; IEEE Trans. Electron Dev. 35 (12) 2221 (1988).
6. P.Habaš and S.Selberherr; Proc. SSDM, (August 1992).
7. G.Groeseneken, H.E.Maes, N.Beltrán and R.F.DeKeersmaecker, IEEE Trans. Electron Dev. ED-31 (1) 42 (1984).
8. P.Heremans, J.Witters, G.Groeseneken and H.E.Maes; IEEE Trans. Electron Dev. 36 (7) 1318 (1989).
9. P.Habaš, O.Heinreichsberger and S.Selberherr; Proc. ESSDERC, (Sept.1992).
10. M.Orlowski and C.Werner; IEEE Trans. Electron Dev. 36 (2) 382 (1989).
11. Q.Wang, W.H.Krautschneider, M.Brox and W.Weber; Proc. ESSDERC, 441 (1991).
12. W.Hänsch, C.Mazure, A.Lill and M.K.Orlowski; IEEE Trans. Electron Dev. 38 (3) 512 (1991).