ADVANCED MOS DEVICE ENGINEERING UTILIZING A TECHNOLOGY CAD FRAMEWORK [1]

Hubert Pimingstorfer and Siegfried Selberherr

Institute for Microelectronics, Technical University of Vienna
Gußhausstraße 27-29, A-1040 Vienna, Austria
Phone +43/1/58801-3850, FAX +43/1/5059224

Abstract

A TCAD framework has been developed which integrates process, device and interconnect simulation tools, a simulation database, a TCAD shell and a graphical user interface into a homogeneous environment. In this paper, the utilization of this framework for the development of advanced devices and the impact on computer-aided MOS device engineering will be demonstrated using several examples.

The use of CAD tools for analysis and prediction of IC technology is generally a substitute for experiments in order to save time, efforts and money, and to provide additional insight into process and device physics. We have integrated the required simulation tools into the technology CAD (TCAD) framework VISTA [1], featuring a common format for data exchange [2] and a TCAD shell [4], which provides for easy combination of all the different functional units through a of a powerful LISP-based command and extension language [3] for defining and solving high-level engineering tasks.

Short shell programs couple process simulation with several runs of a MOS device simulator [5] and postprocessing tools to automate the computation of I-V characteristics and to display them immediately. Taking advantage of the inherent parallelism of data independence, the device simulator is run simultaneously on several machines, making use of remote compute servers or workstation clusters.

The identification of the impact of variations in the fabrication process on device performance is a typical TCAD application. The effect of varying the spacer width, resulting from a not-so-easy-to-control back-etch process during spacer formation, on the device behavior in the strong inversion regime has been investigated for a high voltage p-channel MOSFET (Fig. 1).

For technology optimization, process and device simulation are coupled with an optimizer forming a closed loop. Extensive profile characterization is necessary to verify that all other specifications besides the optimized ones are met for the improved device. A well-known example is the bulk current minimization obtained by varying the LDD implant dose of an n-channel MOS transistor. The result is the I_b/I_d versus LDD implant dose diagram in Fig. 2.

The improvement of the punch-through immunity of a p-channel device has been subject of another investigation, also carried out by utilizing our VISTA system. This goal has been achieved by raising the well doping concentration and simultaneously adjusting the threshold adjust implant dose under the constraint of an unchanged threshold voltage.

[1] to appear in: Proc. Third International Conference on Solid State and Integrated Circuit Technology, ICSICT '92, Oct. 18-24, 1992, Beijing, China

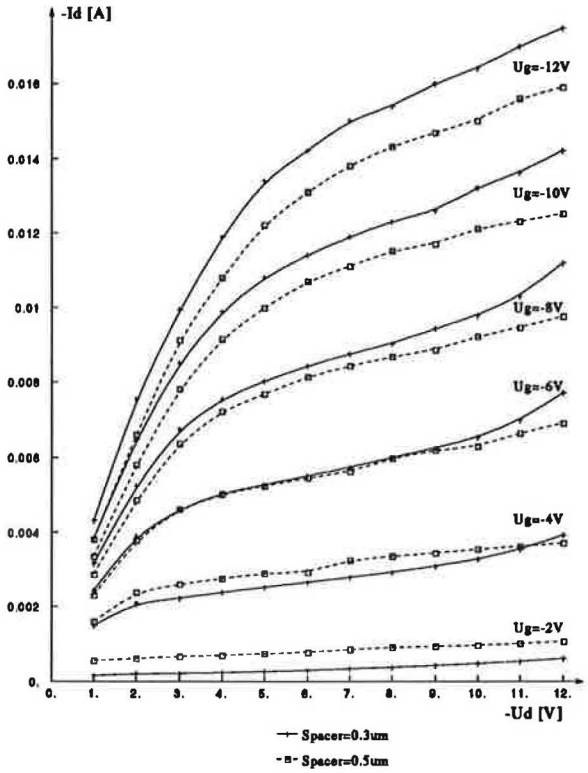

Figure 1: PMOS Drain Characteristic

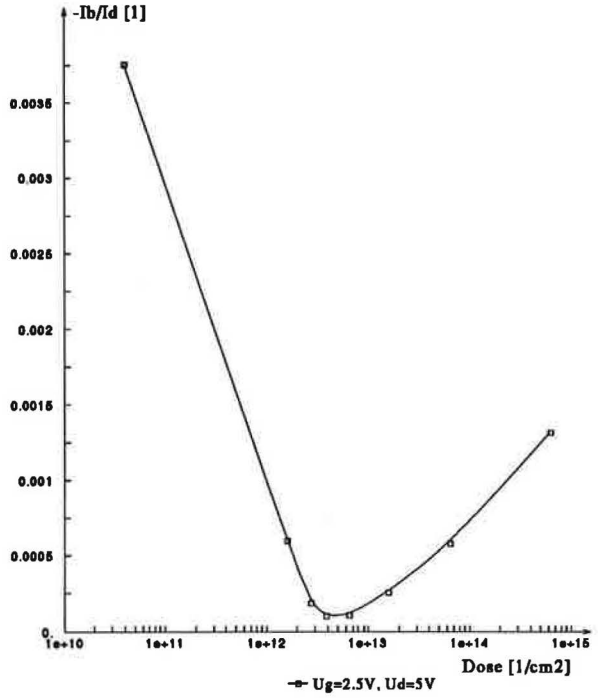

Figure 2: I_b/I_d vs. LDD Implant Dose

Substate current characteristics of a high-voltage n-channel MOSFET for different tilt angles of the LDD implant are shown in Fig. 3. Implanting at -12 degrees (from the drain towards the gate edge) lowers the substrate current dramatically. The lateral electric field maximum at the drain edge splits up into two peaks, one of it lying under the gate (Fig. 4). This arrangement reduces the device degradation and substantially improves the expected device lifetime [6].

Our TCAD framework adds value to the capabilities of the integrated tools with a uniform graphical user interface (Fig. 5), in automated simulator sequencing and closed loop optimizations. The aim of our TCAD framework is to ease and automate complex development tasks in process and device engineering, thus efficiently supporting the user in the design of tomorrow's MOS devices.

References

[1] S. Selberherr *et al.*, *The Viennese TCAD System*, Proc. International Workshop on VLSI Process and Device Modeling, Oiso, Japan, 1991.

[2] F. Fasching *et al.*, *A PIF Implementation for TCAD Purposes*, Proc. SISDEP, Vol. 4, pp. 477–482, Zurich, Switzerland, 1991.

[3] S. Halama *et al.*, *Consistent User Interface and Task-Level Architecture of a TCAD System*, Proc. NUPAD IV, pp. 231–236, Seattle, WA, 1992.

[4] H. Pimingstorfer *et al.*, *A Technology CAD Shell*, Proc. SISDEP, Vol. 4, pp. 409–416, Zurich, Switzerland, 1991.

[5] S. Selberherr, *Three Dimensional Device Modeling with MINIMOS 5*, Proc. Int. Workshop on VLSI Process and Device Modeling, pp. 40-41, 1989.

[6] Min-Liang Chen *et al.*, *Suppression of Hot-Carrier Effects in Submicrometer CMOS Technology*, IEEE Trans. Electron Devices, Vol. 35, No. 12, pp. 2210-2220, 1988.

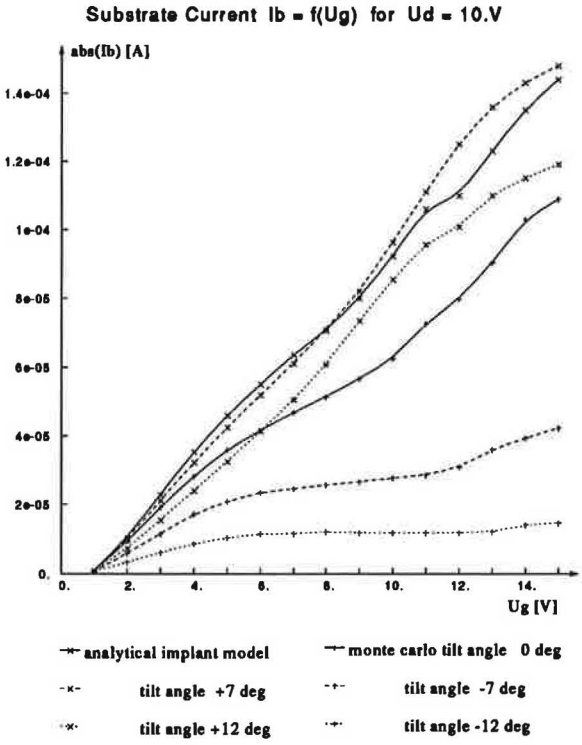

Figure 3: NMOS Substrate Current

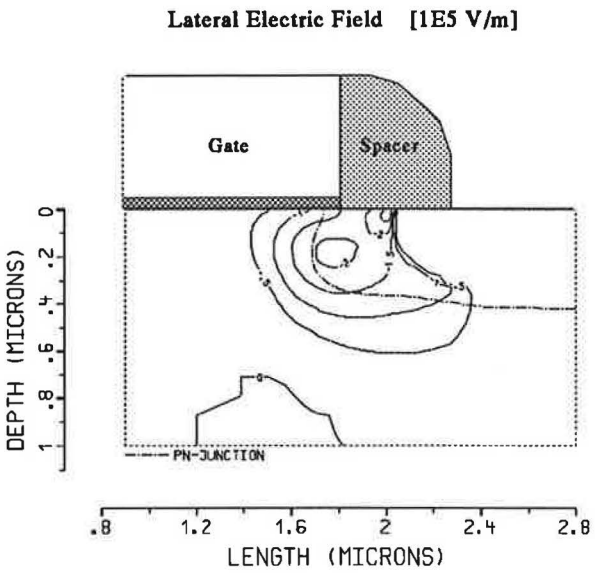

Figure 4: Electric Field in Drain Region

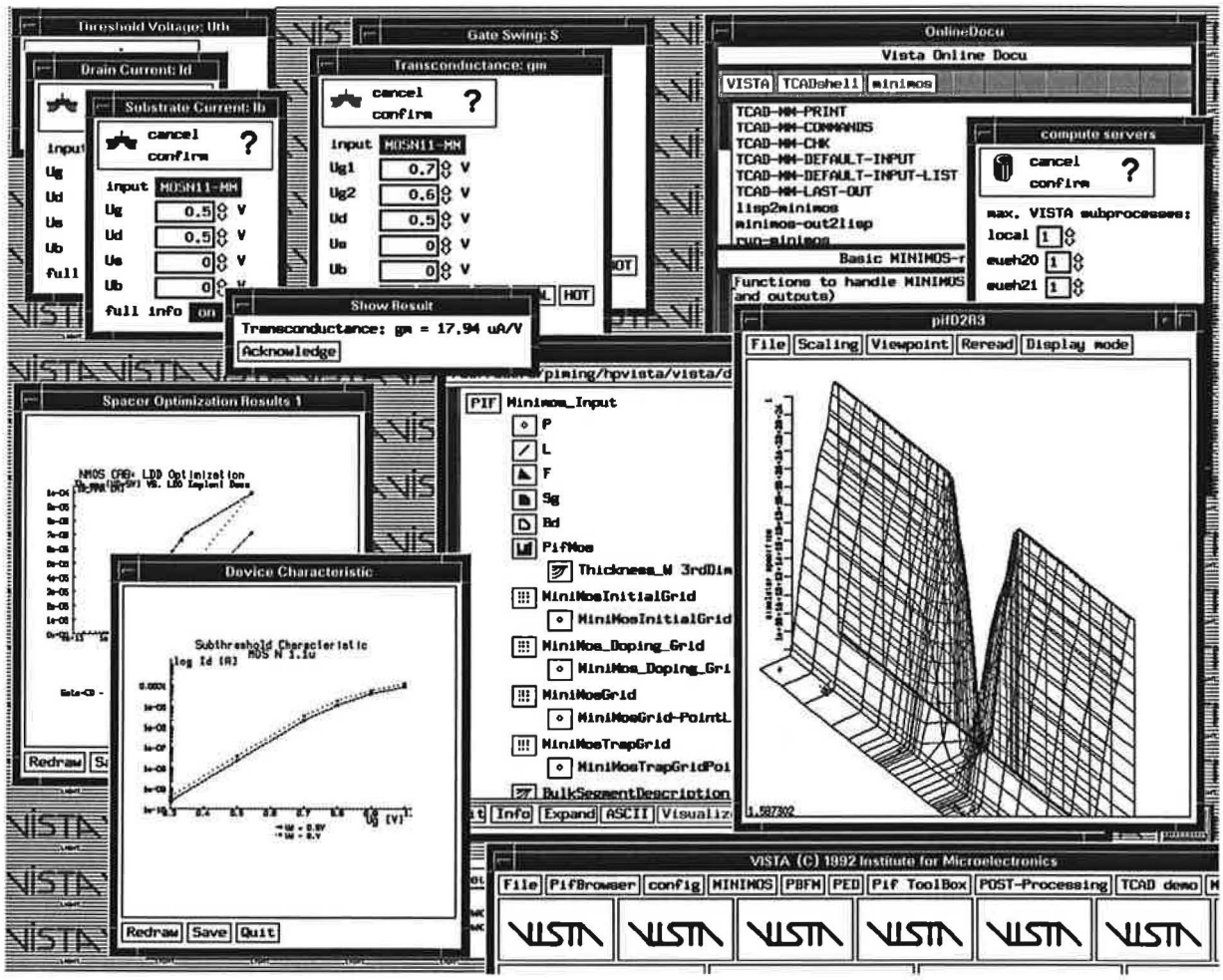

Figure 5: Example of VISTA's Graphical User Interface