Overvoltage Protection with a CMOS-Compatible BJT

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Abstract

A new method of overvoltage protection in the supply path of CMOS circuits is described. The central device of the protection circuit is a CMOS-compatible npn bipolar transistor (BJT) which uses no n^+ buried layer and can be manufactured in a simple p-well CMOS process without additional process steps. The device is especially suitable for high-voltage applications in electrically hostile environments such as automotive circuits.

1. Introduction

The protection circuit is essentially a series regulator (Fig. 1) which limits the internal supply to ≈16V and must handle a static overvoltage of 24V d.c. and overvoltage pulses of up to 80V at $t_r = 1\mu s$. In normal operation, the BJT must not saturate, because otherwise it would be a bypass for steep pulses. As the collector is contacted to the substrate, the circuit needs Zener diodes on its output too.

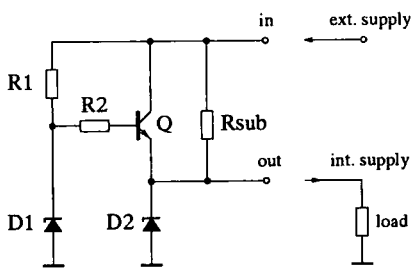

Figure 1: Series regulator

2. Integration of the Circuit in a CMOS Process

The proposed BJT uses a p-well as base and an n^+ S/D doping as emitter. The collector consists of the n^- substrate and does not require an n^+ buried layer or a highly doped substrate (Fig. 2,4). Four different structures (layouts of the BJT, Fig. 3) were designed and analyzed with the two-dimensional device simulator BAMBI 2.1 [2]. Using a high-voltage CMOS process, the S/D junction depth is $1.8\mu m$ and the p-well junction depth is about $6\mu m$, thus, the base thickness is $\approx 4\mu m$.

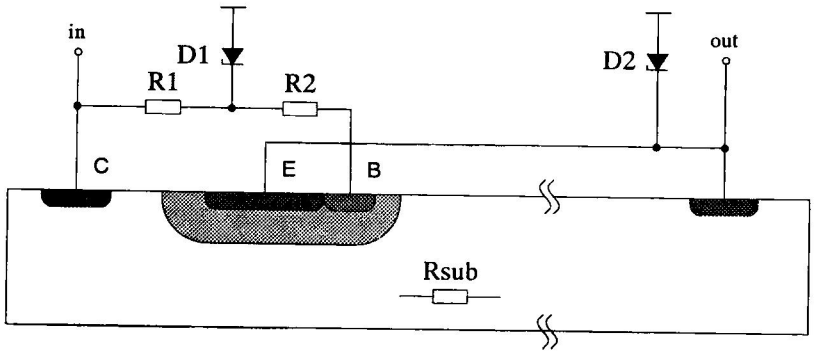

Figure 2: Integration of the protection circuit

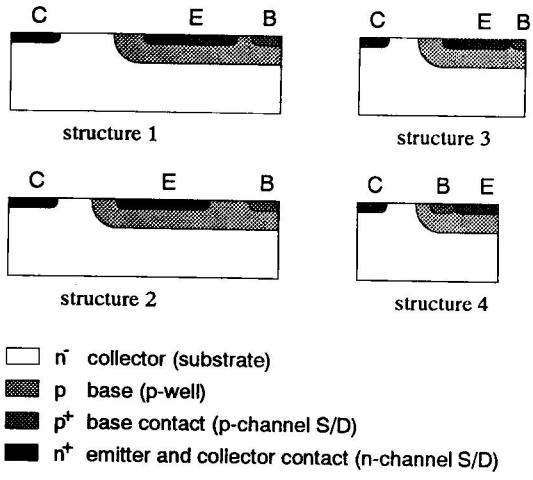

Figure 3: CMOS-compatible BJT structures

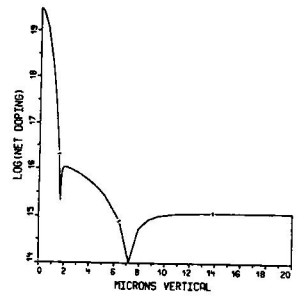

Figure 4: Vertical doping profile

The characteristics of the optimal structure are: $h_{FE} = 160$, $I_{KF} = 0.17\text{A/cm}$, $V_{AF} = 170\text{V}$, $\tau_F = 0.5\text{ns}$. The behavior of the BJT in typical operating and transient overload situations is shown in Figs. 7 and 8. The currents of the smaller structures 3 and 4 were scaled so that the comparision refers to the same total device area.

3. Optimization of the BJT

Due to the distributed collector resistance, the BJT exhibits a distinct quasi-saturation behavior which adversely affects the operation at low V_{CE} because of minority injection into the substrate. By optimizing the device, this effect can be kept sufficiently small even without a buried layer (Fig. 5). The optimization was performed by reducing both the emitter stripe width and the distance between emitter and collector to a minimum which is determined by high-level injection in the base. The vertical doping profile was not changed so that the NMOS and PMOS transistors on the chip are not affected (in particular, the substrate resistivity is confined to 3–5Ωcm).

The placement of the base contact has an essential impact on the dynamic and high-voltage behavior: The lateral part of the transistor limits the overall high-voltage performance due to the higher electric field at the surface, which is responsible for punch-through behavior, especially, when steep pulses are applied to the collector. However, if the base contact is placed between collector and emitter the p^+ doping at the base contact virtually eliminates the lateral BJT, which allows for higher V_{CE} and reduces the avalanche multiplication current at the surface (Fig. 6).

Fig. 9 and 10 show the influence of the resistor in the base branch. In Fig. 10 the emitter voltage overshoot for various currents is shown where the actual load current is 26mA. The additional voltage drop across R_b reduces the minority injection into the substrate so that the voltage overshoot is virtually not increased by the base resistor.

Further possible applications of the BJT include shunt regulators, solenoid drivers, and stepper motor drivers.

REFERENCES

[1] F. Berta, J. Fernandez *et al.*, *A Simplified Low-Voltage Smart Power Technology*, IEEE Electron Device Lett., pp. 465-467, 1991.

[2] W. Kausel, G. Nanz, S. Selberherr, H. Pötzl, *BAMBI – A transient two-dimensional device simulator using implicit backward Euler's method and a totally self-adaptive grid*, NUPAD II Workshop, May 9–10, 1988, San Diego, Ca., Digest No. 105/106.

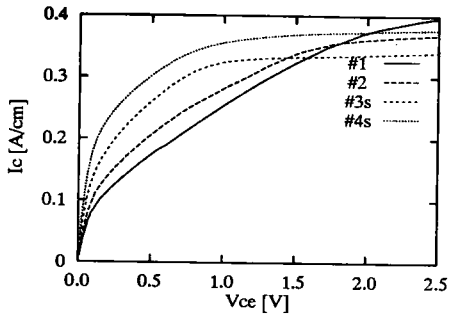

Fig. 5: Output-characteristics for different structures

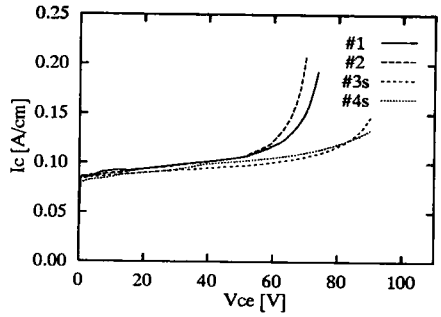

Fig. 6: Output-characteristics for different structures

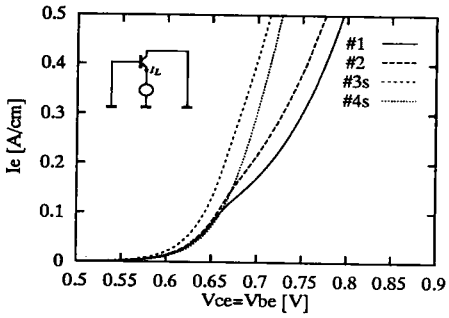

Fig. 7: Voltage drop vs. load current for different structures

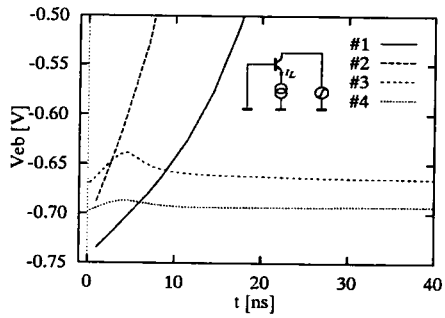

Fig. 8: Voltage overshoot at 80V/us, I=300mA/cm for different structures

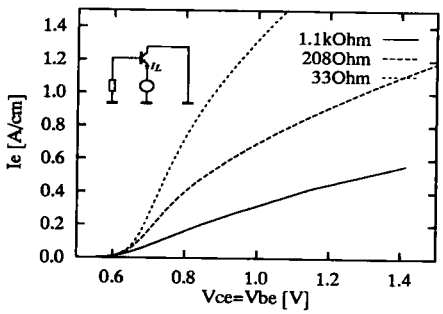

Fig. 9: Voltage drop vs. load current for structure 4 with various base resistors

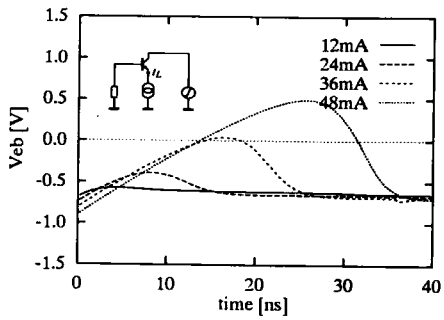

Fig. 10: Voltage overshoot at 80V/us, at various load currents for structure 4 with Rb=208Ohm