A Physically Based DC- and AC-Model for Vertical Smart Power DMOS Transistors

Martin Stiftinger†, Winfried Soppa‡, and Siegfried Selberherr†

†Institute for Microelectronics, Technical University Vienna
Gusshausstraße 27–29, A–1040 Wien, Austria

‡Bereich Halbleiter, SIEMENS AG
Balanstraße 73, D–8000 München 80, Germany

Abstract

Based on device simulations an analytical DC- and AC-model for vertical DMOS transistors has been developed. It is based on a subcircuit approach. An enhanced MOS model for the channel and an adapted JFET model which accounts for drift velocity saturation in the drift region are used. As in existing approaches both the nonconstant doping in the channel region and the AC-behavior of the DMOS have not been thoroughly investigated special attention is paid to these aspects. Comparisons with numerical device simulations are presented to confirm the physical correctness of the new approaches.

1 Introduction

Smart Power DMOS transistors (see Fig. 1) serve primarily as interface between digital control logic and the power load (DMOS-switches can consist of up to 10.000 cells). Since they are also used in analog applications (e.g. as a single cell transistor) there are high demands on the accuracy of analytical models for circuit simulation.
Extensive device simulations with MINIMOS [5] and BAMBI [1] have led us to develop a subcircuit approach for an analytical model which is shown in Fig. 2. As circuit simulations of DMOS transistors have often to be performed in complex circuits (integrated technology) one of the major goals was to use as little elements in the subcircuit as possible to keep simulation times short.
The channel is represented by an enhanced analog MOSFET model which also accounts for the strongly nonuniform channel doping profile in lateral direction, the drift region is approximated by a modified JFET model which includes the drift velocity saturation in the epi-layer. The gate-drain capacitance is modeled by a nonlinear capacitance, while parasitic behavior under reverse bias is described by standard bipolar transistor models.

2 Drift region

The modified JFET model accounts for the special geometry of a DMOS cell (see Fig. 3) [6] and drift velocity saturation which has important influence on the quasi-saturation behavior

(only slight dependence of the drain current on V_{GS} for high gate voltages) of the device [2]:

$$I_D = \frac{A_d q N_{epi} \mu_{epi}}{x_d (U_{bi} - U_p)} \cdot \frac{\left(U_{BD} - U_p - \frac{1}{2} U_{dD}\right) U_{dD}}{\left(1 + \left(\frac{U_{dD}\mu_s}{x_d v_{max}}\right)^a\right)^{1/a}} \quad \text{with} \quad U_p = U_{bi} - \frac{q N_{epi} (L_p - 2x_{body})^2}{8\epsilon_s} \tag{1}$$

For μ_s the perpendicular field reduction of the mobility in the epi-layer is taken into account, x_d is the vertical extent of the space charge region, which can also easily be calculated. A_d is the maximal area for the vertical current flow. U_{dD} denotes the voltage between drain and the drain end of the channel (nodes 22 and 11 in Fig. 2).

3 Channel

The channel doping profile is defined by the different lateral subdiffusions of n^+-source and p-body and is analytically approximated by [3]

$$N_A(x) = N_A(0) \exp\left(-\eta \frac{x}{L}\right) = N_{A0} \exp\left(-\eta \frac{x}{L}\right) \tag{2}$$

where N_{A0} is the channel doping concentration on the source end of the channel. The only approximation made when including equation (2) in our model is the assumption of a linearly distributed channel potential. This can be justified by observing that the carriers reach their saturation velocity v_{sat} first on the source end of the channel (higher doping concentration) and then move with v_{sat} through the channel and by the quasi-saturation behavior of the drift region which keeps the voltage across the channel sufficiently low (no classical pinch-off).
In the DC-case the result are two additional terms in the drain current. The first term increases the effective gate-source voltage (i.e. decreases threshold voltage), the second decreases the bulk depletion charge C_{dB}. Both lead to a higher drain current and are plotted (N is a normalization factor) against the "steepness factor" η in Fig. 4. η simply is the logarithm of the ratio of the doping concentration at the source and the drain end of the channel, where an exponential shape is assumed.
The higher drain current can physically be explained by a higher channel conductivity due to a smaller depletion charge at the drain end of the channel. Numerical device simulations with PISCES [7] and MINIMOS confirm this result. Fig. 5 shows the influence on the input characteristic with a clear decrease of the threshold voltage, Fig. 6 that on the output characteristic. For $\eta = 0$ the "classical" result is obtained.
This approach can also be used to generalize a charge based capacitance model [4] for nonconstant channel doping. The drain charge e.g. in this model reads (U_C is the channel potential):

$$Q_D = -WL \frac{\int_0^{U_{DS}} q^2 n^2(U_C) \int_0^{U_C} qn(U_C') \, dU_C' dU_C}{\left(\int_0^{U_{DS}} qn(U_C) \, dU_C\right)^2} \tag{3}$$

Instead of the channel charge in the classical case

$$qn(U_C) = C_{ox} (U_{GSeff} - (1 + \kappa f_B) U_C) \tag{4}$$

the expression

$$qn(U_C) = C_{ox} \left(U_{GS} - U_{FB} - 2\Phi_F - U_C(x) - f_{B0} \exp\left(-\frac{\eta}{2} \frac{x}{L}\right) (2(2\Phi_F - U_{BS}) + \kappa U_C(x))\right) \tag{5}$$

is used. For $\eta = 0$ also in this case the "classical" results are obtained. Also the AC-description of the depletion regime includes the dependency on the "stepness" of the channel doping. Comparisons with AC device simulations of a MOSFET with nonconstant doping profile performed with PISCES and the analytical model (Fig. 7 and 8) show clearly that the new approach is both a considerable improvement over the "classical" model and physically sound. The curves in Fig. 8 have neither been fitted to those in Fig. 7 nor have overlap- and junction-capacitances been taken into account in the curves in Fig. 8.

Acknowledgement

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References

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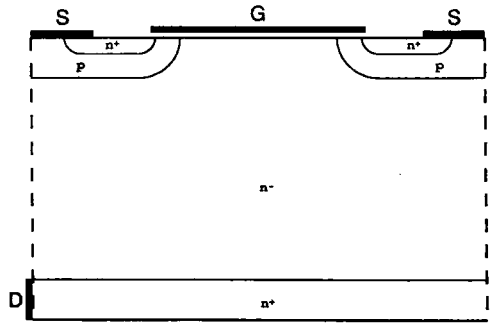

Fig.1. Structure of the vertical DMOS transistor

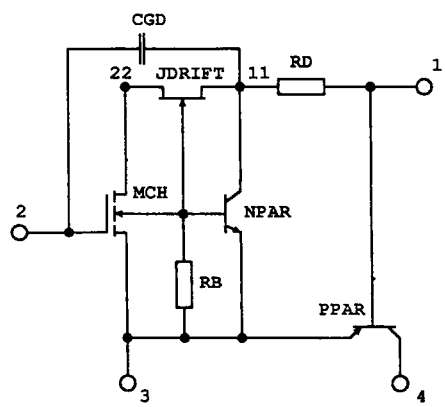

Fig.2. Subcircuit model for the vertical DMOS transistor

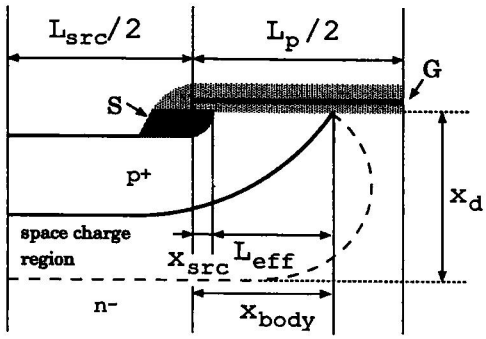

Fig.3. Geometry of the DMOS cell for the modified JFET model

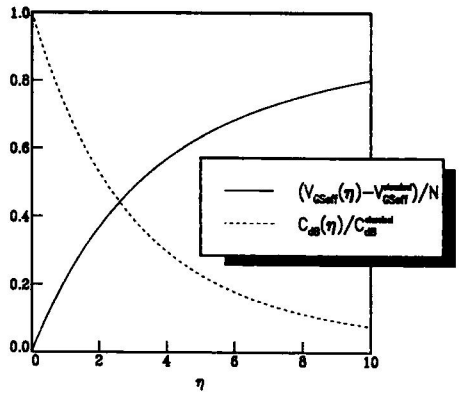

Fig.4. $U_{GSeff}(\eta) - U_{GSeff}^{classical}/N$ and $C_{dB}(\eta)/C_{dB}^{classical}$ over η

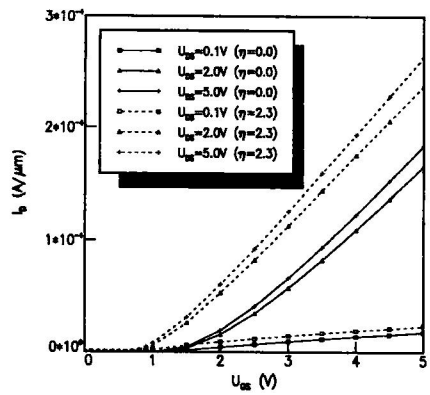

Fig.5. Numerical simulations of input characteristic for uniform and non-uniform channel doping profile

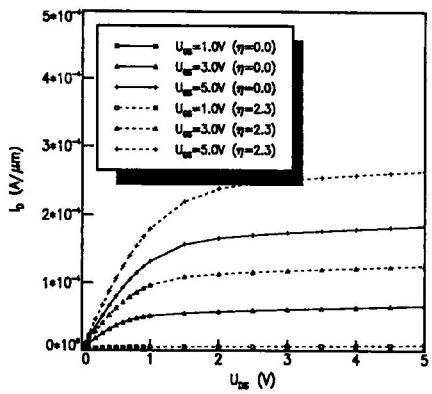

Fig.6. Numerical simulations of output characteristic for uniform and non-uniform channel doping profile

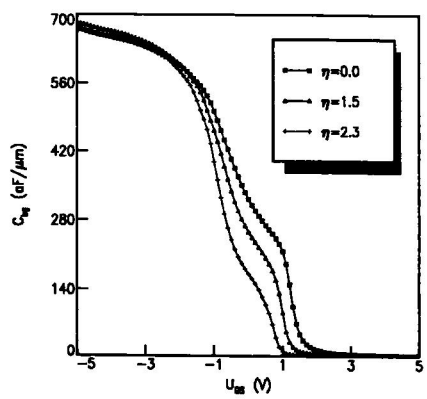

Fig.7. Numerical simulations of C_{bg} over U_{GS} for uniform and non-uniform channel doping profile

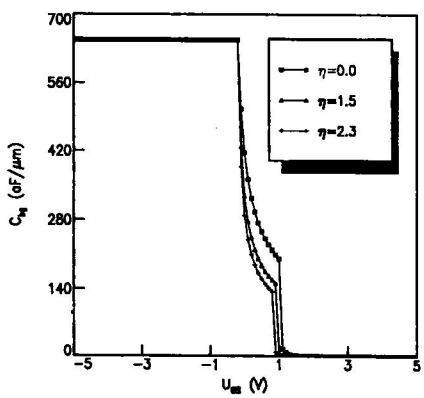

Fig.8. C_{bg} over U_{GS} for uniform and non-uniform channel doping profile in the analytical channel model.