Analysis of the Fabrication Process of Multilayer Vertical Stacked Capacitors

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Abstract

The increased complexity of new capacitor cell structures for high-density dynamic RAMs requires an accurate description of the fabrication process. We present a three-dimensional topography simulation of a stacked capacitor cell, using a new simulation method for etching and deposition processes. Sequential process steps are simulated and results are shown in comparison to a measured cell structure.

1. Introduction

Several capacitor cells have been proposed to achieve high-density dynamic RAMs. To obtain sufficient cell capacitance, horizontal [1] and vertical [2] [3] multilayered cell structures have been studied. The Multilayer Vertical Stacked Capacitor which was proposed in [4] is suited for 64Mbit and 256Mbit dynamic RAMs. Fig. 1 shows the process sequence of such a cell structure.

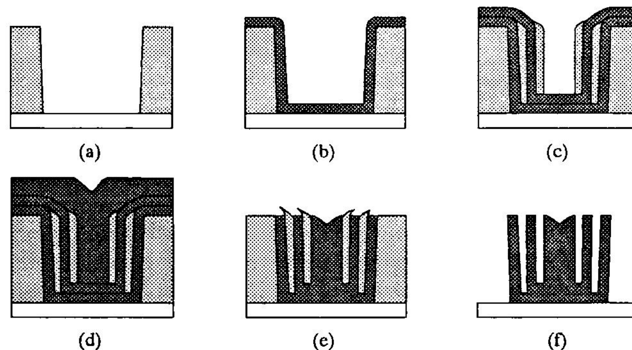

Figure 1: Process flow of capacitor cell

After transistor and bitline process subsequently a PSG layer is deposited and the storage node is patterned. The slope of the storage node reduces vertical layer deposition and is controlled by the etching process. Multiple layers of storage node PolySi separated by

oxide spacers serve to enlarge the area of the stacked capacitor as shown in Fig. 1c. Then the capacitor is refilled and planarized with a doped PolySi layer. Oxide removal with wet etching and cleaning concludes the first plate formation as shown in Fig. 1f. Finally, ONO dielectric is deposited and the top cell plate is formed.

2. Simulation Method

A variety of surface evolution algorithms has been reported to build three-dimensional topography simulators. Many algorithms such as ray tracing and volume removal methods are used for lithography simulation [5], [6]. A few methods have been applied to three-dimensional simulation of etching and deposition processes [7]. Surface advancement algorithms offer highly accurate results but with potential topological instabilities such as erroneous surface loops. Our new simulation method is based on morphological filter operations for advancing the etch front. By use of a cellular material representation our method allows the accurate and absolutely stable simulation of arbitrary structures.

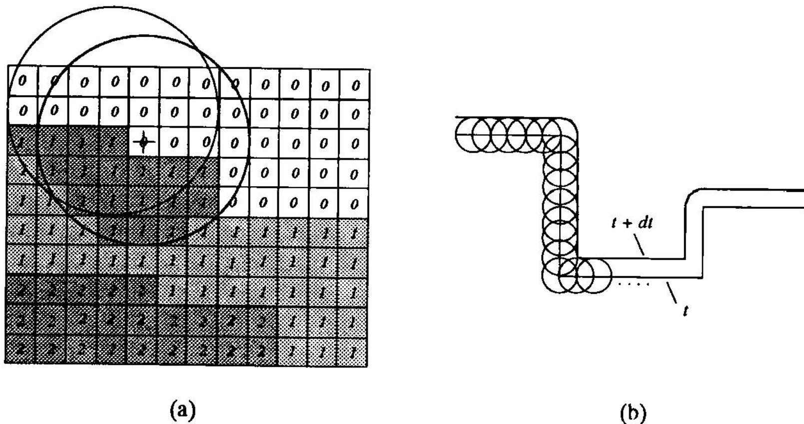

Figure 2: Simulation method

Each geometry cell is characterized as etched or unetched. A material identifier is defined for each cell, therefore material boundaries need not be explicitly represented. To advance the etch front adaptive spatial filter operations are performed along the surface boundary as shown in Fig. 2. These filter operations are based on Minkowski algebra which allows to simulate topography processes by use of the fundamental morphological operations of erosion and dilation, as they are termed in image processing [8]. During etching, all cells within a filter are etched away, while cells outside stay unchanged. In general, for anisotropic simulation filters are ellipsoids, for isotropic movement of surface points filters are spheres. The spatial filter dimension is related to the simulation time step and to the local etch rates. The etch front at a given time step is obtained by the envelope of filtered cells.

With our method we avoid the inherent inaccuracy of the original cell algorithm [9] which in two dimensions produces an octagon instead of a circle during uniform etching from

a single point [10]. Choosing an appropriate filter shape the simulation of etching with preferred etch directions such as in crystalline etching is also possible.

Filter operations at material boundaries are performed using composite filters. In general, interfaces lead to an abrupt change in etch rates. For this reason, on both sides of the interface a filter operation has to be performed selectively to the actual material. Filters which extend over a material boundary demand an additional filter operation for this time step. The etch rates for those filters depend on the etch rates on both sides of the interface and on how far a filter reaches into the other material.

3. Simulation Results

Fig. 3 shows a cross section through the simulated cell structure after the second spacer formation. The simulation starts from a planar oxide layer. First the storage node is etched using a circular mask. The plasma assisted etching process is modeled using an isotropic and a directional etch rate component. Directional etching only takes place at unshadowed regions. The slope of the resulting structure is controlled by the ratio of isotropic to directional etch rate. Next, isotropic deposition of PolySi is performed followed by isotropic deposition of oxide. The oxide is then etched back with high directional rate to form the first oxide spacer. Isotropic PolySi deposition and the two process steps for the spacer formation are then repeated to obtain the simulation result shown in Fig. 3.

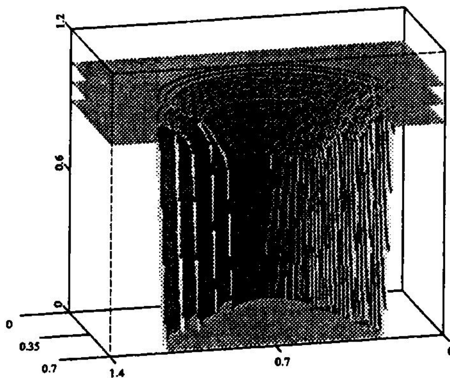

Figure 3: Cross section after second oxide spacer formation

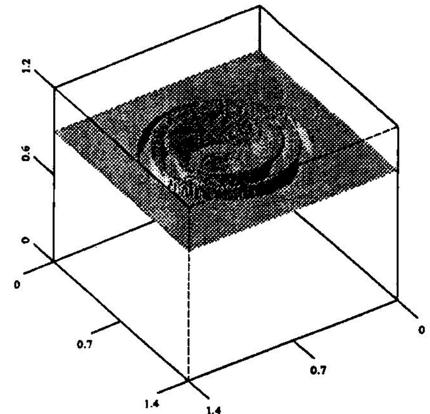

Figure 4: Top view after etch back of polysilicon

As a next simulation step the capacitor cell is refilled by isotropic deposition of a thick PolySi layer. The etch time of the following etching process of PolySi determines the resulting height of the capacitor. Fig. 4 shows the capacitor after etching back PolySi. At the top of the simulation region a part of the oxide spacers can be seen. Finally the oxide is removed by an isotropic etching process. Fig. 5 shows the final simulation result of the capacitor cell. The crater at the center of the top is formed during the planarizing

step and can also be observed in Fig. 6 which shows a SEM of the original cell structure taken from [4]. The diameter of the simulated cell structure is $1\mu m$ at the top of the cell, the capacitor height is 800nm and the wall thickness is 80nm. The simulation region was divided in 200x200x200 geometry cells. The total CPU time was 118 minutes on a HP 9000/755.

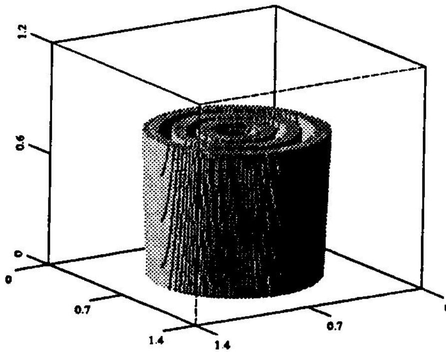

Figure 5: Simulation result after oxide removal with wet etching

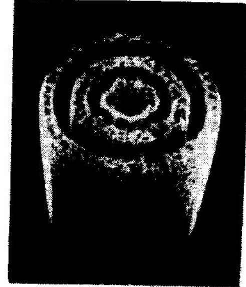

Figure 6: SEM of capacitor cell [4]

4. Conclusion

The fabrication process of a Multilayer Vertical Stacked Capacitor was simulated using a new simulation method based on morphological filter operations. In comparison to a measured cell structure the accuracy and the generality regarding the simulation geometry of this method were demonstrated.

Acknowledgements

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