A Novel Method for Extracting the Two-Dimensional Doping Profile of a Sub-Half Micron MOSFET

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Abstract

A novel method for extracting the two-dimensional doping profile of a sub-half micron gate length MOSFET from capacitance measurements is presented. The method is able to resolve the lateral doping profile of a MOSFET, even for very shallow junctions with 0.1 micron lateral extent. It does not require any "heroic" sample preparation and uses measurements easily performed during process characterization, such as gate overlap and source/drain diode capacitances.

Introduction

Inverse modeling [1] provides an alternative method to determine dopant profiles. The method is not hindered by the limitations of direct experimental measurement techniques when applied in two dimensions and on the very shallow junctions of modern technologies. In [2] a methodology for determining the 2D doping profile from MOSFET and source/drain diode capacitance measurements by inverse modeling was described. The method is based on the Tensor Product Spline (TPS) representation of the donors and acceptors profiles in a device, and the extraction by nonlinear least squares optimization of the individual B-splines coefficients. In this paper, we will present the results of applying our methodology to the determination of the 2D doping profile of a 0.4 μm gate length, large-angle-tilt implanted drain (LATID) N-channel MOSFET [5].

Extraction Algorithm

Using the TPS representation with fixed knot sequences, the net doping can be expressed as a nonlinear function of the spline coefficients for the acceptors and donors. Because of the interdependence between the donors and acceptors, we perform a coupled solution of the non-linear least squares problem. At each iteration we perform one step of the Levenberg-Marquardt algorithm [3] for the donors and acceptors respectively. We use forward differences to calculate the Jacobian and limit further approximations (i.e. [4]) which can cause the trapping of the solution in local minima.

Results

We use data from a CMOS process with a physical polysilicon gate length of 0.4 μm. The oxide thickness is 9.5nm as measured in accumulation. The NMOS device received a phosphorus LATID and a heavy arsenic implant, and has an effective length of 0.26 μm. Starting from the one-dimensionsal (1D) source/drain (S/D) donors profile from secondary ion mass spectroscopy (SIMS), we use the reverse junction diode area capacitance to determine the 1D acceptors profile. Figure 1 shows the resultant 1D net doping, and figure 2 shows the corresponding fit to the diode data. We then extract the 1D channel doping from deep-depletion CV measurements taken on a large square capacitor. To generate the 2D starting profile we rotate the S/D donors 1D profile, and spread the channel acceptors profile laterally except in the S/D region where we use the profile extracted in the preceding step. We also adjust the donors subdiffusion to yield the measured electrical effective channel length. The resultant 2D profile is shown in figure 3. This initial 2D profile is commonly used as input for device simulation.

Gate to S/D capacitance (Cov) data as a function of gate and substrate bias were measured on a structure with many polysilicon fingers over active area and divided by the total perimeter length (740 μm). The diode periphery capacitance as a function of gate and substrate bias was also measured on the same fingered polysilicon structure. The gate capacitance data is shown in figure 4 together with the simulated capacitances using the initial 2D profile.

We then perform an optimization to extract the TPS coefficients from the overlap and diode data. The final profile is shown in figure 5. We show in figure 6 the gate overlap experimental capacitance data together with the simulated capacitance calculated using the extracted 2D profile. The fit improvement seen by comparing figures 4 and 6 is apparent. Besides device structure and geometry, the dopant distribution is the main input in solving Poisson's equation to calculate the capacitance values. By matching the experimental capacitance measurements, the extracted profile is an accurate representation of the net dopants distribution in the device.

Conclusion

By making use of the full overlap and diode data, it is possible through optimization to extract the 2D profiles of sub-half micron MOSFET. Accurate 2D profiles are crucial for device characterization and an important input for device simulation.

References

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[3] D. W. Marquardt, SIAM, Vol. 11, 1963, 431-441.
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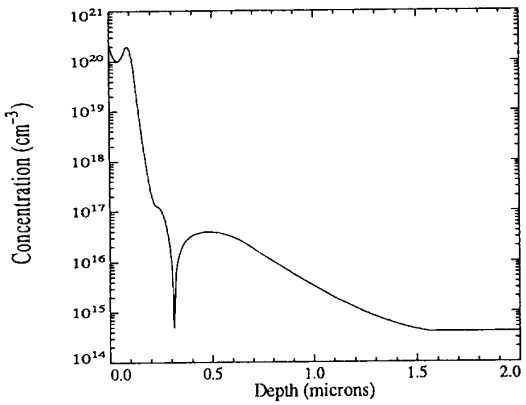

Figure 1: Source/Drain net doping.

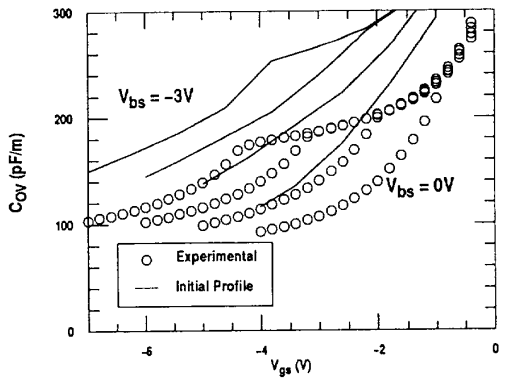

Figure 4: C_{ov} vs V_{gs} before extraction.

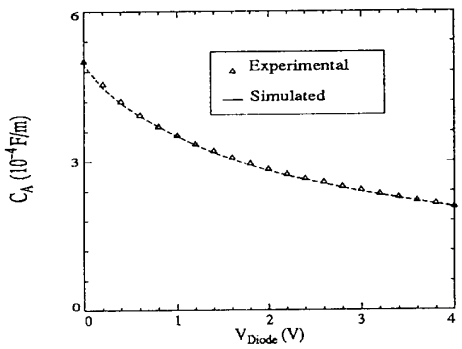

Figure 2: Diode area capacitance fit.

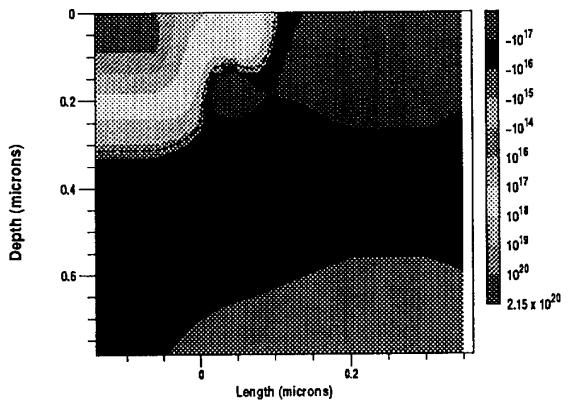

Figure 5: Extracted 2D profile.

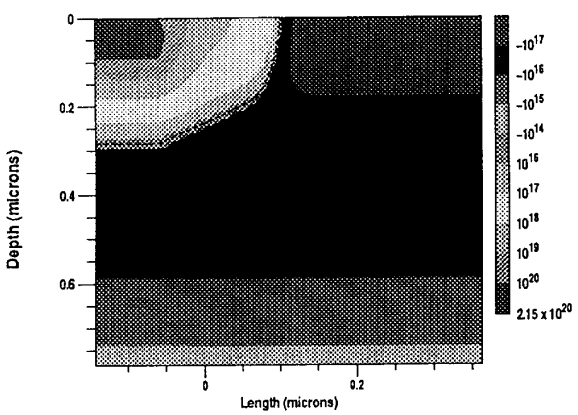

Figure 3: Initial 2D profile.

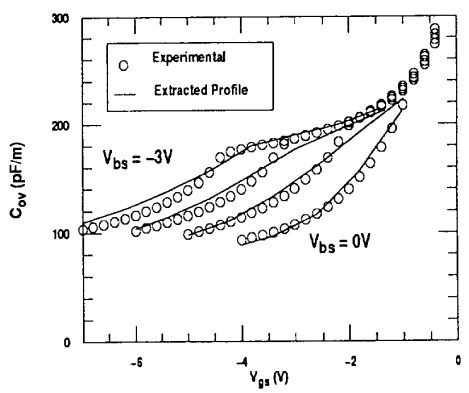

Figure 6: C_{ov} vs V_{gs} after extraction.