A SCALABLE PHYSICALLY BASED ANALYTICAL DMOS TRANSISTOR MODEL

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Abstract

An analytical DMOS model for circuit simulation based on a subcircuit approach is extended for a variable number of cells. The subcircuit itself consists of a minimal number of elements whose models are physically based and optimized for the special DMOS structure. The DC-description is continous (smooth transitions between the different operating regions of the device), the AC-description is charge based and the model also accounts for temperature effects. Over a wide range of cell numbers the same parameters can be used due to the scalability of the model.

1. Introduction

One of the main advantages of the vertical concept for power MOS-devices is the possibility of adapting the on-resistance by a variable number of parallel cells (up to 10000 in our case). The used technology is optimized to the n-channel DMOS transistor but also allows the integration of all other important devices like *n*- and *p*- channel MOSFETs, *npn*- and *pnp*-bipolar transistors and a (lateral) high-voltage *p*-channel transistor. This allows gate-driving, logic, and all kinds of protection circuits to be integrated on the same IC (Smart Power Technology). The DMOS transistor is usually used as a switching device but e.g. in control circuits it is also used in the analog region (V_{gs} not far above V_{th}) and therefore high accuracy of the model is demanded. Transient simulations of the switching behavior require an accurate AC-model. Especially the fact that the gate contact is extended over the drift region between adjacent cells (to improve the forward blocking capabilities and the on-resistance) and the rather large drain resistance slow down the switching speed (Miller effect). Especially when switching inductive loads a considerable amount of power is dissipated in the device and can lead to self heating.

2. The Model

The DMOS transistor (structure see Fig. 1) is described by a subcircuit with a minimal number of elements (see Fig. 2) in order to keep simulation times low also for complex circuits. On the other hand the models describing the elements in the subcircuit have been extended (in comparison to standard models) to account for the special situation in the DMOS transistor to make the DMOS model as accurate as possible [5].
The model for the MOSFET describing the channel accounts e.g. for the strongly non-constant channel doping profile in lateral direction both for the DC- and the charge

based AC-description [5], the JFET model takes the geometry of the DMOS transistor into account [4], and the resistor R_D is modeled according to [1]. This model also depends on the geometry of the cell and assumes a 45° current flow angle [2] (see Fig. 1).
We have implemented two levels of C_{gd} capacitances for the DMOS transistor model. The first one allows a good description only above the threshold voltage and is defined by the charge Q_{gd}:

$$Q_{gd} = \begin{cases} AC_{ox}\gamma\left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} - V_{gd} + V_{fb}}\right) & \text{for} \quad V_{gd} < V_{fb} \\ AC_{ox}\left(V_{gd} - V_{fb}\right) & \text{for} \quad V_{gd} \geq V_{fb} \end{cases} \tag{1}$$

with the flatband voltage of the interface between drift region and gate oxide V_{fb} and $\gamma = \frac{\sqrt{2\epsilon_{si}qN_{epi}}}{C_{ox}}$.
The second model is based on the calculation of the surface potential of the drift region v and is given by

$$v = V_{gd} + \frac{q_{sc} + q_{fix} + q_{if}}{C_{ox}} - v_{ms} \tag{2}$$

with the surface-, fixed-, and interface-charges q_{sc}, q_{fix}, and q_{if} and the workfuncion v_{ms}. As q_{sc} depends nonlinearly on v

$$q_{sc} = -\sqrt{2q\epsilon_{si}N_D U_T}\sqrt{\frac{n_i^2}{N_D^2}\left[\exp\left(-\frac{v}{U_T}\right) - 1\right] + \exp\left(\frac{v}{U_T}\right) - 1 + \frac{v}{U_T}\left(1 - \frac{N_A}{N_D}\right)} \tag{3}$$

we use a feature of the circuit simulator of our choice SABER [3] which allows implicit equations simply to be written into the device description in the input deck. A virtual node (corresponding to v) is automatically added to the subcircuit and the surface potential is calculated in the nonlinear solution process. This method allows a proper modelling of capacitances for all bias conditions, but is slower than the first model.
Using the same feature of SABER also self heating can be considered. The heat dissipated in the device is determined and a very simple thermal network consisting of a thermal resistor and a thermal capacitor allows the calculation of the device temperature. The temperature itself then influences the device behavior (especially the drain resistance and the threshold voltage).

3. Scalability

All existing DMOS models are restricted to a fixed number of cells. As all of our device models in the subcircuit are geometry dependent a scaling of all subcircuit elements to a variable number of cells is possible. For the channel MOSFET only the width has to be scaled (all other width dependent MOSFET parameters like capacitances are internally scaled to the channel width). The definition of the channel width for the DMOS transistor is not totally straightforward as the source side of the channel can approximately be regarded as the perimeter of a square (looking at the DMOS cell from above). The length of one side is $2Z$. The drain end of the channel is the perimeter of a square with the length of one side of $2(Z + L)$ where L is the channel length (see Fig.1). The channel resistance is given by (with the channel doping N_A):

$$R_{ch} = \int_{Channel} \frac{dx}{W(x)q\mu C_{ox}N_A} \tag{4}$$

Applied to the DMOS cell this reads (under the simplifying assumption of a constant channel doping):

$$R_{ch} \propto \frac{1}{8L} \int_{Z}^{Z+L} \frac{dx}{x} = \frac{1}{8L} \ln\left(1 + \frac{L}{Z}\right) \tag{5}$$

Compared to a constant W and with the number of cells N the scaled channel width is

$$W = N \frac{8L}{\ln\left(1 + \frac{L}{Z}\right)} \tag{6}$$

To account for the fact that the influence of the JFET for the cells at the border of the cell array is much lower a second JFET with a much more negative pinch-off voltage is added in parallel to the first one. The areas of the device contributing to inner and outer cells can easily be calculated. Also the drain resistance, the parasitic bipolar devices, and the gate-drain capacitance can easily be scaled. According to the design rules and the layout of our process the geometrical areas affecting all elements in the subcircuit and their influence on the model parameters are calculated in a sort of preprocessing step out of the number of cells. This allows a good description of both the DC- and the AC behavior of DMOS transistors from few up to some thousands of cells with the *same* parameter set.

4. Results

Fig. 3 and 4 show the input charcteristics for a 60- and 80-cell DMOS transistor, in Fig. 5 R_{on} for low drain voltage and three different temperatures is shown for a 4000-cell DMOS transistor (our equipment didn't allow to make measurements for higher currents). We have also included a simple model for the influence of the self heating of the device which is shown in Fig. 6 for a 60-cell DMOS transistor. Fig. 7 shows the first capacitance model for a 60-cell DMOS transistor, Fig. 8 the second capacitance model for a 80-cell DMOS transistor. For all figures the same parameter set has been used. Good agreement with the measured data can be observed.

Acknowledgement

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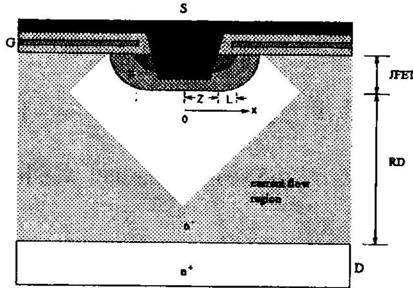

Fig.1. Structure of the vertical DMOST

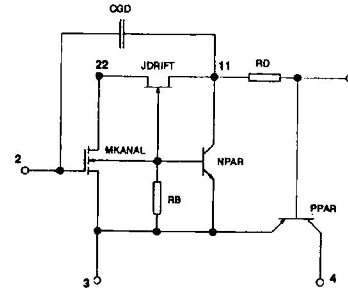

Fig.2. Subcircuit model for the vertical DMOST

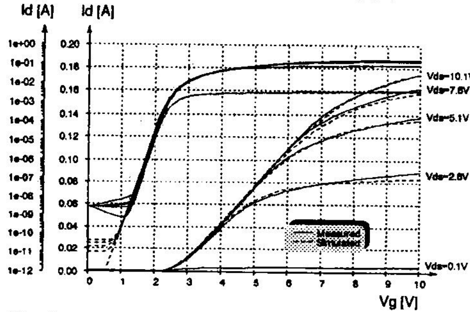

Fig.3. Input Characteristic of 60-cell DMOST

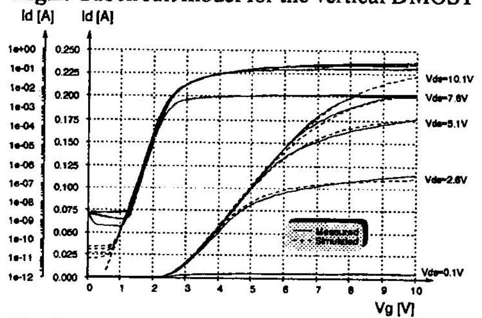

Fig.4. Input Characteristic of 80-cell DMOST

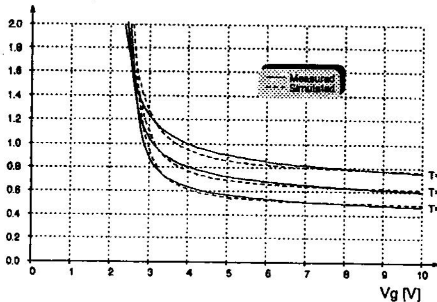

Fig.5. R_{on} for 4000-cell DMOST at $V_{DS} = 0.1V$

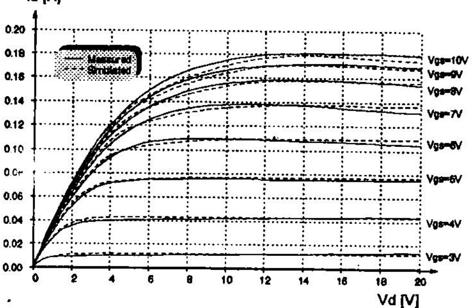

Fig.6. Output Characteristic of 60-cell DMOST

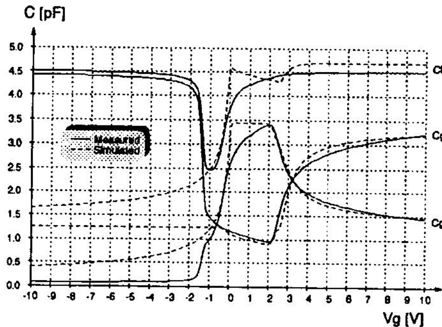

Fig.7. First capacitance model for 60-cell DMOST

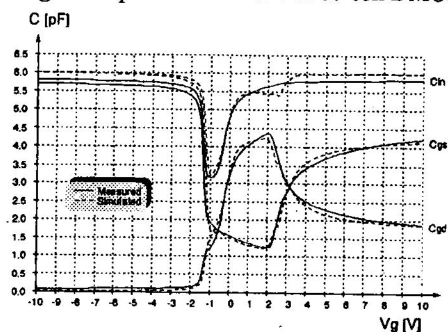

Fig.8. Second capacitance model for 80-cell DMOST