SIMULATION OF GRAFT BASE FORMATION AND EMITTER OUTDIFFUSION IN HIGH-PERFORMANCE BIPOLAR LSIs

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Abstract
Crucial polysilicon-related process steps in high performance bipolar technology are simulated successfully. The forming of a shallow graft base by boron self-aligned outdiffusion from a base-polysilicon film and arsenic outdiffusion from an emitter-polysilicon layer has been studied. Therefore, a two-dimensional simulation model for dopant diffusion in polysilicon has been developed, which includes dopant clustering in polysilicon grain interiors as well as in the grain boundaries. The grain growth model is coupled with the diffusion coefficient of the dopants and the process temperature.

1. Introduction
In recent device fabrication technology polysilicon-related processes have become more important for high performance bipolar LSIs [1], [2]. Due to the low thermal budget and high dose implantation processes, more accurate physical models are required. To predict precise concentration profiles in polysilicon layers various phenomena such as clustering, segregation at material interfaces, generation/recombination mechanisms, and grain growth must be incorporated in the polysilicon diffusion models.

2. Polysilicon Diffusion Model
Within polysilicon material four major transport mechanisms for dopants can be found. The grain boundary network as fast diffusion pathes, the grain boundary motion due to grain growth, the segregation between grain boundaries and grain interior mono-Si, and the grain interior mono-Si diffusion itself. Especially the fast diffusion routes and the grain growth kinetics determines the final distribution of the dopants after annealing. The two-dimensional coupled PDEs for the active dopant concentration in the grain interior (C_{ga}) and the grain boundaries (C_{gb}) are given in Eq.s (1)-(2).

$$\frac{\partial C_{ga}}{\partial t} = \text{div}\left(D_{ga} \cdot \left(\text{grad } C_{ga} + s \cdot \frac{C_{ga}}{U_T} \cdot \text{grad } \psi\right)\right) - G_s, \tag{1}$$

$$\frac{\partial C_{gb}}{\partial t} = \text{div}\left(\gamma \cdot D_{gb} \cdot \left(\text{grad } C_{gb} + \frac{C_{gb}}{r} \cdot \text{grad } r\right)\right) + G_s \tag{2}$$

$$G_s = t \cdot \left(\frac{T_b^{max}}{r} - C_{gb}\right) \cdot C_{ga} - e \cdot \left(C_g^{sol} - C_{ga}\right) \cdot C_{gb} \tag{3}$$

γ denotes a geometric factor taking into account the different average grain size of polysilicon material in lateral and vertical direction. The segregation kinetics (Eq.3) is

considered with generation/recombination terms of the exchange of dopants between grain interiors and grain boundaries by use of trapping t and emission e mechanisms, where a maximum number of free states in the grain boundary T_b^{max} itself is assumed [6]. During low thermal budget processing the average grain size of polysilicon increases due to high dopant concentrations. By high-thermal processing an additional grain growth starts from the initial interfacial oxide layer between mono-Si and polysilicon [3].

3. Grain Growth Model

In our model the grains of polysilicon are assumed to be tiny squares with an initial grain size r_0. During the thermal treatment the grain boundaries will migrate, so grain growth occurs. The calculation of the migration is based on thermodynamic concepts [4],[5] and depends on grain boundary thickness λ, grain boundary energy $\Delta\mu$, diffusion of dopants across the grain boundary D_{ga}, and process temperature T. The lattice dependent grain growth rate is given in Eq.(4) by the product of the net rate of dopant transfer across the grain boundary and the grain boundary thickness.

$$\frac{\partial r(x,y)}{\partial t} = \frac{D_{ga}(C_{ga}(x,y))}{\lambda} \cdot \left[1 - e^{-\frac{\Delta\mu}{K \cdot T}} \right]. \tag{4}$$

Via the diffusion coefficient of the active dopants the grain growth depends on the local dopant concentration. Due to the anisotropic material properties of polysilicon the average grain size becomes non-uniform along the vertical and lateral direction. On the other hand this non-uniform grain size distribution causes an oriented diffusion flux for the grain boundary diffusion. The above given grain growth model seems to be valid for low thermal budget processing, but by high-thermal processing an additional grain growth starts from the poly-Si/mono-Si interface, due to the large amount of generated impurities (vacancies and interstitials) from interface oxidation [3].

4. Simulation Results

Fig.1 shows the device geometry for a graft base formation process. After an isolation process, a base polysilicon film was deposited working as outdiffusion source to form an extrinsic base doping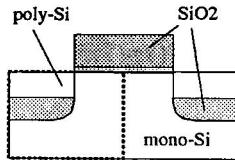. High-concentration boron was implanted with an energy of 40 keV and a dose of $5 \cdot 10^{15} cm^{-2}$ into the polysilicon film at a constant distance from the mono-Si. This distance controls, combined with the following annealing conditions, the final amount of boron dopants in the graft base region. Then the film was etched to produce a planar surface. During annealing at 950°C the boron dopants diffuse into the intrinsic base region and so the graft base is formed.

Figure 1: Device geometry for extrinsic base doping by graft base formation [1].

Fig.2 shows the dopant distribution before performing the base anneal, where Fig.3 gives the boron concentration after 20 min. furnace annealing at 950°C. A graft base depth of $0.2\mu m$ can be measured. After oxide deposition and an open up emitter process, the emitter poly-layer is deposited (Fig.4) which is used as an arsenic diffusion source forming a shallow emitter. Therefore high-concentration arsenic with an energy of 40 keV and a dose of $2 \cdot 10^{15} cm^{-2}$ was implanted into the emitter poly-layer. In our

Boron Concentration cm-3
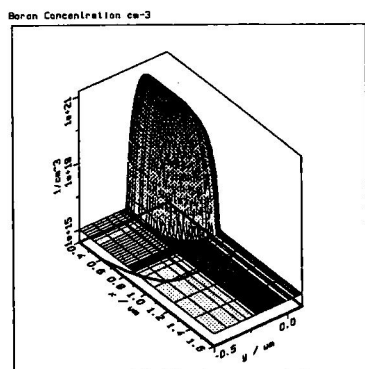
Boron Concentration cm-3

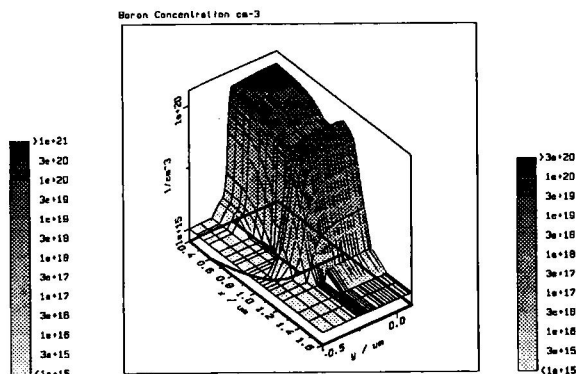Figure 2: Boron concentration in the base poly-layer after 40keV, 5E15 implant

Figure 3: Boron concentration after 20 min. high dose boron diffusion, the graft base is formed

simulations we use perpendicular boundaries between the oxide spacer and the emitter poly-layer so there are less dopants in the corner regions. This leak of dopants nearby the poly/mono-Si interface causes a smaller interface dopant pile-up.

Fig.5 gives the final arsenic concentration after performing an outdiffusion simulation from the emitter poly-layer in substrate for 10 min. furnace annealing at 900°C.

Here the poly-layer is filled with dopants up to the solobility limit in the grain boundaries and the interface pile-up is not significant. By appling a better implantation technique, where the dopants are distributed homogeneously along the interface, a huge and characteristic dopant pile-up can be found (Fig.6).

Arsenic Concentration cm-3
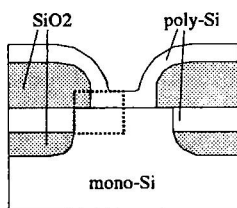
SiO2   poly-Si
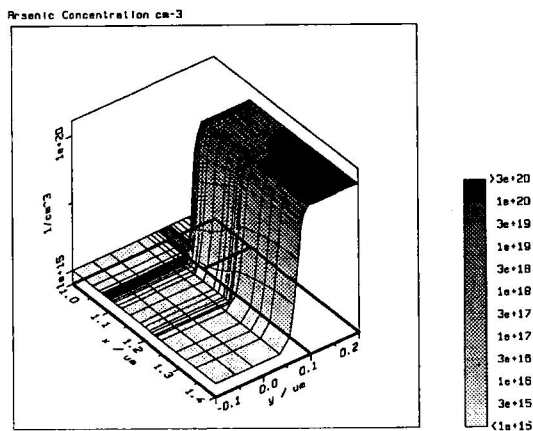
mono-Si

Figure 4: Device geometry after emitter poly-layer deposition [2]

Figure 5: Poly emitter outdiffusion of Arsenic for 900°C 10min. FA. with dopant leak due to previous implantation
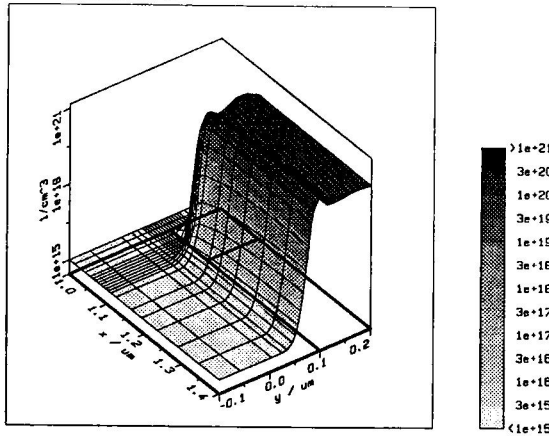
Figure 6: Poly emitter outdiffusion of Arsenic for 900°C 10min. FA. with optimal previous implantation
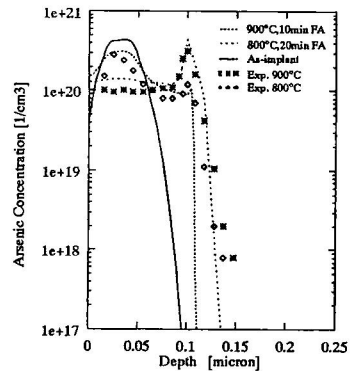

Figure 7: Arsenic profile in the emitter poly-layer, emitter depth W_d=40nm and comparision with experimental data[1].

Fig.7 shows one-dimensional simulation results for outdiffusion simulations at two different thermal budgets under optimal previous implantation conditions. For the 900°C annealing an emitter depth(W_d) of 40nm is computed, which agrees with SIMS measurements [1] at higher concentrations, where at lower concentrations a leak of dopants can be recognized, because of neglection of vacancy and interstitial diffusion in our model.

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