A B-SPLINES REGRESSION TECHNIQUE TO DETERMINE ONE-DIMENSIONAL MOS DOPING PROFILES

N. Khalil, G. Nanz[†], and R. Rios
Digital Semiconductor, ULSI Operations Group,
77 Reed Rd, Hudson, MA 01749, USA
[†]Campusbased Engineering Center Vienna
Favoritenstraße 7, A-1040 Vienna, Austria
and
S. Selberherr
Institute for Microelectronics, TU Vienna
Gußhausstraße 27-29, A-1040 Vienna, Austria

Abstract

The use of B-splines representation as a general non-parametric functional form in the inverse modeling determination of MOS doping profiles from deep depletion capacitance data is described. A self-adaptive algorithm for the spline knots placement is presented. Its use results in a fully automated extraction procedure. The profile of an N-channel MOSFET is shown together with results that illustrate the performance of the proposed algorithm. Finally, a comparison of simulated and experimental I_{ds} current values highlights the accuracy of the extracted profile.

1. Introduction

The analytical extraction of doping profiles from differential capacitance measurements is based on the deep depletion approximation which, for a MOS device, results in the following standard equations:

$$N(x) = \frac{2}{q\varepsilon_{si}} \left[\frac{d}{dV_g} \left(\frac{1}{C_g^2} \right) \right]^{-1} \tag{1}$$

and

$$x = \varepsilon_{si} \left(\frac{1}{C_o} - \frac{1}{C_{ox}} \right) \tag{2}$$

where q is the electron charge, ε_{si} the semiconductor permitivity, C_g and C_{ox} are the gate and oxide capacitance per unit area respectively. The limitations of the above equations and their inability to determine the doping near the interface and for rapidly changing profiles are well documented 1).

In the inverse modeling method, Poisson's equation is solved numerically without the deep depletion approximation. This has been shown to be more accurate than the analytical extraction ^{2,3)}. To circumvent the need to assume an *a priori* functional form of the profile variation, the use of B-splines has been proposed ^{4,5)}. However, the issue of selecting the appropriate number of breakpoints, or knots, and their location was not addressed. In this paper, we present an algorithm for the spline partition selection based on ideas from similar applications ⁶⁾.

2. One-Dimensional Profile B-splines Representation

The one-dimensional doping profile can be formulated as a linear combination of the B-splines basis functions $(B_{i,k,t})$ of order k defined on the so-called knot sequence $t = (t_i), i = 1, n^{-7}$:

$$N(x) = \sum_{i=1}^{n} \alpha_i B_{i,k,t}(x)$$
 (3)

The coefficients α_i can be selected so as to minimize the least squares criterion between the simulated and experimental deep depletion capacitance values. Typically quadratic or cubic splines are used to ensure the smoothness of the profile. However, no algorithmic solution to the more intricate and difficult knot placement problem exists. We resort to a heuristic strategy that is based on prior knowledge of the physical laws involved as explained in Section 4.

3. Extraction Procedure

We use a one-dimensional Poisson's solver that models all the physical effects present in state-of-the-art CMOS technology such as quantum mechanical and polysilicon depletion effects ^{8,9)}. The oxide thickness is first determined using one capacitance measurement in the accumulation region ⁸⁾. Next, the average polysilicon doping concentration is calculated by fitting quasi-static C-V measurements in the inversion regime with simulation. Using deep depletion data taken on a large MOS capacitor, the doping profile is first extracted using (1) and (2). This profile forms the initial guess of the inverse modeling procedure.

The use of equally spaced knots usually does not provide sufficient accuracy. This simple strategy tends to increase the number of degrees of freedom in the profile representation beyond the available information 6). It results in an overdetermined problem and a large variance error of the extracted coefficients. Fig. 1 compares the analytically extracted profile with profiles determined using 10 and 15 equally spaced knots. It is clear that the oscillations between 0.6 μm and 1.3 μm are artifacts of the extraction procedure.

4. B-Splines Knot Placement Algorithm

The MOS profile can be extracted from the SiO_2/Si interface down to the maximum extent of the depletion region (w_{max}) . w_{max} is calculated using (2). Initially 3 knots x_i are placed at 0, $\frac{1}{2}w_{max}$, and w_{max} . After an initial extraction, the fit error is analyzed. Since the capacitance errors are given at a certain gate voltage, (2) is again used to calculate the depletion depth that corresponds to this voltage. The interval with the highest error reduction potential (Φ) is identified. Φ is defined as the integral of absolute errors on the interval between two knots:

$$\Phi = \int_{z_i}^{z_{i+1}} (|C_i^{cal} - C_i^{ezp}|) dx \tag{4}$$

A new knot is inserted in the middle of that interval and the extraction is repeated until the information contained in the measurement data is fully used and the insertion of new points does not provide any significant improvement. In general, the necessary criterion of the equidistribution of the errors in all intervals cannot be achieved, however, it gives important information to choose a proper stopping criterion.

5. Results

The use of the self-adaptive scheme resolves the problems associated with determining the spline partitions. For our example, only six knots were sufficient to reach a good fit. Fig. 2 shows the extracted doping using the proposed algorithm together with the analytical extracted profile. As seen, the failure of the deep depletion approximation near the interface and in rapidly changing profile regions, results in large errors for the analytical profile. The performance of the knot placement strategy is depicted in Fig. 3 which compares the decrease in the residual sum of squares as a function of the number of knots when using the new algorithm to the case of equally spaced knots. Finally, the excellent capacitance fit achieved is shown in Fig. 4.

To validate the accuracy of the extracted profile, a two-dimensional device simulator, MINIMOS 10), was used to calculate the current of a long channel MOSFET (I_{ds}). In this case, the one-dimensional vertical variation of the profile is the main influence in determining I_{ds} . Fig. 5 compares MINIMOS simulations using the extracted profile to experimental current data in the subthreshold and in the linear regions. As seen the fit is excellent for a wide range of gate and bulk bias voltages.

6. Conclusion

We have presented a new technique for one-dimensional MOS dopant profiling using inverse modeling and B-splines representation. The method was applied successfully to data from state-of-the-art CMOS process and validated using two-dimensional device simulation.

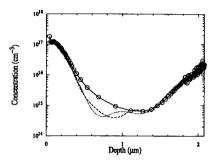


Figure 1: Comparison of Analytically Extracted Profile (solid-symbols) with Profile Extracted using 10 (dashed) and 15 (dotted) equally spaced knots.

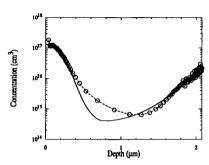


Figure 2: Inverse Modeling (solid) and Analytical (dashed) extracted profiles.

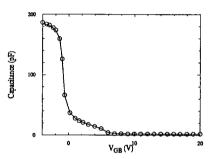
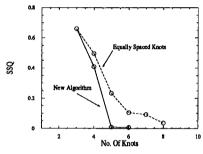


Figure 3: Simulated (solid) and experimental (symbols) deep depletion C-V data of a 39800 µm2 MOS capacitor.



Residuals sum of relative error Figure 4: squares (SSQ) v/s number of knots for the new algorithm (solid) and equally spaced knots (dashed).

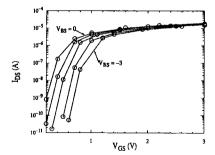


Figure 5: Simulated (line) and experimental (symbols) Ids current of a MOSFET with 70Å oxide, $64\mu m$ width, $64\mu m$ length, and $4.4 \times 10^{19}/cm^3 N_p$.

References

- E.H. Nicollian and J.R. Brews, MOS Physics and Technology, John Wiley & Sons, 1982.
- G.J.L. Ouwerling, Ph.D. Dissertation, 1989, The Delft University of Technology, Netherlands.
- [3] K. Iniewski and C. A. Salama Solid State Electronics, Vol.34, No. 3, pp. 309-314, 1991.
- [4] N. Khalil and J. Faricelli, SISDEP-1993, p. 365-368.
- N. Khalil, et al., *IEEE EDL-16*, No.1, pp. 17-19, 1995.
- A.T. Watson, et al., SPE Reservoir Engineering, p. 953, Aug. 1988.
- C. De Boor, A Practical Guide to Splines, Springer-Verlag, 1978.
- [8] R. Rios and N. Arora, IEDM-1994, pp.613-616.
- [9] P. Habaŝ and J. Faricelli, IEEE ED-39, p. 1496, 1992.
- [10] S. Selberherr et al., IEEE ED-27, (8), 1980.