VLSI PERFORMANCE ANALYSIS METHOD FOR LOW-VOLTAGE CIRCUIT OPERATION

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ABSTRACT

An efficient and accurate method for VLSI performance analysis is presented. It takes measured or simulated IV and capacitance data as input and yields the noise margins and delay parameters directly without any intermediate parameter extraction, avoiding the common errors of compact modeling. The method is applied to the IV/C data of an ultra-low-power CMOS process and the results are then verified by a rigorous device-level simulation of ring oscillators.

INTRODUCTION

Because of the enormous possible power savings and due to reduced thermal and reliability problems future VLSI technologies will increasingly employ low-voltage circuit operation [1]. This, however, implies that the transition region between weak and strong inversion in MOSFETs will dominantly determine VLSI circuit performance [2]. Unfortunately, this is a weak point of virtually all compact MOSFET models, so a new method was developed avoiding these problems.

ANALYSIS METHOD

For the DC analysis a matrix of drain currents $I_D(V_G,V_D)$ for the PMOS and NMOS transistor is computed. Using cubic interpolation in V_D direction and a modified exponential interpolation in V_G direction results in a very accurate DC model. The inverter transfer curve and noise margins are then obtained by solving $I_{Dn}+I_{Dp}=0$ [3]. For the dynamic analysis a ring oscillator is modeled as shown in Fig. 1. All capacitive effects are modeled by a constant load capacitance of $C_L = C_1+4C_M+C_2 = C_{Gn}+C_{GDn}+C_{DGn}+C_{Dn}+C_{Gp}+C_{GDp}+C_{DGp}+C_{Dp}$ where $C_X(V_{GS},V_{DS}) = (C_X(0,0)+C_X(V_{DD},V_{DD}))/2$, assuming a partial compensation of the nonlinearities in the inverter circuit. The inverter delay is then calculated from the delay T and the period t_p as $t_d = (t_p - 2T)/2$. The influence of interconnects can be easily included by adding the appropriate capacitance to C_L. Similarly, the maximum clock frequency and leakage time of dynamic circuits can be determined [2].

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VERIFICATION AGAINST DEVICE-LEVEL SIMULATIONS

The method was tested with an ultra-low-power CMOS process designed for V_{DD} = 200mV [2]. The device data were obtained by process and device simulation using VISTA with its SFC (Simulation Flow Controller) to allow quick process design and evaluation [4]. The analysis yielded inverter noise margins of $NM_H = 28\%$ and $NM_L = 23\%$ and a delay time of t_d = 290ps. Fig. 2 shows the inverter transfer curves and Fig. 3 shows the inverter noise margins and delay time over a range of V_{DD}. To verify these results complete ring oscillators with 5 and 9 stages were rigorously simulated on the two-dimensional device level. The inverter delay is determined from the ring oscillator period t_p as $t_d = t_p/2n_{stage}$ as t_d = 230ps. Despite of the simple, i.e., quasi-static and linear dynamic model the delay time error is only 26%. This can be partially attributed to the fact that only small voltages (reducing the non-linearity of the capacitances) and small currents (reducing the non-quasi-stationary error) are involved.

CONCLUSION

The analysis method presented here takes measured or simulated IV/C data and extracts the most important performance parameters, i.e., noise-margins and inverter delay directly without any model parameter fitting. It is noteworthy that there is no necessity to know any compact model of the devices or to *define* model parameters such as $\beta_{n,p}$ or $V_{Tn,p}$ which become very questionable at low supply voltages. Avoiding these sources of error makes our method a simple, yet powerful tool for performance analysis, especially for low-voltage/low-power circuit operation.

ACKNOWLEDGEMENTS

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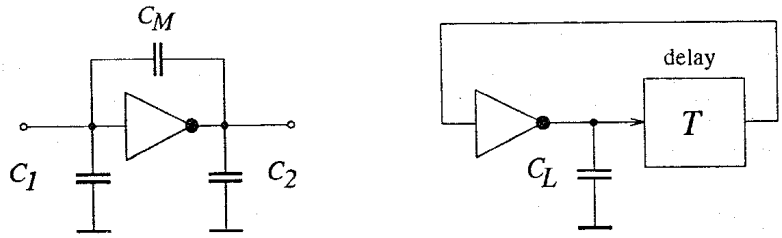

Figure 1: Dynamic inverter model and simplified ring oscillator model

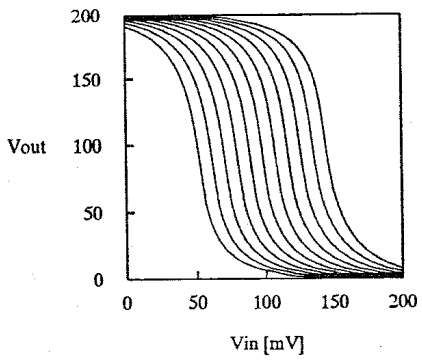

Figure 2: Inverter transfer characteristics for $W_n/W_p = 0.1...10$ (ULP process at $V_{DD} = 200$mV)

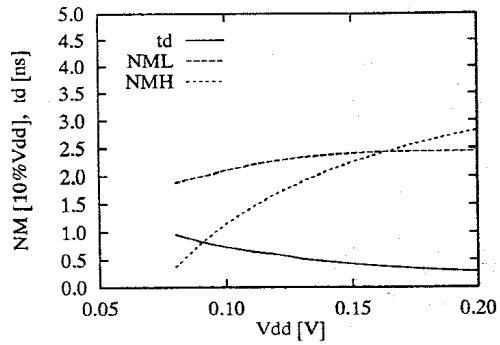

Figure 3: Noise margins and delay time vs. V_{DD}

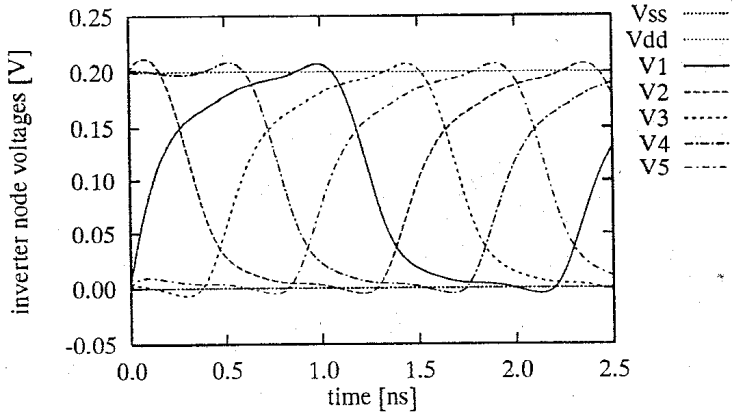

Figure 4: Inverter output voltages of a 5-stage ring oscillator at $V_{DD} = 200$mV (device-level simulation)