

# The Extraction of Two-Dimensional MOS Transistor Doping via Inverse Modeling

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**Abstract**—We present a novel method for the determination of the two-dimensional (2D) doping profile of a MOSFET using inverse modeling. In our method, the logarithms of the donors and acceptors concentrations are each represented by a tensor product spline (TPS). The TPS coefficients are extracted by nonlinear, least squares optimization from source/drain (S/D) diode and gate capacitance data. After validating the method by applying it to simulated capacitance data, we present the results of using the new technique to extract the 2D profile of a 0.42  $\mu\text{m}$  gate length CMOS technology N-channel device.

## I. INTRODUCTION

DIRECT experimental measurements of 2D doping profiles require difficult sample preparation procedures such as sophisticated data reduction or complicated angle lap and stain techniques [1]–[3]. They have met with limited success when applied on shallow junction devices of modern technologies. Their shortcomings have restricted their usage in spite of the importance of determining 2D doping profiles for characterization and accurate device simulation. Inverse modeling [4] provides an alternative methodology that is not hindered by experimental difficulties. In this letter, we describe a new inverse modeling based methodology [5], [6] for MOSFET profiling. Our method uses measurements easily performed during process characterization such as gate overlap and S/D diode capacitances. We present two applications of our methodology. In the first example, we use simulated capacitance data generated from a known profile and compare the extracted and the original profiles. In the second example, we show the results of determining the 2D doping profile of a 0.42  $\mu\text{m}$  gate length CMOS technology N-channel device. We also assess the resolution of our method for different regions of the device and discuss its limitations.

## II. PROFILE REPRESENTATION

We parameterize 2D doping profiles by representing the logarithm of the donors and acceptors concentrations as TPS [7]. TPS is a generalization to multidimensional space of the one-dimensional spline representation. Each TPS has its own sequence of breakpoints, or knots, to accommodate the different field variation for each impurity type. This formulation was chosen because it is more general than other analytical forms: It does not assume *a priori* knowledge of the profile functional variation. Using TPS with fixed knots we can write

the net doping as:

$$N(x, y) = \Theta(\delta_{ij}, \alpha_{ij}) \quad (1)$$

where  $\alpha_{ij}$  and  $\delta_{ij}$  are TPS coefficients for the acceptors and donors respectively. We typically use quadratic splines with five knots in each direction. The positioning of the knots is important and should be guided by process information such as junction depth, gate length, and spacer width.

## III. METHODOLOGY

The method is based on the numerical solution of Poisson equation in the silicon and polysilicon gate regions that take into account polysilicon depletion effects [8]. We calculate the different capacitances by differentiating the appropriate charges from SEDAN III [9] for 1D, and MINIMOS [10] for 2D simulations. To avoid numerical problems, we carefully refine the grid where the space charge varies rapidly, and we fix the grid while applying small voltage steps to calculate the charge variation. We describe our methodology using an N-channel MOSFET. The same procedure can be applied to P-channel devices.

- First, we determine the oxide thickness ( $t_{ox}$ ) from high frequency C-V measurements.
- We then fit the simulated gate-to-channel capacitances ( $C_{gc}$ ) to measured values with the device biased in inversion and extract the gate length ( $L$ ) and the doping of the polysilicon gate concentration ( $N_p$ ).
- Using deep depletion capacitance data taken on a large MOS capacitor, the coefficients of the vertical channel profile spline representation and the gate work function are then extracted.
- We rely on SIMS or 1D process simulation to determine the donors profile in the S/D region and generate its spline coefficients by curve fitting. The acceptors coefficients are then determined from the reverse junction diode area capacitance data.
- A 2D starting profile is formed by rotating the S/D donors 1D profile and spreading the channel acceptors profile laterally except in the S/D region where the acceptors profile from the previous step is used. We adjust the rotation factor to yield the measured electrical effective channel length. The resultant profile is the initial guess for the 2D extraction.
- Finally, we perform an optimization to extract the remaining TPS coefficients of the doping for both acceptors and donors. We use gate and diode capacitance data taken on a fingered polysilicon structure over active region. The

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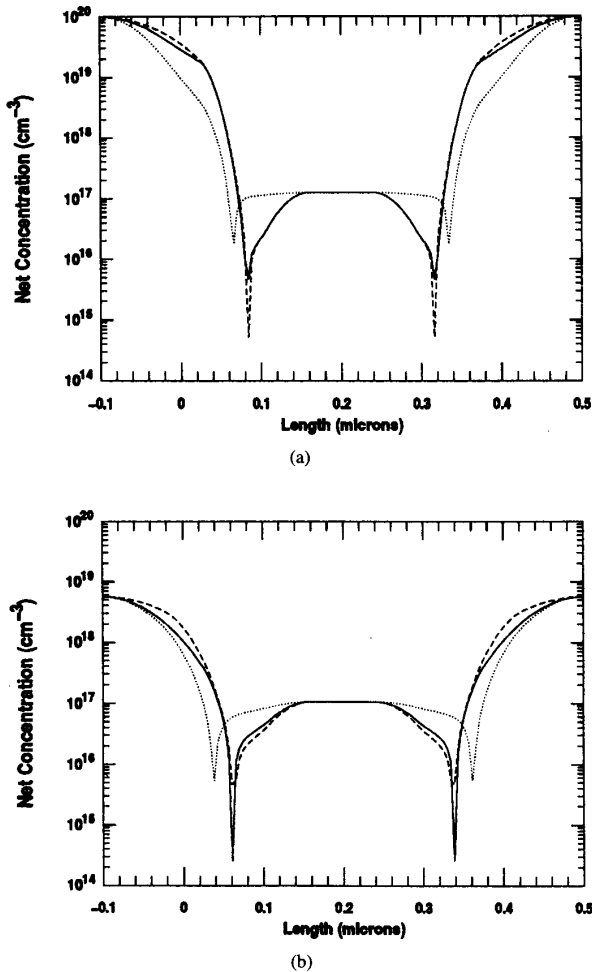


Fig. 1. Comparison of original (dashed), initial guess (dotted), and extracted (solid) net doping at the  $\text{SiO}_2/\text{Si}$  interface (a) and at  $0.1 \mu\text{m}$  depth into silicon (b) for the simulation experiment.

diode is surrounded by a gate on all sides to eliminate any capacitance coupling to the isolation area. We take our measurements under a variety of bias conditions that “probe” various portions of the doping profile by depleting or accumulating the carriers in that region. We perform a coupled solution of the nonlinear least squares problem. At each iteration, we update the TPS coefficients of the acceptors and donors separately by taking one step in the Levenberg-Marquardt algorithm while keeping the coefficients of the other impurity type fixed. We only extract coefficients at knots when they are of the same type as the net doping at that location. We note the importance of a good initial 2D profile to avoid the trapping of the solution in a local minimum.

#### IV. RESULTS

In the absence of independent means of verification, our extraction methodology is validated by applying it on capacitance data generated using simulation with a known TPS profile. The extracted profile is then compared to the original one.

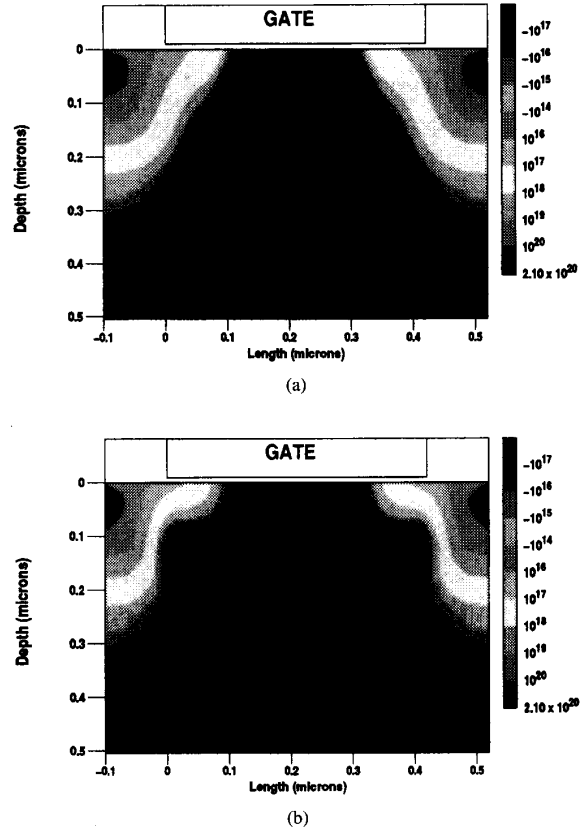


Fig. 2. Starting (a) and extracted (b) 2D net doping for NMOS device with LATID implant,  $L = 0.42 \mu\text{m}$ ,  $t_{ox} = 95 \text{ \AA}$ , and  $N_p = 3.5 \times 10^{19} \text{ cm}^{-3}$ .

We used a TPS profile with known knot locations to eliminate errors associated with the TPS approximation. Fig. 1 shows the original, starting, and extracted lateral net doping profiles at the  $\text{SiO}_2/\text{Si}$  interface (a), and at  $0.1 \mu\text{m}$  depth into silicon (b). As seen, the agreement is very good in both cases. However, the fit accuracy decreases slightly in the high concentration S/D region (Fig. 1(a)) and as we move into the silicon (Fig. 1(b)).

In our second example, we used data from a CMOS process with a physical polysilicon gate length of  $0.42 \mu\text{m}$  and an effective channel length of  $0.28 \mu\text{m}$ . The oxide thickness is  $9.5 \text{ nm}$  as measured in accumulation. The NMOS device has a phosphorous large-angle-tilt implanted drain [11], and received a heavy arsenic implant. The starting and extracted 2D profiles are shown in Fig. 2. In Fig. 3(a) we plot the experimental gate to S/D capacitance, together with simulated results calculated using the starting and the extracted profiles. The fit improvement is apparent. Fig. 3(b) shows the corresponding inner periphery diode data which also fits very well.

#### V. DISCUSSION

Besides the device structure and geometry, the net doping is the only other input for solving Poisson equation. By matching the experimental capacitance measurements, the extracted profile is an accurate representation of the net dopant distribution in the device. The following points illustrate some characteristics of the method and associated uncertainties:

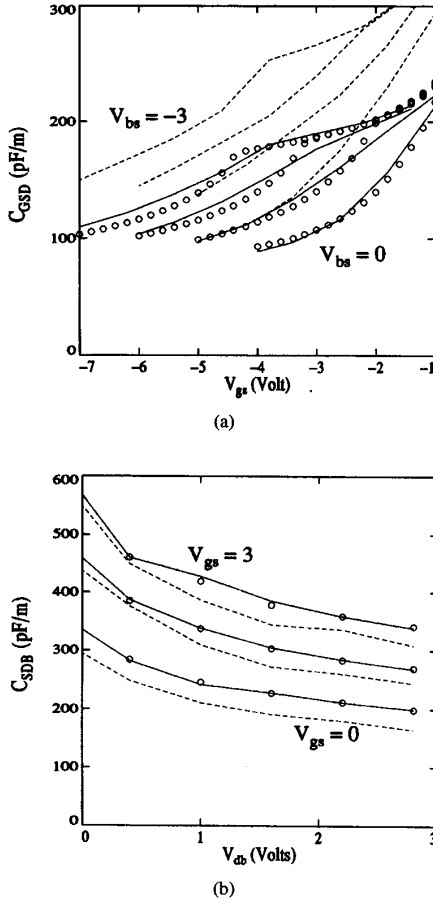


Fig. 3. Comparison of experimental (symbols), simulation with starting profile (dashed), and simulation with extracted profile (solid) of gate to source/drain capacitances  $C_{GSD}$  vs.  $V_{gs}$  at varying  $V_{bs}$  (a) and inner periphery source/drain diode capacitances  $C_{SDB}$  vs.  $V_{ds}$  at varying  $V_{gs}$  (b).

- The method capability is limited to extracting the electrically active impurity doping concentration, not the chemical concentration of atoms.
- The net doping term in Poisson equation results in a correlation between the donors and acceptors coefficients. We address this issue by using the coupled iterative extraction scheme as described in the previous section.
- Uncertainties in device geometrical structure such as nonplanar surfaces have a direct effect on the extracted profile. These can be resolved by independent determination of the structural information using TEM imaging.
- As seen in Fig. 1, the resolution is slightly degraded for the high concentration S/D and the inner diode regions. This is caused by the inability to uncover the dopant atoms in those regions due to the limited capability of the gate to deplete the region of carriers under accumulation bias without oxide breakdown in the first case, and to the screening effects of the intermediate dopant layers in the second. In other words, we cannot “probe” those portions of the doping profile. We note however that the junction delineation is very good.

- Since no analytical approximations are involved in the solution of Poisson equation, the method has a better resolution than analytically based profile extraction methods [12].
- The dopant concentration values near the  $\text{SiO}_2/\text{Si}$  interface are correlated to the values of the gate work function and the oxide charge density along the channel used in solving Poisson’s equation. We presently use the work function and charge density values determined during the deep depletion extraction step.
- The amount of computation needed to extract the 2D profile is approximately 36 hours of CPU time on a desktop Alpha AXP workstation model 3000-400. We have already devised software strategies to reduce this time significantly.

VI. CONCLUSION

We have presented a new method for MOSFET 2D profile determination. The method is nondestructive and provides important information for device design and characterization, especially for modeling and predicting device capacitances. Moreover, it provides a means for calibrating 2D process simulation models.

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REFERENCES

- [1] S. H. Goodwin-Johansson, R. Subrahmanyam, C. E. Floyd and H. Z. Massoud, “Two-dimensional impurity profiling with emission computed tomography techniques,” *IEEE Trans. Computer Aided Design*, vol. 8, no. 4, 1989.
- [2] R. Subrahmanyam, H. Z. Massoud and R. B. Fair, “Experimental characterization of two-dimensional dopant profiles in silicon using chemical staining,” *Appl. Phys. Lett.*, vol. 52, no. 25, 1988.
- [3] S. Kordic, E. Van Leonen, D. Dijkkamp, A. Hoeven and H. Moraal, “Scanning tunneling microscopy on cleaved silicon PN junctions,” *IEDM Technical Digest*, 1989, pp. 277-280.
- [4] G.J.L. Ouwering, “Nondestructive one- and two-dimensional doping profiling by inverse methods,” Ph.D. Dissertation, 1989, The Delft University of Technology, Netherlands.
- [5] N. Khalil and J. Faricelli, “MOSFET two-dimensional doping profile determination,” in *SISDEP-93*, p. 365, 1993.
- [6] N. Khalil, J. Faricelli, D. Bell and Siegfried Selberherr, “A novel method for extracting the two-dimensional doping profile of a sub-half micron MOSFET,” *Symp. VLSI Technology 1994*, Digest of Technical Papers, pp. 131-132.
- [7] Carl De Boor, *A Practical Guide to Splines*. New York: Springer-Verlag, 1978.
- [8] P. Habaš and J. Faricelli, “Investigation of the physical modeling of the gate-depletion effect,” *IEEE Trans. Electron Dev.*, vol. 39, p. 1496, 1992.
- [9] *SEDAN III - A Generalized Electronic Material Device Analysis Program*, Stanford University, July 1985.
- [10] S. Selberherr, A. Schütz and H. W. Pötzl, “MINIMOS — A two-dimensional MOS transistor analyser,” *IEEE Trans. Electron Dev.*, vol. 27, no. 8, Aug. 1980.
- [11] T. Hori, “1/4- $\mu\text{m}$  LATID (Large-Tilt-Angle Implanted Drain) technology for 3.3-V operation,” in *IEDM-1989 Technical Digest*, pp. 777-780.
- [12] W. C. Johnson and P. T. Panousis, “The influence of Debye length on the C-V measurement of doping profiles,” *IEEE Trans. Electron Dev.*, vol. 18, no. 10, pp. 965-973, Oct. 1971.