A CHARGE BASED MOSFET MODEL FOR LOW-VOLTAGE MIXED-SIGNAL APPLICATIONS

G. Schrom, A. Stach and S. Selberherr

Institute for Microelectronics, TU Vienna
Gusshausstrasse 27-29, A-1040 Vienna, Austria
E-mail schrom@iue.tuwien.ac.at

Abstract

Recent developments towards lower voltages [1, 2, 3, 4] pose increasingly stringent demands on compact device model accuracy. We present a new approach to dynamic MOSFET modeling which is especially suited for the simulation of low-voltage mixed analog digital circuits. The model is based on terminal charges and conductive currents which are determined from transient current/voltage data. These data sets can be easily obtained through measurement or simulation of the devices. Using a physically motivated interpolation method the model supplies the accurate current/charge data and their derivatives for given terminal voltages.

1. Model Function and Simulation Environment

The model function is based on the interpolation of the terminal currents and charges of the device. The interpolation also supplies the derivatives, i.e., the conductance and capacitance matrices of the device. These data are directly interfaced to a new circuit simulator, MINISIM [5], which uses charge conservative capacitance modeling. The interpolation is based on piecewise polynomial and/or exponential splines to account for the physical nature of the quantities, especially the exponential dependence of the currents. This approach precludes common problems like discrepancies between the AC-model conductance parameters and the derivatives of the DC-model currents.

2. Data Acquisition

The input data to the model can be obtained either by measurements or by process and device simulations. In this work we used VISTA with MINIMOS [6] to obtain the device data by simulation. All conductive currents can be obtained directly from DC measurements. The charge data are computed

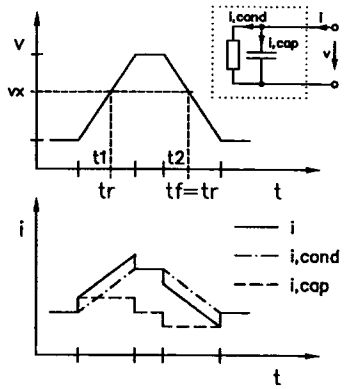

Figure 1: Quasi static black-box model of a two-pole

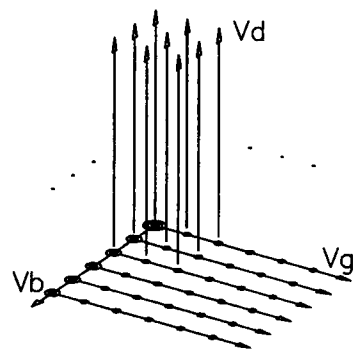

Figure 2: Transient MOSFET simulations / measurements

from transient simulations as shown in Fig. 1 for the case of a two-pole: the device is modeled as a quasi static black box which is equivalent to a nonlinear conductance parallel to a nonlinear capacitance $C(v) = dq/dv$. Applying a symmetrical trapezoidal voltage $v(t)$ to the device will result in a current $i(t)$ which can be separated into a conductive and a capacitive component,

$$\begin{aligned} i_{cond}(v) &= \tfrac{1}{2}\left[i(t_1(v)) + i(t_1(v))\right], \\ i_{cap}(v) &= \tfrac{1}{2}\left[i(t_1(v)) - i(t_1(v))\right], \end{aligned} \tag{1}$$

which is related to the charge by $i_{cap}(v) = dq/dt = (dq/dv) \cdot (dv/dt)$. Thus, the charge can be determined as

$$q(v) = q_0 + \int_v^{v_0} i_{cap}(u)du. \tag{2}$$

The charge offset q_0 can be determined from $q(0) = 0$. In the case of the MOSFET we have a three-pole (assuming the source always grounded), one of the other terminals is ramped, and the currents at all terminals (including the ramped) are measured and subsequently converted to i/q-data. To obtain a complete field of charge data, including the charge offset, a series of transient measurements/simulations is required as shown in Fig. 2. The simulations in 'V_{ds}-direction' yield the main data set which is used for i/q extraction. The simulations in 'V_{bs}-direction' and 'V_{gs}-direction' are required for the charge offset computation. The steepness of the ramp determines the accuracy of the charge data and the influence of non-stationary effects accordingly. Both can be verified with single transient measurements, using the i/q-extraction software. Fig. 3 shows a comparison with gate capacitance data obtained from gate charge simulations using MINIMOS.

3. Applications

Example applications are shown in Figs. 4–7. Fig. 5 shows the simulated switching transients of an RS flip-flop shown in Fig. 4 built in a 0.5V ultra-low-power technology [4]. The same technology can be used to build OPAMPs, operating at even lower supply voltages: Fig. 7 shows the simulated large-signal step response of the two-stage OPAMP shown in Fig. 6, operating as a unity-gain follower at $V_{DD} = 0.4$V with two different loads. The OPAMP is biased for medium speed, consuming a total of 1.44μW.

4. Conclusions

Our new low-voltage MOSFET modeling approach, together with the supporting software, enables the accurate simulation of modern low-voltage mixed analog digital circuits directly from measured or simulated device data without parameter fitting.

Acknowledgments. Our work is significantly supported by Austria Mikro Systeme AG, Unterpremstätten, Austria; Christian Doppler Gesellschaft, Vienna, Austria; and Siemens Corporation at Munich, Germany.

References

[1] J.B. Burr. *Stanford Ultra Low Power CMOS.* In *Symposium Record, Hot Chips V*, pp. 7.4.1–7.4.12, 1993.

[2] D. Liu and Ch. Svensson. *Trading Speed for Low Power by Choice of Supply and Threshold Voltages.* IEEE J.Solid-State Circuits, vol. 28, no. 1, pp. 10–17, 1993.

[3] E.A. Vittoz. *Design of Low-Voltage Low-Power IC's.* In J. Borel, P. Gentil, J.P. Noblanc, A. Nouailhat, and M. Verdone, editors, *23rd European Solid State Device Research Conference - ESSDERC'93*, pp. 927–934, Gif-sur-Yvette Cedex, France, 1993. Edition Frontieres.

[4] G. Schrom, D. Liu, Ch. Pichler, Ch. Svensson, and S. Selberherr. *Analysis of Ultra-Low-Power CMOS with Process and Device Simulation.* In C. Hill and P. Ashburn, editors, *24th European Solid State Device Research Conference - ESSDERC'94*, pp. 679–682, Gif-sur-Yvette Cedex, France, 1994. Editions Frontieres.

[5] A. Stach. *Simulation von MOSFET-Schaltungen.* Diplomarbeit, Technische Universität Wien, 1995.

[6] Ch. Pichler and S. Selberherr. *Process Flow Representation within the VISTA Framework.* In S. Selberherr, H. Stippel, and E. Strasser, editors, *Simulation of Semiconductor Devices and Processes*, vol. 5, pp. 25–28. Springer, 1993.

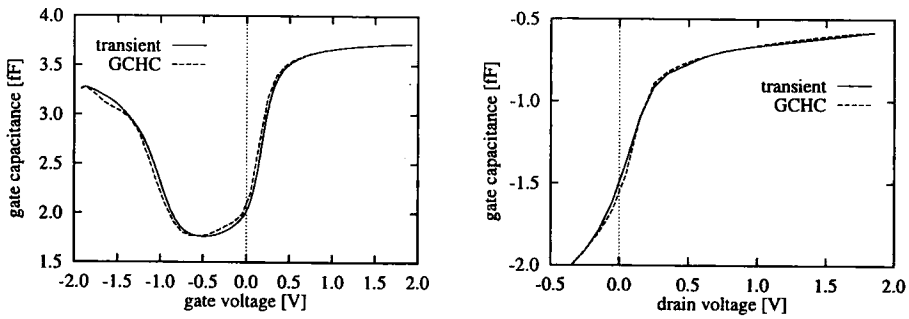

Figure 3: Gate capacitance of an ULP n-channel MOSFET (V_{bs} = 0V). - - -: computed through accurate gate charge integration using MINIMOS's 'GCHC' option. ——: transient method (t_r = 3ns).

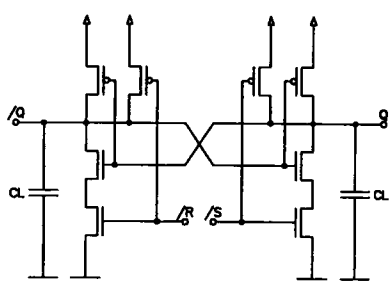

Figure 4: ULP RS flip-flop

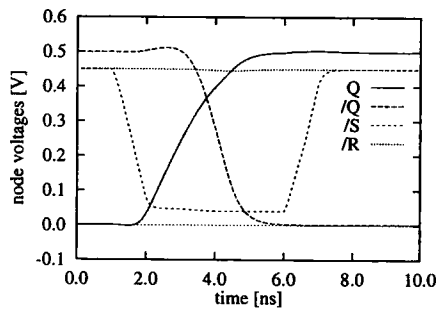

Figure 5: RS flip-flop switching transients (V_{DD} = 0.5V)

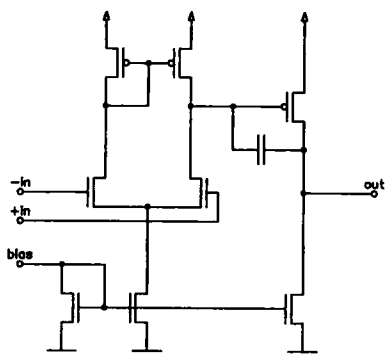

Figure 6: ULP OPAMP

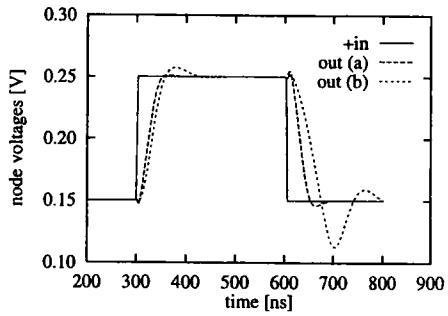

Figure 7: OPAMP large-signal step response at V_{DD} = 0.4V with (a) C_L = 0pF and (b) C_L = 0.5pF