Ultra-Low-Power CMOS Technologies

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Abstract

The fast growing portable-electronics market as well as thermal dissipation, reliability, and scalability issues have launched a massive trend towards low-power and low-voltage technologies. This has lead to a new, reduced standard digital CMOS supply voltage of 3.3V reducing the power consumption by 70%. However, the power consumption can still be cut down substantially by reducing the supply and threshold voltages much further without compromising systems performance. A loss in device speed can be compensated on the systems level by appropriate parallel architectures. Based on this concept of *ultra-low-power CMOS technologies* we explore the lower limits of CMOS supply voltage and switching energy for a variety of circuit classes analytically and numerically. Ultra-low-power (ULP) process and device design, device modeling, performance evaluation, and the specific problems associated with ULP mixed-analog-digital technologies are discussed.

1 Introduction

During the past two decades CMOS has emerged as the main-stream VLSI technology, and downscaling has greatly increased the systems performance, doubling the raw computing power every two years. Industry has long followed a strategy of constant-voltage scaling mainly to sustain the traditional standard supply voltage of 5V and to increase the performance without changing circuit design styles and systems architectures too much. However, as the minimum feature sizes entered the sub-micron regime, not only have reliability and process complexity become a major concern, but, above all, power consumption has turned out to be the key factor in modern high-performance technologies. The increased speed and packing density, i.e., performance per chip area, has been accompanied by an increase of heat generation to a point where the total chip performance is limited by the thermal dissipation capability of the mounted IC package. At the same time, the booming market of portable electronics, where battery life time is a major issue, called for new high-performance low-power technologies [1, 2, 3, 4, 5, 6].

In a typical CMOS technology the total power consumption is dominated by the dynamic power consumption, which is a square function of the supply voltage V_{DD} [7]

$$P = N f C V_{DD}^2, \tag{1}$$

where N is the number of switching gates, f is the clock frequency, and C is the average capacitance per gate. Nf can be taken as a performance measure. The circuit speed, on the

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other hand, (and thereby the maximum clock frequency) increases only linearly with the supply voltage. For sub-micron devices operating at higher voltages this increase is even less because of velocity saturation.

By decreasing the supply voltage and adapting the threshold voltages, a significant reduction of the power consumption can be achieved at the expense of an increase in gate delay. This can be compensated to a certain extent by employing parallelism in the systems design so that, for the same overall performance, the total power consumption is drastically reduced compared to conventional CMOS technologies [3, 8, 9, 10]. The feasibility of this concept of *ultra-low-power CMOS* has been shown also by numerical process and device simulation [11, 12], and by experiments [13, 14, 15]. Mixed-analog-digital systems need special attention due to the different requirements of the analog part [4, 16, 17]. Minimum signal-to-noise ratio and distortion force a higher supply voltage. Yet, there is a large potential in ULP mixed-analog-digital CMOS [18].

2 Analytical Lower Bounds

Early work in this field was based on a minimum-inverter-gain criterion, and a minimum supply voltage of 200mV was found for inverters operating in weak inversion [15]. To determine an absolute lower bound of the supply voltage we assume MOSFETs operating completely in the weak inversion mode. The drain current is then given by [16]

$$I_D = I_0 e^{\frac{V_{GS}}{nU_T}} \left(1 - e^{-\frac{V_{DS}}{U_T}}\right). \tag{2}$$

I_0 is determined by the technology and the channel width-to-length ratio W/L. For the following, we assume also an ideal gate swing of $S = \ln(10)U_T$, thus, $n = 1$. Setting $I_{Dn} + I_{Dp} = 0$ with $I_{0n} = I_{0p}$ yields an implicit equation for the transfer curve $V_{out}(V_{in})$ of a symmetric inverter [19]

$$\frac{\sinh\left(\frac{V_{in}-V_{out}}{U_T}\right)}{\sinh\left(\frac{V_{in}-V_{DD}/2}{U_T}\right)} = e^{\frac{V_{DD}/2}{U_T}} \tag{3}$$

and the critical points where the voltage gain $A = dV_{out}/dV_{in} = -1$ are determined by [7]

$$\frac{2\cosh\left(\frac{V_{in,c}-V_{out,c}}{U_T}\right)}{\cosh\left(\frac{V_{in,c}-V_{DD}/2}{U_T}\right)} = e^{\frac{V_{DD}/2}{U_T}}, \tag{4}$$

from which the noise margins $NM_H = NM_L = NM$ are computed as

$$NM = \frac{V_{DD} - V_{out,c} - V_{in,c}}{V_{DD}} \quad [\%V_{DD}]. \tag{5}$$

The maximum voltage gain which occurs at $V_{in} = V_{out} = V_{DD}/2$ (cf. (12)) is given by

$$-A_{max} = e^{\frac{V_{DD}/2}{U_T}} - 1. \tag{6}$$

Solving the equations (3) and (4) numerically, together with (2) and (6) yields noise margins and maximum gain as a function of the supply voltage.

For the design of digital circuits we have to impose certain constraints, i.e., to specify minimum values for NM and A_{max} at a nominal and maximum temperature and to estimate the impact of an effective unsymmetry $F_U = W_n/W_p$ as a consequence of minimum-transistor-size design.

This is accounted for by a shift of the input voltage $\Delta V_{in} = -U_T \ln(F_U)/2$. Minimum supply voltages for various constraints are compiled in Table 1. For static logic with a fan-in of 3 the minimum V_{DD} is 83mV at 300K or 3.22 times the thermal voltage. Note that these numbers are absolute lower bounds which cannot likely be achieved with any CMOS process technology. Achievable values for V_{DDmin} may be estimated by scaling the numbers from Table 1 by a factor of $n = S/(U_T \ln(10))$ where S is an achievable average gate swing. Although this is not consistent with (3) and (4), it can be used as a worst-case estimate for sub-threshold operation.

Table 1: Ideal-case minimum supply voltage V_{DD} for given of circuit design constraints

constraint		V_{DDmin} (T=300K)	V_{DDmin} $[U_T]$
$A_{max} > 1$	(ring osc.)	36mV	1.40
$NM > 10\%$	(inverter)	55mV	2.13
$A_{max} > 4$	(std. design)	83mV	3.22
$F_U > 9$	(fan-in = 3)	83mV	3.22
$I_{on}/I_{off} > 10^4$	(dyn. logic)	238mV	9.22

To determine a lower bound for the switching energy we regard only the intrinsic channel charge of a turned-on transistor (still operating in weak inversion)

$$Q_{on} = \frac{L^2 I_{on}}{\mu U_T}, \tag{7}$$

where L is the effective channel length and μ is the effective carrier mobility, and the turn-on current I_{on} for a given supply voltage is adjusted by the channel doping. If we now consider an inverter chain with each output node connected to the two gates of the following stage, and we neglect all other parasitics, then the charge of this node is altered by $4Q_{on}$ during one clock period, so that the switching energy is given by

$$E_s = 4\frac{Q_{on} V_{DD}}{2} = 2\frac{L^2 I_{on} V_{DD}}{\mu U_T}. \tag{8}$$

This means that the mere device physics does not limit the switching energy, because I_{on} can be chosen almost arbitrarily (disregarding design rules and tunneling effects). However, if we require a node to be charged with at least, say, 10 electrons then (taking V_{DDmin} for $A_{max} > 4$ from Table 1) the switching energy is at least 0.13aJ. Another limit comes from the error rate in digital systems subject to thermal noise [10]

$$R_E = \frac{M}{t_g} e^{-\frac{E_s}{kT}}, \tag{9}$$

where M is the number of gates and t_g is the gate delay, which is larger than the inverter delay

$$t_d > 2\frac{Q_{on}}{I_{on}} = 2\frac{L^2}{\mu U_T}. \tag{10}$$

If we assume, e.g., a deep sub-micron technology with L = 50nm and $\mu \approx 500\text{cm}^2/\text{Vs}$, and a system with 10^7 gates requiring less than one error per year, then we get $t_d >$ 4ps and $E_s >$ 0.25aJ.

Of course, these values cannot be reached because of the parasitics, most important the gate-drain overlap, junction, and interconnect capacitances, that were not accounted for. When they are included the circuit speed becomes a function of I_{on}, making higher currents necessary to keep up the performance and they also add to the switching energy by $CV_{DD}{}^2$. Because the parasitics are largely technology dependent a simple general analysis is not possible. However, what can be seen from (8) is that the power efficiency scales as $1/L^2$, i.e., the benefit of ULP CMOS increases with downscaling.

3 Ultra-Low-Power Process Technology

As a consequence of the low voltages, ultra-low-power processes differ from conventional CMOS processes in several points: Because of the low V_{DD}, the hot-carrier problem virtually does not exist, and therefore an LDD (lightly doped drain) process is not necessary. Also, no GIDL (gate induced drain leakage), DIBL (drain induced barrier lowering) or latch-up can occur. Furthermore, because of the lower electric field mobility degradation and velocity saturation are greatly reduced. As a result, ULP CMOS processes are much better scalable compared to conventional processes.

The processes under consideration are recessed-well dual-gate processes with a very thin gate oxide (below 6nm) to achieve a good subthreshold behavior and to obtain controllably low threshold voltages. The source/drain doping is formed by single shallow implants and a conventional furnace anneal. The G/S and G/D overlap capacitances are controlled with a spacer formed prior to the S/D implants.

As for very low V_{DD} the devices must operate in the weak inversion regime, the difference of the carrier mobilities μ_n, μ_p can be roughly compensated by adjusting the threshold voltages to achieve symmetric inverter transfer characteristics. This compensation does not work, however, in the transient case because the speed is mainly determined by the strong-inversion part of the input characteristics. The sub-threshold behavior is crucial because it determines the achievable ratio of I_{on}/I_{off}, which is limited by $\exp(V_{DD}/nU_T)$ and decreases as $V_{Tn,p}$ are made smaller. Therefore, "zero-V_T" transistors are not desirable at a very low V_{DD} of a few 100mV. On the other hand, if $V_{Tn,p}$ are too high the speed becomes unacceptably low. As a rule of thumb [13], to maximize the performance the ratio I_{on}/I_{off} should be kept at a minimum value by adjusting $V_{Tn,p}$ as V_{DD} is increased. This will also result in increased leakage currents but that is no problem as long as the total power consumption is kept at a minimum. In other words: leakage is a systems issue.

A major challenge is to achieve controllably low threshold voltages. Although the adjustment of $V_{Tn,p}$ with a bulk bias seems very attractive, this method is not practical (using a traditional layout) because of the significant overhead due to the additional lines for bulk biasing. There are, however, alternative biasing and layout methods to overcome this problem [14].

Another problem can arise from the very thin gate insulator. Although devices with ultra-thin oxides have been successfully fabricated [20] thin oxides are susceptible to boron penetration causing a threshold shift. On the other hand, there are several options for the gate insulator. Nitrides or oxinitrides may prove good alternatives to conventional (pure SiO_2) gate oxides [21, 22]. For "higher" supply voltages the demands on the subthreshold slope and hence on the oxide thickness can be relieved. In the future, fully depleted SOI may be the better choice, as it offers intrinsically good subthreshold behavior and smaller parasitics [23].

4 Numerical Performance Analysis

To determine feasible lower values of the supply voltage, a set of tuned CMOS processes was numerically analyzed by means of process and device simulation. The resulting device data were used for performance analysis on the circuit level [11, 12]. Both process and device simulation were done using the VISTA Technology CAD framework to allow for quick process design and evaluation [24, 25, 26]. For the electrical characterization of the devices MINIMOS [27, 28] was used to calculate a matrix of drain currents $I_D(V_G, V_D)$ over a range of V_G and V_D for the p-channel and n-channel transistors. Based on these data, a fast and accurate table-driven DC analysis of simple gates and inverters is possible [12]. The dynamic behavior was estimated from capacitance data obtained by AC analysis with MINIMOS.

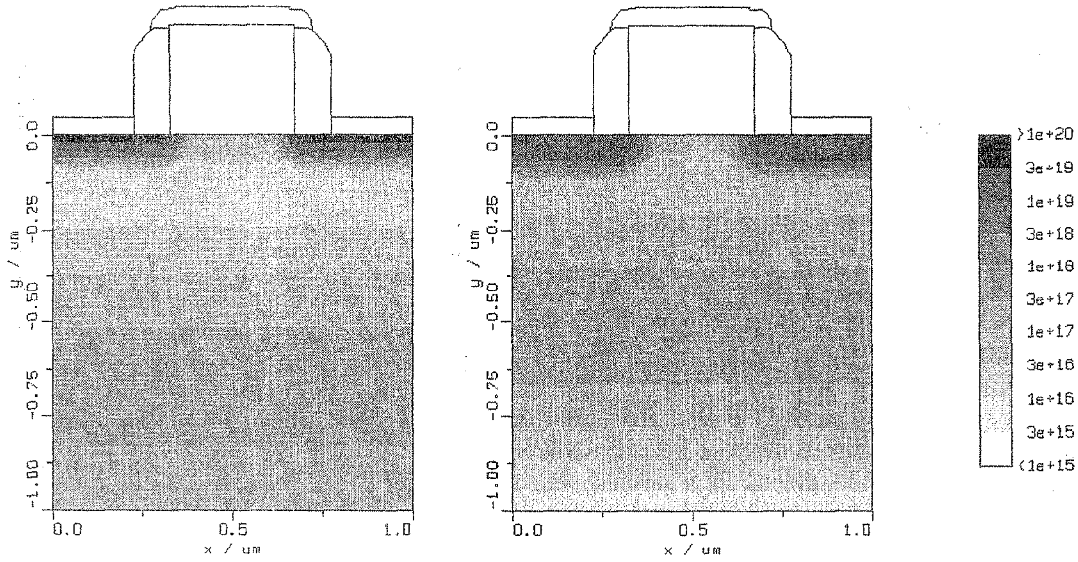

Figure 1: Doping profiles of ULP n-channel and p-channel transistors designed for digital operation at $V_{DD} = 200\text{mV}$ (process A)

The simulated processes were a $0.35\mu\text{m}$ process (A) for static logic and a $0.5\mu\text{m}$ process (B) for dynamic logic. The processes were designed for proper DC characteristics but were not optimized for speed. The essential simulation results are compiled in Tables 2 and 3. The device characteristics for process A are shown in Figs. 2 and 3. Figs. 4 and 5 show the noise margins and the inverter delay as a function of the supply voltage. Figs. 6 and 7 show the inverter transfer curves and the temperature sensitivity of process A. It can be seen that a ring oscillator built with process A would work even at $V_{DD} = 80\text{mV}$, and by using additional inverters at the gate inputs and outputs one could also design digital circuits for $V_{DD} < 100\text{mV}$, but the overhead of the additional components would be considerable.

Table 2: Simulated device characteristics. The threshold voltage was defined as $|I_D(V_T)| = 1\mu\text{A}/\mu\text{m}$. All voltages are in V, all currents are in $\text{A}/\mu\text{m}$

process	V_{DD}	$V_{T,n}$	$V_{T,p}$	$I_{off,n}$	$I_{off,p}$	$I_{on,n}$	$I_{on,p}$
A	0.2	0.067	-0.059	$0.14 \cdot 10^{-6}$	$0.27 \cdot 10^{-6}$	$16.7 \cdot 10^{-6}$	$9.4 \cdot 10^{-6}$
B	0.5	0.26	-0.24	$0.7 \cdot 10^{-9}$	$2.8 \cdot 10^{-9}$	$25.6 \cdot 10^{-6}$	$16.7 \cdot 10^{-6}$

Table 3: Noise margins (in $\%V_{DD}$) for a simple inverter and a 3-input NAND gate, and inverter delay, leakage time, switching energy, and static power consumption

process	$NM_{H,inv}$	$NM_{L,inv}$	$NM_{H,gate}$	$NM_{L,gate}$	t_d	t_l	E_s	P_{stat}
A	28	23	13	39	0.29ns	7.2ns	0.65fJ	41nW
B	38	44	31	49	0.55ns	1.3μs	4.3fJ	0.88nW

To see how close the two processes are to the absolute lower limits for V_{DD} we define the factors $X = V_{DD}/U_T$ and $X_{crit} = V_{DDcrit}/U_T$. Using (2) we get $I_{on}/I_{off} = \exp(V_{DDeff}/U_T)$, and we define

$$X_{eff} = \frac{V_{DDeff}}{U_T} = \ln \sqrt{\frac{I_{on,n} I_{on,p}}{I_{off,n} I_{off,p}}}. \tag{11}$$

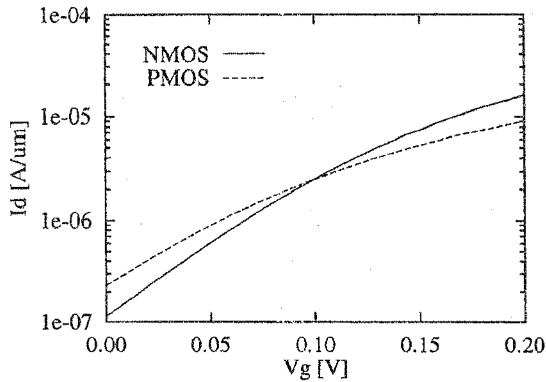

Figure 2: Input characteristics, process A ($V_{DD} = 200\text{mV}$)

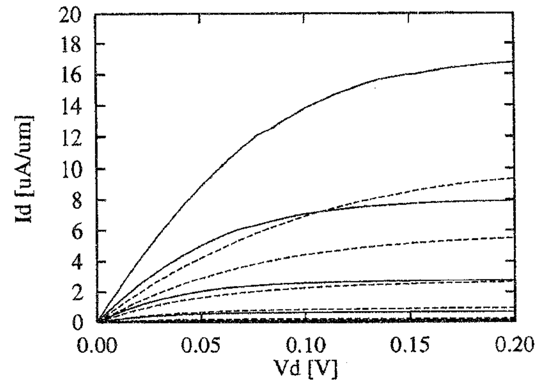

Figure 3: Output characteristics, process A ($V_{DD} = 200\text{mV}$)

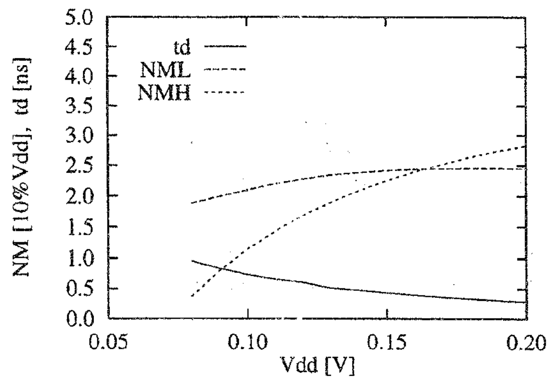

Figure 4: Noise margins and delay time vs. V_{DD}, process A

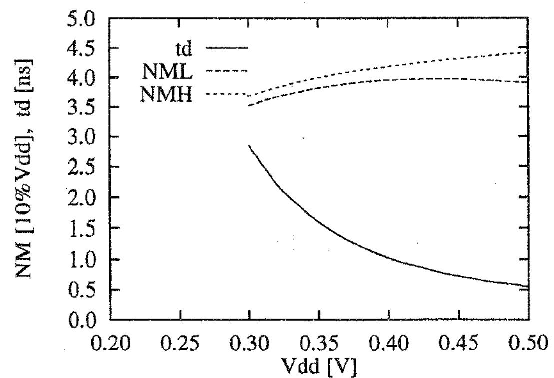

Figure 5: Noise margins and delay time vs. V_{DD}, process B

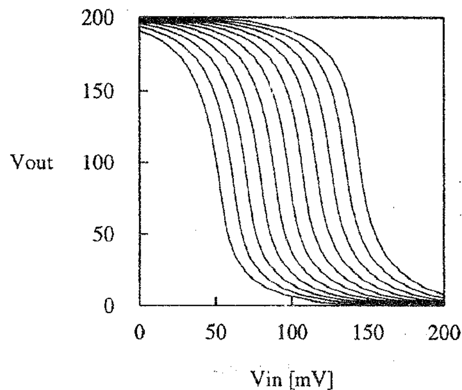

Figure 6: Inverter transfer characteristics for $W_n/W_p = 0.1...10$, process A ($V_{DD} = 200\text{mV}$)

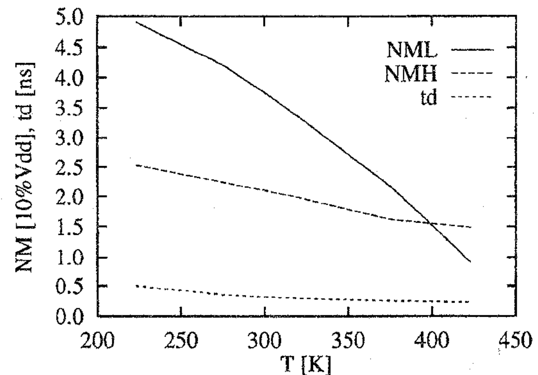

Figure 7: Temperature sensitivity of process A ($V_{DD} = 200\text{mV}$)

These data are compiled for the two processes in Table 4: The ratio X/X_{crit} tells how close a technology is to the lower limit of V_{DD}, regardless of the circuit performance. X/X_{eff} tells the percentage of V_{DD} which is used up to fulfill the criterion (cf. Table 1); the remainder serves to increase the performance. X_{eff}/X_{crit} is an indirect measure for the sensitivity of a process (for process A the ratio is 1.31; a value below 1 would mean a violation of the criterion).

Table 4: Supply voltage utilization

process	V_{DD}	V_{DDcrit}	X	X_{eff}	X_{crit}
A	200mV	83mV	7.8	4.2	3.2
B	500mV	238mV	19.6	9.6	9.2

From these data we conclude that the limits for the supply voltage will be around 200mV for static logic and 500mV for dynamic logic with a fan-in of 3 at T = 300K.

5 Mixed-Analog-Digital Technology

The recent development of low-power CMOS technologies has brought up a growing discrepancy between analog and digital technologies, especially, concerning the supply and threshold voltages. Traditionally, analog micropower designs favor higher threshold voltages $V_{Tn,p}$ and a supply voltage $V_{DD} > 1V$ [16], which is still higher than the end-of-discharge voltage of a single alkaline cell ($\approx 0.9V$) or the solar-cell voltage ($\approx 0.4V$). On the other hand, high-performance digital ultra-low-power technologies, requiring a comparatively small gain per stage, are optimized by lowering the supply voltage and the threshold voltages to a minimum.

For low-power mixed-analog-digital (MAD) systems it would be advantageous to have compatible ultra-low-voltage (ULV) analog components such as OPAMPs to keep the process technology simple. To find the lower limits of the supply voltage a set of basic circuits designed with dedicated digital ULP processes was simulated to determine the achievable performance.

To achieve an appropriate voltage gain almost all devices of ULV OPAMPs are operated in weak inversion (cf. (2)). An upper bound for the voltage gain of a single transistor loaded with an ideal current source can be derived as

$$A_{max} = \frac{1}{n}\left(e^{\frac{V_{DS}}{U_T}} - 1\right). \qquad (12)$$

This means that the gain is mainly determined by the available voltage drop V_{DS} of the amplifying devices. Another limit to the gain originates from the (bipolar) Early effect of submicron devices: $A \leq V_A/nU_T$. Cascoding can reduce the Early conductance of sub-micron devices, but also decreases the available V_{DS}. For process B an improvement was found only for $V_{DS} > 300mV$, i.e., $V_{DD} > 600mV$.

The MOSFET model used for circuit simulation is based on a physically motivated interpolation of the terminal currents and charges of the device [18]. These data are directly interfaced to a new circuit simulator, MINISIM [29], which uses charge conservative capacitance modeling. This approach avoids parameter fitting and rules out common problems like, e.g., discrepancies between the AC-model conductance parameters and the derivatives of the DC-model currents.

The simulation results of basic OPAMP types (OTA, folded-cascode OTA, and two-stage OPAMP) are shown in Figs. 8–13. We found that voltage gains of more than 60dB are possible at 0.5V and more than 38dB at 0.2V. The big advantage of this strategy is the compatibility of analog and digital devices which enables a simple ULP mixed-analog-digital process technology without compromizing performance on the systems level.

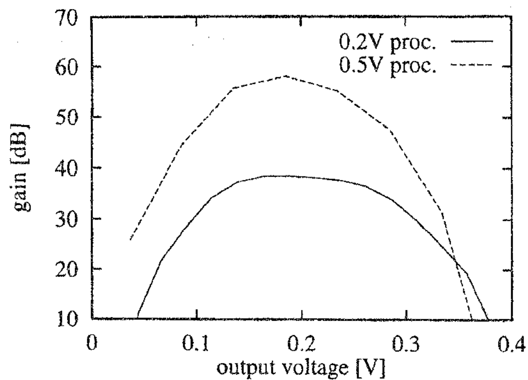

Figure 8: Voltage gain of two-stage ULV OPAMPs, operating at $V_{DD} = 0.4$V as a function of the output voltage (0.2V technology (a) and 0.5V technology (b))

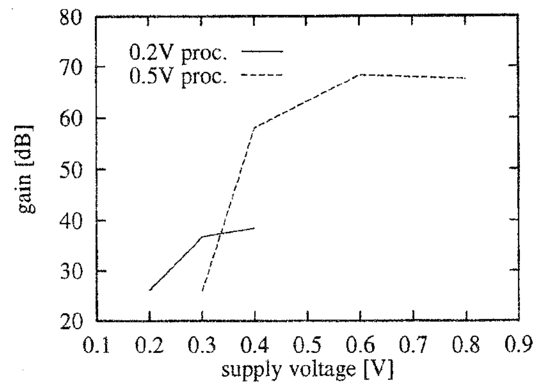

Figure 9: Maximum gain of two-stage ULV OPAMPs, operating at $V_{DD} = 0.4$V as a function of the supply voltage (0.2V technology (a) and 0.5V technology (b))

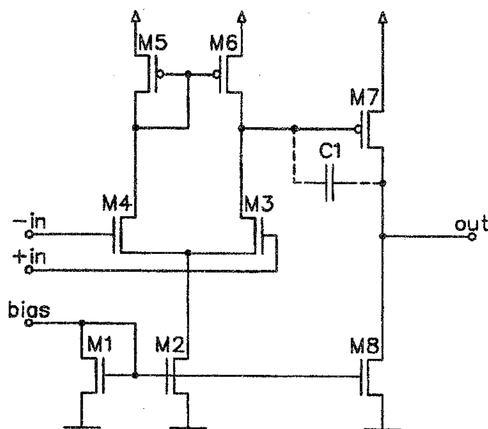

Figure 10: Two-stage OPAMP

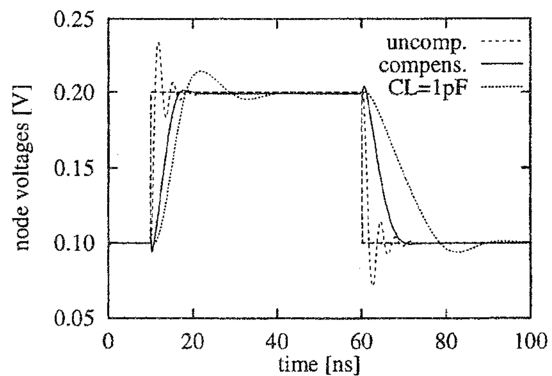

Figure 11: Step response of a two-stage ULV OPAMP (0.2V ULP technology) operating as a unity gain buffer at $V_{DD} = 0.3$V (uncompensated (a), compensated (b), and with $C_L = 1$pF, compensated)

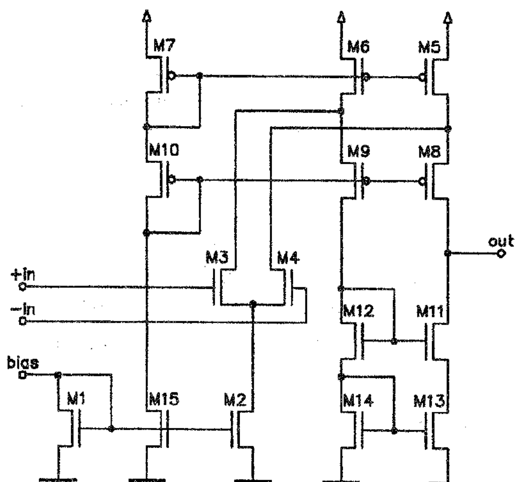

Figure 12: Folded-cascode OTA

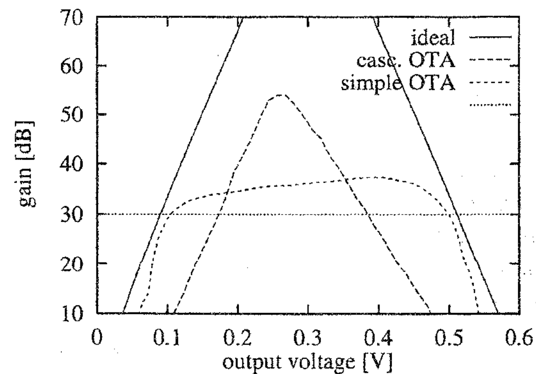

Figure 13: Voltage gain of a simple OTA and a folded-cascode OTA (0.5V technology), operating at $V_{DD} = 0.6$V as a function of the output voltage

6 Conclusion

The possibilities to accomplish a substantial reduction of the power consumption of CMOS technologies without performance loss were discussed. Lower bounds for supply voltage and switching energy were found to be $V_{DD} > 83\text{mV}$ and $E_s > 0.25\text{aJ}$ at 300K. The feasibility of ULP CMOS technologies was demonstrated by numerical simulation. Also, analog components, implemented in a digital ULP technology, were shown to work well even below 0.5V. Considering the current standard low-power supply voltages and switching energies, as well as the excellent scalability of ULP CMOS technologies, power savings of several orders of magnitude can still be achieved.

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