Modeling Integrated Circuit Interconnections

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Abstract

The minimum feature sizes of integrated circuits were reduced to a stage where interconnections between the active devices strongly influence deep-submicron circuit performance. To efficiently model interconnect structures we introduce a set of tools to perform precise three-dimensional capacitance and resistance extraction. The interconnect structures are generated automatically from layout data and a given process description using complete and accurate topography simulation with previous optional lithography analysis. Thus at a process design phase, problems can been foreseen and corrected. The capacitance and resistance/thermal extractor simulators are based on optimized finite element methods and the topography simulators use a cellular data based approach.

1 Introduction

As Integrated Circuits (IC) are being scaled-down, the influence of interconnections in circuit performance increases. In deep-submicron technologies such influence is so strong that a careful and precise interconnect modeling is mandatory. Several software packages were reported to extract capacitances and resistances in three dimensions. Since we are interested in very accurate simulations, fast procedures based on analytic models [1] are not considered. Only numerical approaches can be used to fully and exactly characterize interconnect structures. Methods such as finite differences [2], boundary elements [3], finite elements [4], [5], multipole algorithms [6] and stochastic [7] have been reported to perform these tasks.

The applicability of three-dimensional interconnect simulators is limited by its input data. Their formats change widely and the input processes are usually extremely time consuming and error prone (eg. geometry-based input formats entered manually). Thus, they can be used only in simple applications or using a rough solid model of the structure to analyze. To solve this problem we present a set of layout-driven CAD tools where the automatically created three-dimensional structures are derived from accurate topography simulation. Simple models for non-critical steps (eg. a wire in METAL1 where the surface is sufficiently planar) can be also used. This allows the reduction of calculation time and simulation resources, while maintaining an high overall accuracy.

The input data are simple to create, as only a layout file (either in CIF or GDSII format) and a process recipe is required. The first is the result of an integrated circuit design and the process recipe is a set of actions corresponding to process steps as in a real fabrication facility. The result is a circuit-level electrical model, compatible with standard circuit simulators as SPICE.

As we enter in deep-sub-micron technologies what is effectively printed in the silicon may not follow the layout due to lithography phenomena. Using an aerial simulator (if necessary) we take these deviations in consideration.

The complete data-flow of the proposed tools is shown in Fig. 1. The basic concept is to link integrated circuit designers with the accurate tools found in Technology CAD (TCAD) environments to extract the interconnect characteristics. As consequence the conservative design rules of a conventional VLSI circuit design (where the design and fabrication phases are uncorrelated) can be relaxed, resulting in more compact circuits with improved performance and functionality, while keeping good yield capabilities.

2 Layout Specification

In the TCAD framework VISTA [8], the tool PED is used to handle layout data [9]. It can edit small pieces of layout from scratch or convert layouts in CIF and GDSII stream formats created elsewhere

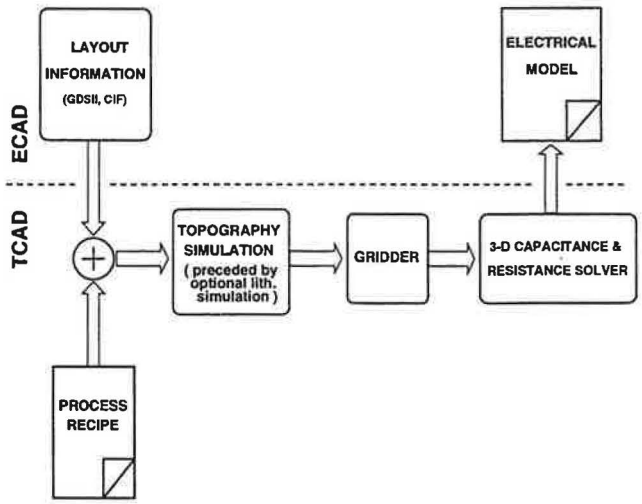


Figure 1: Data flow and block diagram of proposed tools.

to the VISTA internal data representation. With a user-friendly interface it allows to perform boolean operations with the masks and to define simulator specific information as the net or contact names. This information is kept along all the simulation phases and the extracted capacitors and resistors are annotated accordingly at the end.

Another important feature of our TCAD oriented layout editor is the automatic generation of layout sets. This resource is consequence of in developing new processes a large number of variations of some geometric parameters is required. This sets can be linked with optimization procedures or Response Surface Methodology (RSM) to investigate in detail the coupling between layout and device/circuit performance.

As shown in Fig. 1 we can precede the topography simulation with a lithography analysis. To handle the more efficient phase-shift masks [10], the layout editor can handle the modulus and phase values of their transmittance. As complete lithography simulation flow (with aerial image calculation, exposure, baking and development) is too complex and time/resources consuming, we use a simplification where only the aerial intensity image is calculated. Then, it is compared at each point with a threshold value in order to generate a binary aerial image that is used as a conventional binary mask in the further process simulation steps. This also allows the use of phase shift masks without any special processing. The threshold can be entered manually or calculated automatically in the same way as in [11]. To compute the aerial intensity image on the resist, the simulator illum2d [13] which is tightly connected with PED is used. A report of printability of the simulated layout is also generated, and the critical nets (if existing) are pointed out.

Fig. 2-left shows the aerial image of the mask METAL2 of an imported layout with an imaging system that uses a lens with a numerical aperture NA of 0.55, a wavelength of 365 nm (I-line) and the focus error is 1 μm. The resulting binary mask is shown if Fig. 2-right. Note the typical effect in the nested elbows where the corners become bloated and the elbows rounded.

3 Topography simulation and grid generation

The simple way to generate a solid model of the interconnect structures is to project the layout of the correspondent mask in the third-dimension associated to some thickness. The several layers are separated by a dielectric with also some thickness value. This procedure introduces large errors when the real structures are strongly non-planar, where an real topography simulation must be performed. In this case, we use the three-dimensional topography simulator etch3d [12]. This program uses methods based on morphological operations derived from image processing, which are performed on a cellular material structure where the formation of unphysical surface loops is completely avoided. The simple model is used in cases where a perfect planarization can be assumed.

In the cellular format, materials are represented as a three-dimensional array of cubic cells, where each byte maps to a unique material (and zero its absence). Although presenting several advantages as pointed out in [12], due to the nature of this data format there are problems in the linkage with the finite element based capacitance and resistance/thermal simulators that require a tetrahedral grid.

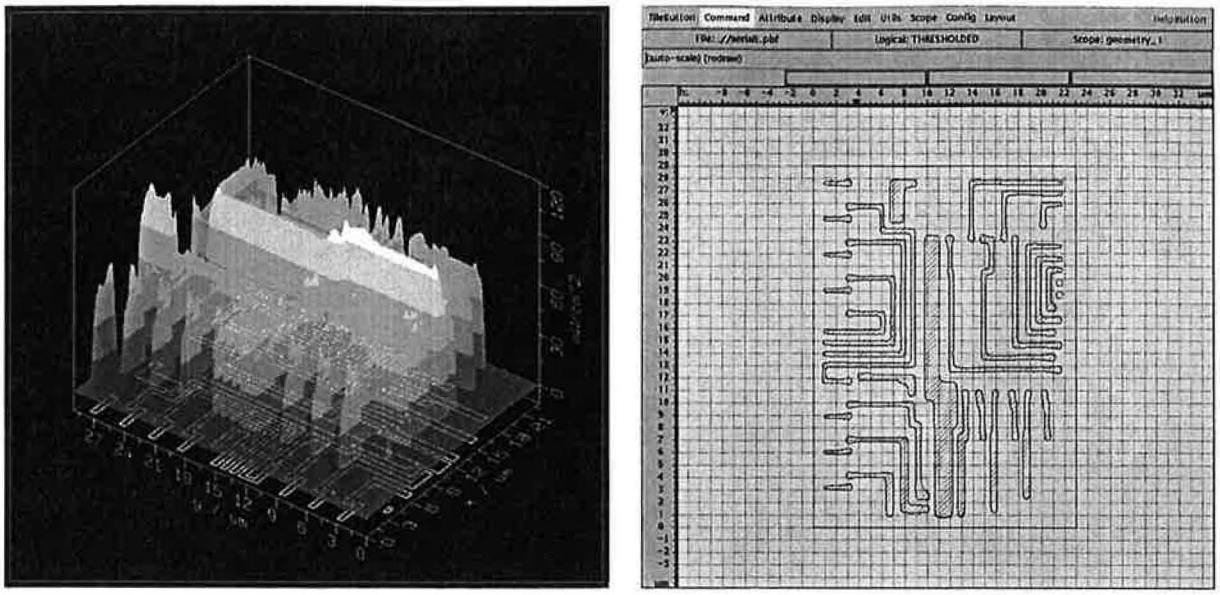


Figure 2: Left- Aerial image of an imported layout. Right- Resulting binary mask.

The preprocessor laygrid [14] was written to generate three-dimensional (tetrahedral) grids compatible with the used finite-element simulators. It is very simple to link with the layout information as the structure are formed and grided by stacking planar layers (that are associated with some thickness). Each layer is made of faces with contacts (specifying net names and external voltage/current conditions) and material references. In the stacking process all new cutting faces are calculated and at the end each layer is grided with Shewchuk's triangle [15].

Although it is based on a layered description, it can be applied to grid the structures created by the topography simulator. The basic concept is to sample planes in the Z-direction of the array of cubic cells. Each plane can be viewed then as a bitmap image with pixel colors equal to the material indexes. If an edge-detection algorithm is applied, polygonal faces defining material boundaries are found and can be used to build one layer of the structure. A new layer is inserted if the difference between the actual image and the last inserted is larger than an error criterion. As along with the number of inserted planes, the number of grid nodes increases (which means more memory and time needed to perform the consequent simulations), efficient sampling must be performed having in attention however, that the differences between the original and the reconstructed structures, must be kept small. Simple algorithms based on an overall error over the image are not satisfactory, as they tend to ignore small features details. The following algorithm overcomes this problem:

1. Divide the plane in regions of the same material R_{Mi} and for each one, calculate its area $A(R_{Mi})$. This means counting the number of adjacent cells with same index.

2. Add each R_{Mi} to the equivalent in the last written plane. Equivalent means that they have the same material and they overlap somewhere. Calculate the area of the sum $A(Sum_i)$ in the same way as $A(R_{Mi})$.

3. For all R_{Mi} calculate:

$$Error_i = \frac{A(R_{Mi})}{A(Sum_i)}$$

4. If any of $Error_i$ is larger than a certain value, this plane is written, otherwise jump to the next plane.

An advantage of this gridding procedure is its simplicity and robustness. Also, it allows to easily build structures that are partially derived from real topography simulation and partially created directly from the layout. This is the case in Fig. 3-right where the trench capacitor is formed by real topography simulation and the poly-gate and metal lines are obtained directly from the layout of Fig. 3-left. In order to round the corners of the bottom of the capacitor, an oxidation and stripping step was made before

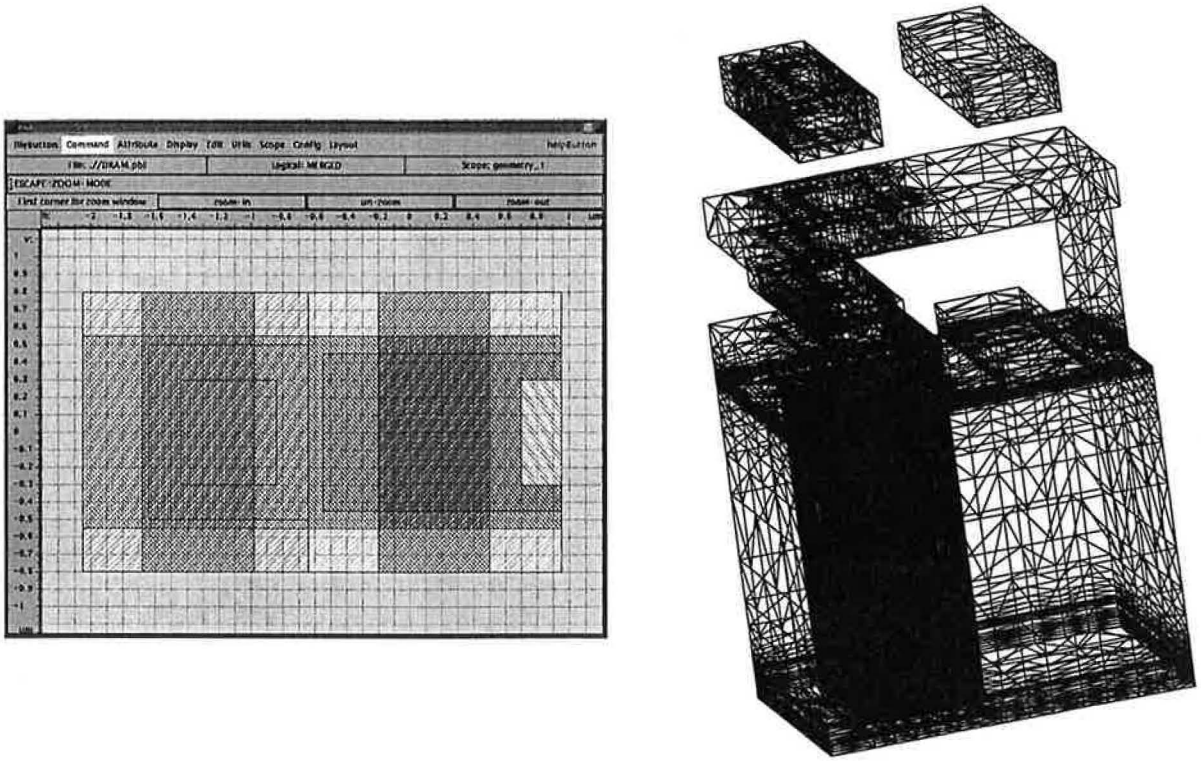


Figure 3: DRAM cell with a trench capacitor: Left- Cell layout. Right- Resulting grid.

forming the actual SiO_2 dielectric film. As this is only 10 nm thin, a very large number of grid points are necessary to resolve such small dimensions as it is seen in Fig. 3-left. The adaptive sampling mechanism of Z-planes in the grid can also be seen.

4 Capacitance and Resistance/Thermal Simulation

In a circuit with n nets (made physically with conductive materials) there are always $\frac{1}{2}n(n-1)$ capacitors $C_{i,j}$ across them. To calculate the capacitance values the energy method is used, as high numerical accuracy is achieved. The equations that are following described are solved using optimized finite element methods in the programs SCAP [4] and STAP [14].

The energy W in a system with n conductors is

$$W = \frac{1}{2}\sum_{i=1}^{n}\sum_{j=i+1}^{n} C_{i,j}(\psi_i - \psi_j)^2.$$

Therefore we must apply $\frac{1}{2}n(n-1)$ different potential conditions and solve the resulting linear system to obtain all capacitor values. The electrical field φ for each partial capacitance pair is obtained by solving the Laplace's equation

$$div(\varepsilon\ grad\varphi) = 0$$

where ε is the permitivity tensor.

A similar equation must be solved to calculate the current density and potential distribution inside the conductors (and also to extract the resistance of that conductor). If γ_E denotes the electrical conductivity and that it is assumed to be 0 in all non-conductor materials we obtain

$$div(\gamma_E\ grad\varphi) = 0.$$

In order to include thermal effects in the value of the extracted resistors, the solution of

$$div(\gamma_T\ gradT) = -p$$

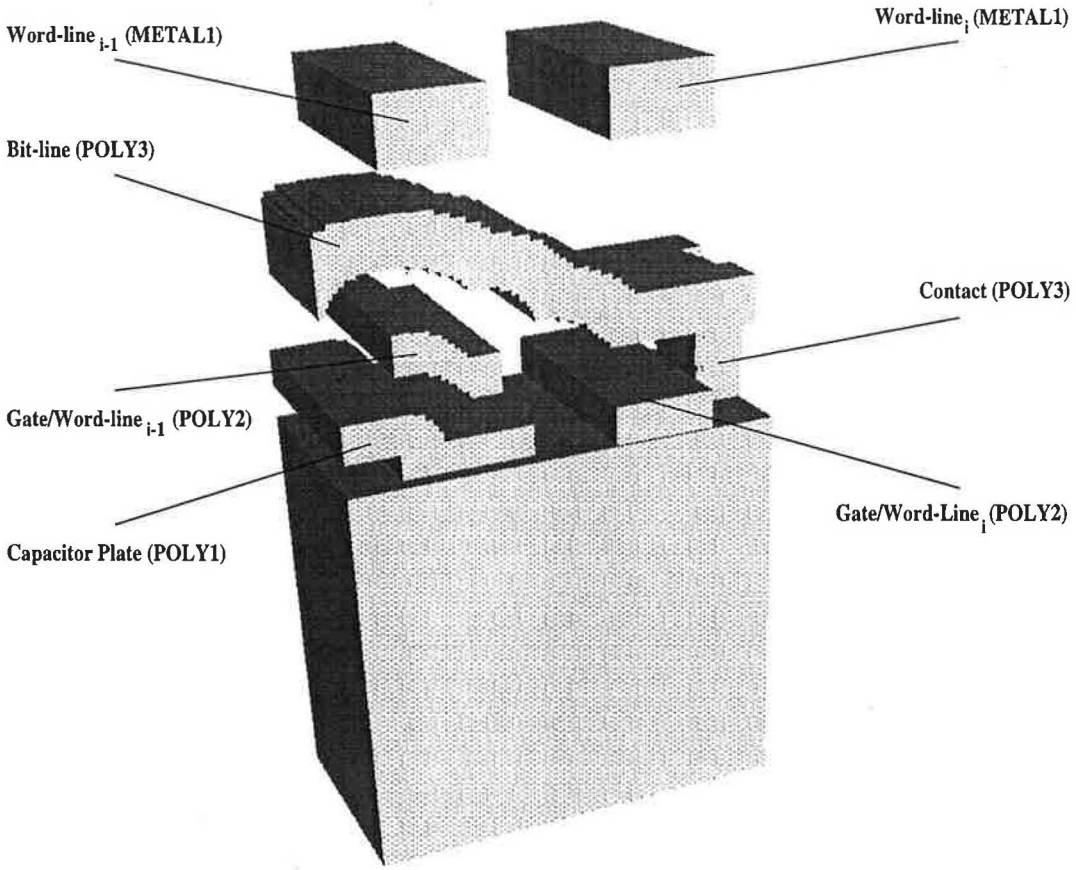


Figure 4: Solid model of the DRAM with topography simulation of interconnect lines.

in all simulation domain is also required. Here γ_T represents the thermal conductivity and $p = \gamma_E \ (grad\varphi)^2$ is the power loss density. The electrical and thermal equations are combined by a first order approximation given by

$$\gamma_E = \gamma_0 \ \frac{1}{1+\alpha \ (T-T_0)}$$

where α is a constant temperature coefficient, and γ_0 is the electric conductivity at room temperature T_0. A equivalent model is used for the thermal conductivity. After several iterations the equilibrium temperature distribution is reached and the resistance is extracted.

5 Examples

5.1 DRAM Cell

The dynamic RAM (DRAM) products are the driven force in semiconductor industry. The proposed tools are suitable to assist the design of new cells with reduced area, what leads to higher bit densities. As in a DRAM the information is stored as charge in a capacitor, a good characterization of this and the total bit-line parasitic capacitance is of paramount importance in the development of new cell configurations. With our tools we can simulate the strongly non-planar topographies of the elements of the cells, namely the storage capacitor and the bit-line.

We present results obtained on a variation of the stacked trench cell [16] which layout was shown in Fig. 3-left. Two cases were considered. In the first case a simple interconnect model is used (see Fig. 3-right) and in the second the topography simulation was performed to all the cell (the resulting solid model is in Fig. 4). The results in Table 1 demonstrate the much better agreement of the second case with the experimental data, revealing an improvement in the error of $C_{trench}/C_{bit-line}$ with a factor of 5. They are explained from the non-planarity of the bit-line and demonstrate the need for precise topography simulation. The value of $C_{trench}/C_{bit-line}$ in Table 1 is for the case of 128 cells sharing the same bit-line.

Table 1: Results of DRAM cell simulation.

	Planar fF	Non-planar fF	Measured fF
C_{trench}	40.1	40.1	38.2
$C_{bit-line}$	1.04	1.72	1.88
$C_{word-line}$	2.22	3.35	-
$C_{bit-line,word-line}$	0.34	0.42	-
$C_{trench}/C_{bit-line}$ (128 cells)	3.3	5.5	6.3

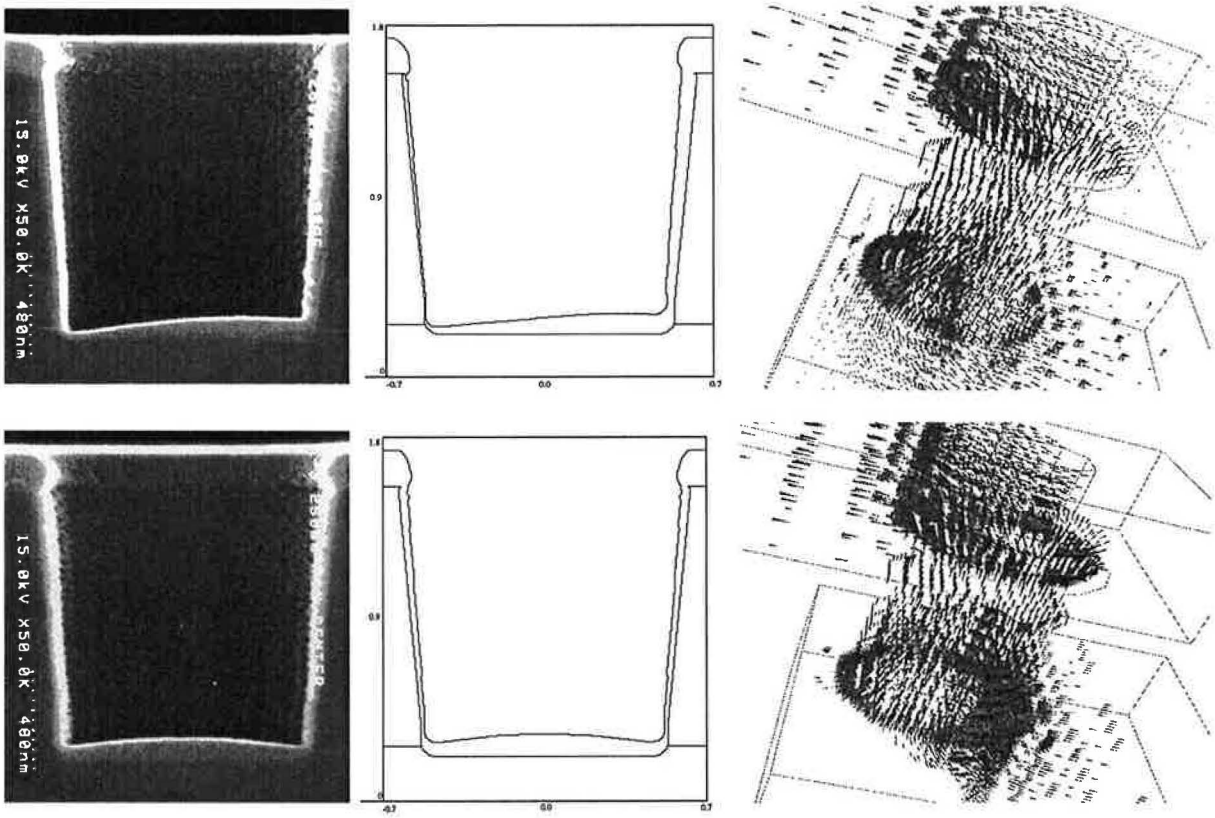
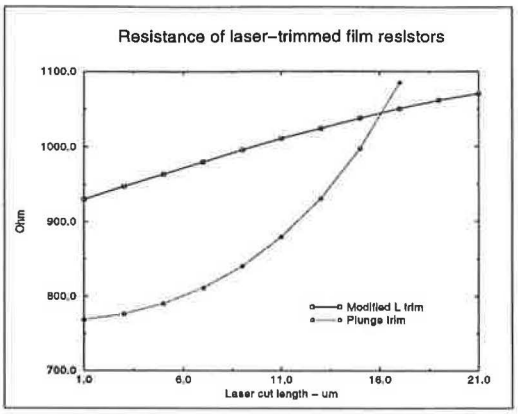


Figure 5: Contact simulation: Left - SEM picture (after TiN sputtering). Middle - Result from topography simulation (a cut is shown). Right - Current density in the contact.

5.2 Contact Resistance Analysis

Contacts and vias are very important elements in the reliability of integrated circuits. A good characterization at the design phase can avoid problems that will reveal much later, like those posed by electromigration. With the proposed tools it is possible to analyze the current distribution inside the conductive materials. As example we present results on a contact structure where a titanium nitride barrier layer is used to metallurgically insulate the metal from the semiconductor. In Fig. 5-left we show SEM pictures after a TiN deposition into a 1.0 μm circular hole located 260 mm below the center of the sputter target disk (bottom picture) and when the deposition of TiN is made at a position 90 mm off the wafer center (top picture). The center pictures, cuts from the simulated three-dimensional structures agree well with the SEMs. In Fig. 5-right we show the current density in the two contacts, after being filled with aluminium. The effect of the asymmetry in the TiN layer in the current density is clearly seen. In the top case the current flows mainly in an abnormal area, namely in the trailing edge of the contact, whereas in the other case we have the known current crowding effect at the opposite edge. As electromigration problems are worse with current crowding effects [17], this study can be very useful. The resistance values obtained were 0.77 Ω and 0.89 Ω respectively for the upper and lower case and agree well with the experiments.



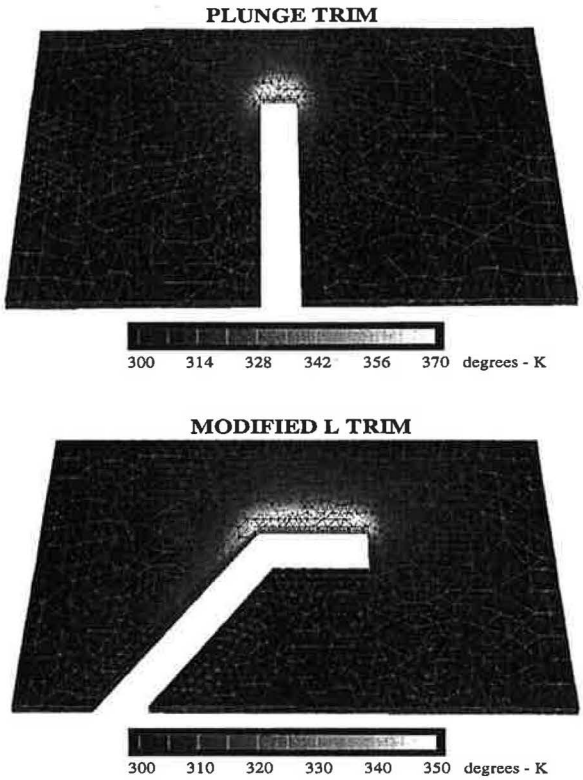


Figure 6: Laser trimmed resistors: Left- Resistance versus cut-length. Right- Temperature distribution when trimmed to 1000 Ω.

5.3 Laser Trimmed Resistors

Laser trimming of film resistors allows integrated circuits manufacturers to accurately control resistance values. As it is an expensive process step, it is important to maximize the benefits once that option is taken. Our electrical/thermal simulator allows the characterization of the most important parameters of this devices, such as the Heat-Affected Zone (HAZ) [18] and the resistance sensibility to a cut imprecision, for different trim algorithms. The HAZ is formed during the trimming process and corresponds to a region along the edge that being heavily heated (but still below the vaporization temperature) after cooling suffers an alteration in its physical properties, namely in the sheet resistance, temperature coefficient, and aging. We model the sheet resistance of HAZ as in reference [18]. The use of parameterized layout generation, facilitates the preparation of sets corresponding to different lengths of the laser cut. The simulated structures are then formed directly from the layout, and are made of a silicon substrate, a SiO_2 layer, the high-resistivity polysilicon resistor layer and finally, a passivation SiO_2 layer. The bottom of the silicon substrate is kept at a constant temperature of 300°K. We analyzed the conventional plunge-trim and a modified L-trim resistor (nominal value is 1000 Ω) as in Fig. 6 with the same dimensions and geometry before trim.

From Fig. 6-left which shows the dependence of the resistance value as function of the cut-length we observe a much higher sensibility of the plunge-trim near the targeted value. In Fig. 6-right we display the temperature distribution in the resistive material. In both cases we notice the crowding effect in the HAZ (corresponding to the maximum values in the current and temperature), but in the plunge-trim this effect is more severe as higher temperatures are reached for the same overall power dissipation (note the scale values). As the stability of material properties degrades with temperature, a better aging for the modified L-trim is expected.

6 Conclusions

To accurately model integrated circuit interconnections there is a need of precise topography simulators. We proved that simple planar three-dimensional models are too inaccurate. We propose a layout driven alternative that being simple to use achieves very good accuracy solving capacitance and resistance/thermal problems. It uses three-dimensional structures created with TCAD topography simulators and can take lithography effects in consideration. Some possible applications were presented and discussed.

Acknowledgments

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