Simulation of a Single Electron Tunnel Transistor with Inclusion of Inelastic Macroscopic Quantum Tunneling of Charge

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We simulated a Single Electron Tunnel (SET) Transistor with the full inclusion of inelastic macroscopic quantum tunneling of charge (q-MQT) or co-tunneling. Numerical results of the q-MQT effect over a wide range of bias and gate voltage were achieved.

A Monte Carlo method was used to simulate electrons that tunnel back and forth through the two tunnel junctions of the SET transistor and co-tunnel back and forth through both junctions simultaneously.

Resonances in the I-V characteristic were found. The resonant peaks decrease with increasing temperature. The origin of this resonance is the q-MQT or co-tunnel effect in contrast with the normal resonant tunneling in double barriers.

Keywords: tunneling; single electron tunneling; macroscopic quantum tunneling; co-tunneling; resonant tunneling; monte carlo simulation

1. INTRODUCTION

Already many single electron tunnel (SET) devices were proposed and studied, e.g., single electron transistor [1], single electron memory cell [2], single electron turnstile [3], single electron pump [4]. Very often macroscopic quantum tunneling of charge (q-MQT) is completely neglected or treated in an approximate way. Regarding q-MQT the best studied device is probably the single electron pump. Nevertheless, in the literature q-MQT is either neglected or approximated. We are dealing here with a rigorous description of q-MQT.

2. THE SIMULATED STRUCTURE

Figure 1 shows the investigated SET transistor. The basic operation of the SET transistor is that electrons tunnel through the junctions from one side to the other, thus a current I will flow. With the gate voltage it is possible to suppress this normal tunnel current. But even if electrons can not tunnel through a single junction, they will co-tunnel through both junctions via a virtual intermediate state. This co-tunnel current is the main contribution to the current I in the Coulomb blockade regime. This structure exhibits a Coulomb blockade for tunneling through the first junction if $E_1 > 0$ and a Coulomb blockade in the second junction if $E_2 > 0$, with
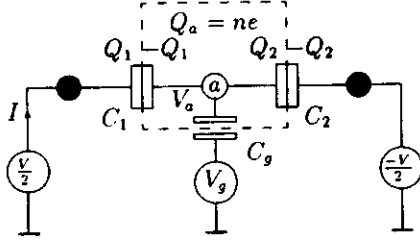
FIGURE 1 SET transistor consisting of two tunnel junctions in series, that form an island a. The device is biased with an ideal voltage source V, and a gate voltage V_g

$$E_1 = \frac{e}{C_\Sigma}\left(e(n+\frac{1}{2}) - V(C_2 + \frac{C_g}{2}) + V_g C_g\right) \quad (1)$$

$$E_2 = \frac{e}{C_\Sigma}\left(e(\frac{1}{2} - n) - V(C_1 + \frac{C_g}{2}) - V_g C_g\right), \quad (2)$$

where $C_\Sigma = C_1 + C_2 + C_g$, and n is the number of electrons on the island a before the tunnel event.

3. MONTE CARLO SIMULATOR

The basic outline of the simulator is as follows. First, the six tunnel rates, normal forward and backward tunneling in the two junctions and forward and backward q-MQT across both junctions, are calculated according to [5]. Then to every possible tunnel event

the elapsed time to the next occuring event is simulated according to a Poisson process.

$$t = -\frac{\ln(r)}{\Gamma} \quad (3)$$

Here, Γ is the tunnel rate corresponding to one of the six possible tunnel events and r is an evenly distributed random number between 0 and 1. The shortest time of the six events determines the actual happening event. The same approach was used by Kirihara et al. [6], but without considering q-MQT. Then the charge on the island is updated and the tunnel rates are calculated according to the new state. The simulation is done for a particular temperature and gate voltage. To obtain the output current, the electrons that tunnel through both junctions are counted and divided by the total simulation time. For one particular value of the bias voltage many thousand tunnel events were averaged to yield a smooth noise free I-V and I-Vg characteristic.

4. I-V AND I-Vg CHARACTERISTIC

For zero gate voltage and a structure with a Coulomb energy of 34 meV the I-V characteristic is shown in Figure 2. A small resonant peak is visible. As can be seen in the right picture which is an enlargement of the resonant peak, the resonance decreases with increasing temperature. Our simulations were done without taking the finite width of the charge states of
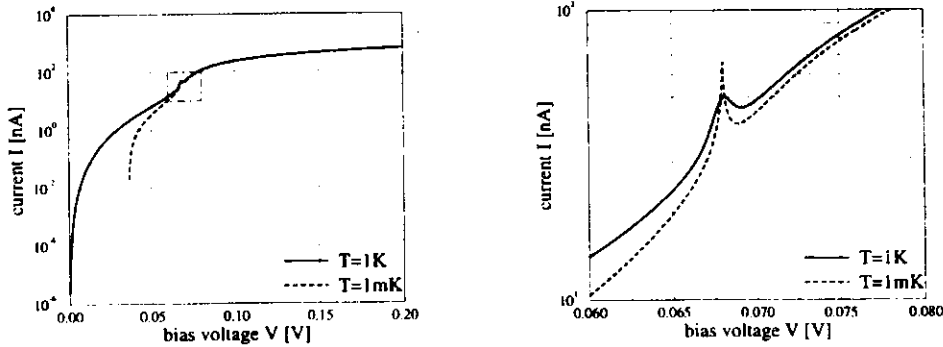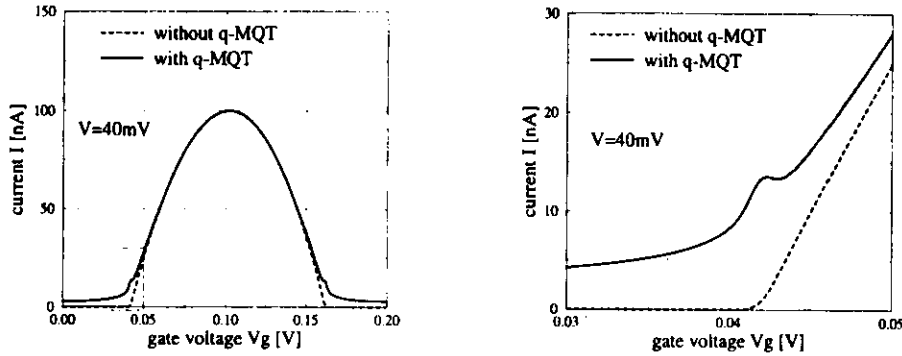

FIGURE 2 I-V characteristic for a SET transistor, $E_c = 34$ meV and $V_g = 0$V

FIGURE 3 I-Vg characteristic for a SET transistor, $T = 1$ K, $E_c = 34$ meV

the transistor into account. Thus, we consider very low conductance tunnel junctions only. An inclusion of this effect should dampen the resonances.

Figure 3 shows the I-Vg characteristic again with an enlargement of one resonant peak. Fig. 3

Fig 4 shows the gate voltage dependence of the I-V characteristic for the same transistor. Note that the graphs are separated by an offset. For each graph $I(0) = 0$ holds. One can see the suppression of the Coulomb blockade due to the applied gate voltage, which induces additional charge on the island a. Again resonance peaks are visible. Their locations change with V_G. The right picture shows the I-V characteristic without the inclusion of the q-MQT effect.

Therefore the coulomb blockade is much sharper and no resonances are visible. Thus, one can see that the rounding of the coulomb staircase at low temperatures is only due to q-MQT. The thermally agitated normal tunneling plays at this temperatures a minor role.

References

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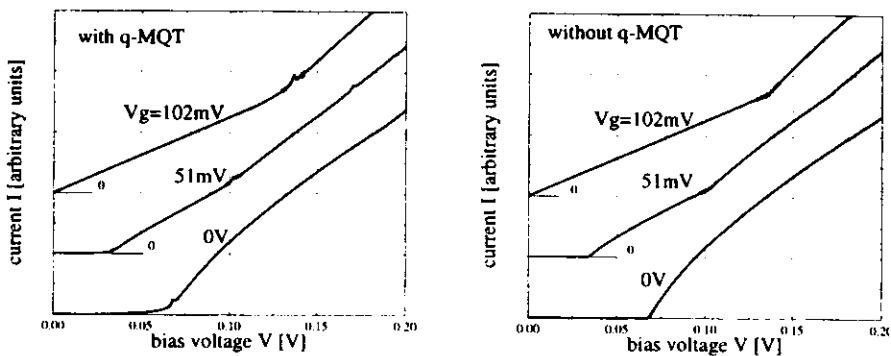
FIGURE 4 I-V characteristic for a SET transistor, $T = 1$ K, $E_c = 34$ meV, with V_G as parameter

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Biographies

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