SAP — A Program Package for Three-Dimensional Interconnect Simulation

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Abstract

We introduce a set of simulation programs for two- and three-dimensional analysis of interconnect structures. The simulators are based on the finite element method and can be used for highly accurate capacitance extraction, resistance calculation, transient electric and coupled electro-thermal simulations. Furthermore, the program package includes two preprocessors that support a layer based input language and an automatic grid generator. Two application examples are given.

Introduction

In deep submicron designs the interconnect structures significantly determine the overall circuit behavior [2]. Due to the tremendous increase in device speed, the delay caused by the interconnect resistance and capacitance becomes larger in comparison. From the aspect of circuit reliability the knowledge of the current density and temperature distribution in the wiring structures is important to prevent electromigration. Careful investigations during the design phase become necessary. Since experimental measurements of these physical effects are often expensive, inaccurate, or impossible, there is an increasing need for numerical calculation.

Conventional ECAD tools supply analytical models for resistance and capacitance extraction, which allow to calculate the delay time, the generated heat, and to estimate the increase in temperature. Since this approach often proves as too inaccurate, a fully three-dimensional simulation becomes necessary. General purpose FEM packages do a good service for this task, but the specification of models, geometry and boundary conditions is a difficult and time consuming job. For this reason the simulation package SAP (Smart Analysis Programs) was developed. It has been designed specifically for interconnect applications, thus enabling a high level of performance.

Mathematical Models

A. *Capacitance and Resistance Extraction*

For the capacitance extraction we use the finite element method to calculate the electric potential φ inside the insulator domain by solving the Laplace equation

$$\operatorname{div}(\varepsilon(x,y,z)\,\operatorname{grad}\varphi) = 0, \tag{1}$$

where ε denotes the permittivity tensor. Conductor surfaces are represented by Dirichlet boundary conditions.

The calculation of resistances is performed in a similar manner by solving

$$\operatorname{div}(\gamma(x,y,z)\,\operatorname{grad}\varphi) = 0 \tag{2}$$

in the domains of conducting material, where γ is the conductivity.

B. *Transient Electric Simulation*

Usually delay times or crosstalk on interconnect lines are calculated analytically based on extracted distributed resistances and capacitances (The effect of the magnetic field can be neglected in most applications). This approach is exact only for straight lines. For general structures more accurate results can be achieved by solving the transient potential distribution function

$$\operatorname{div}(\gamma\,\operatorname{grad}\varphi + \varepsilon\,\operatorname{grad}\frac{\partial\varphi}{\partial t}) = 0 \tag{3}$$

again using the finite element method.

C. *Thermal Interconnect Analysis*

For the calculation of the distribution of the temperature T the heat conduction equation

$$\operatorname{div}(\gamma_T\,\operatorname{grad}T) = p - c_p\rho_m\frac{\partial T}{\partial t} \tag{4}$$

has to be solved, where γ_T represents the thermal conductivity, c_p the specific heat and ρ_m the mass density.

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The power loss density p is derived from the electric potential φ resulting from (2)

$$p = \gamma_E (\text{grad}\,\varphi)^2. \tag{5}$$

For the dependence of the electrical resistivity of the conductors on the temperature we use a linear model:

$$\gamma_E = \gamma_0 \frac{1}{1+\alpha(T-T_0)}. \tag{6}$$

γ_0 is the electrical conductivity at the temperature T_0 of 300K, and α is a constant temperature coefficient. The temperature dependence of the thermal conductivity is very low for commonly used interconnect materials and can be neglected in most applications.

For accurate simulation results it is important to specify a sufficiently large simulation domain. We found that the lateral extension of the simulation area should be at least 1.2–1.5 times the vertical dimension of the thickest layer (i.e. the Si substrate) but it is possible to omit small geometric features in areas where accuracy is not critical. Decreasing the simulation domain first causes an error in the calculated temperature while current densities and temperature gradients still may be accurate.

The Simulation Package SAP

The two main programs (SCAP: capacitance and resistance extraction and STAP: transient electric/thermal analysis) use the finite element method to solve Laplace's and Poison's equations. For time dependent problems, the Backward-Euler and Crank-Nicholson methods have been implemented. Triangular and tetrahedral grid elements can be used for two- and three-dimensional simulations. The calculations can be performed with linear and quadratic shape functions. For efficient utilization of computer memory the sparsely occupied stiffness matrix is stored in a compressed format (MCSR). A preconditioned conjugate gradient solver is used to solve the large linear systems. For highly accurate results a global grid refinement algorithm is implemented.

Two preprocessors (LAYGRID and CUTGRID [1]) are used for specification of the simulation geometry and contacts (both electrical and thermal) in terms of polygonal layers. The preprocessors are also responsible for the generation of the simulation grid. In two dimensions the mesher called Triangle [8] is used, for the three-dimensional case we perform a layer-based grid generation method [3]. A tool for importing layout files in GDSII or CIF format is available [4]. The calculated potential, current density, and temperature profiles can be inspected with a visualization program (based on [7]).

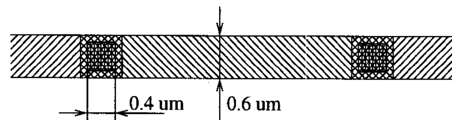

Fig. 1: Layout of Tungsten-via test structure.

Application Examples

A. Thermal Analysis of a Via-Chain Structure

A chain of Tungsten vias is a commonly used test structure in reliability experiments (see Fig. 1). Thicknesses of the layers are 600nm for SiO_2, 580nm for Metal 1+2 (40nm/60nm Ti/TiN barrier, 440nm AlCu(0.5%), 40nm TiN ARC), and 700nm for the passivation. Table 1 shows the material properties used for the simulation.

A current of 34mA is applied to the ends of the line, which is equivalent to a current density of approximately 13MA/cm^2 in the AlCu line and approximately 21MA/cm^2 in the Tungsten-plug. The bottom of the Si-Substrate is kept at constant temperature of 24°C.

Since the geometric structure repeats periodically it is only necessary to simulate one single via. The high resistivity of TiN causes a large voltage drop at the bottom of the W-plug resulting in a high heat generation rate.

Fig. 2 shows the temperature profile cross-section. The maximum temperature of 99°C occurs on the bottom of the Tungsten plug and coincides well with the heat generation rate.

Fig. 3 shows the temperature distribution after 1ns on the surface of the half via structure.

B. Crosstalk Analysis

The test structure for capacitive crosstalk experiments consists of two parallel, 0.6μm wide interconnect lines. The layer thicknesses above the silicon substrate are 0.5μm SiO_2, 0.5μm Metal 1, and 0.8μm passivation oxide. Each line is 40μm long. On one end a voltage step from 0V to 1V is applied to the first line, while the second line is constantly connected to 0V. The voltage on the other side of the lines and has been calculates and is shown in Fig. 4. Although the second line is grounded a

Table 1: Material properties.

Material	ρ [$\mu\Omega$cm]	α [1]	γ_T [$\frac{W}{mK}$]
Al-0.5%Cu	3	0.0042	238.00
Ti	60	0.0041	15.00
TiN	600	0.0041	10.00
W	10	0.0038	140.00
Si			84.00
SiO_2			1.35

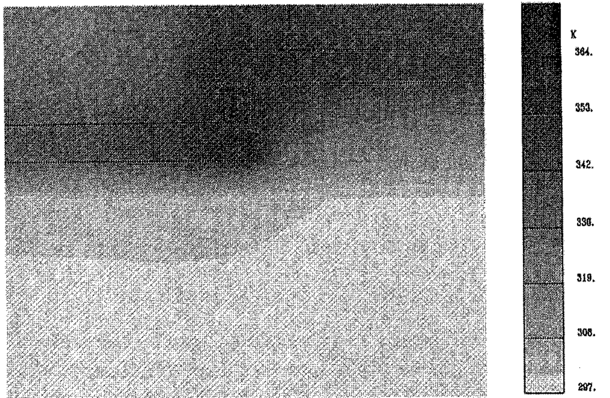

Fig. 2: Cross-sectional temperature profile of the test structure.

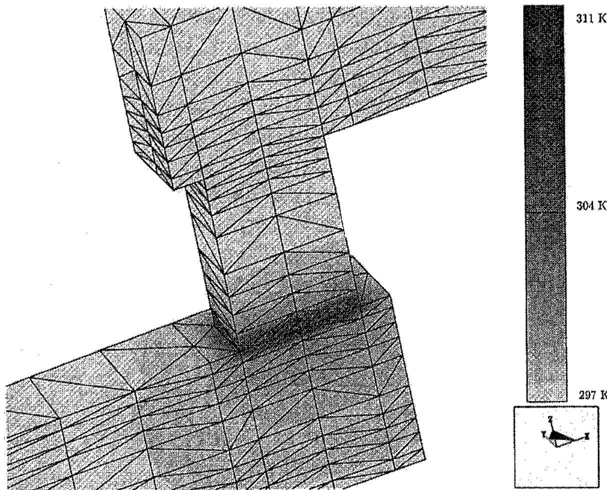

Fig. 3: Temperature profile of one half of the conductor structure after a current pulse of 34mA after 1ns.

voltage peak of 0.3V can be noticed on its output.

Conclusion

We have developed a finite element based simulation package for two- and three-dimensional resistance extraction, capacitance extraction, transient electric and coupled electro-thermal interconnect analysis. We have formulated models suitable for the majority of applications. The program has been tested with a large number of applications and is freely available (www.iue.tuwien.ac.at).

Acknowledgment

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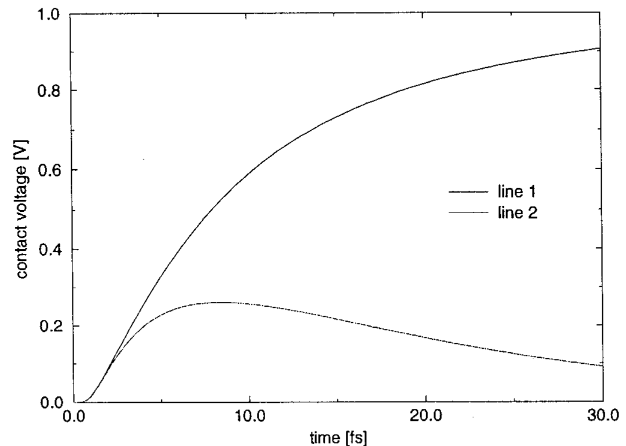

Fig. 4: Output voltages of the crosstalk experiment

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