Optimization of Pseudomorphic HEMT's Supported by Numerical Simulations

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***Abstract*— Measurements and simulations of three different pseudomorphic high electron mobility transistors (PHEMT's) are presented. The PHEMT's possess the same epitaxial structure but different geometrical properties. For the simulations, the generic device simulator MINIMOS-NT is employed. This simulator is not restricted to planar device surfaces but is able to model complex surface topologies including the effect of passivating dielectric layers. Mixed hydrodynamic and drift-diffusion simulations are demonstrated. They include the DC characteristics as well as the bias-dependent gate capacitances. Thus, bias-dependent current-gain cutoff frequencies f_T can be calculated. The results compare very well with the values obtained by small-signal parameter extractions from S-parameter measurements. Although a single consistent set of parameters is used for the simulations of all three devices, their characteristics are reproduced with an accuracy to our knowledge not reported before. Therefore, the DC and RF properties of PHEMT's with geometries significantly different from the measured devices can be reliably predicted.**

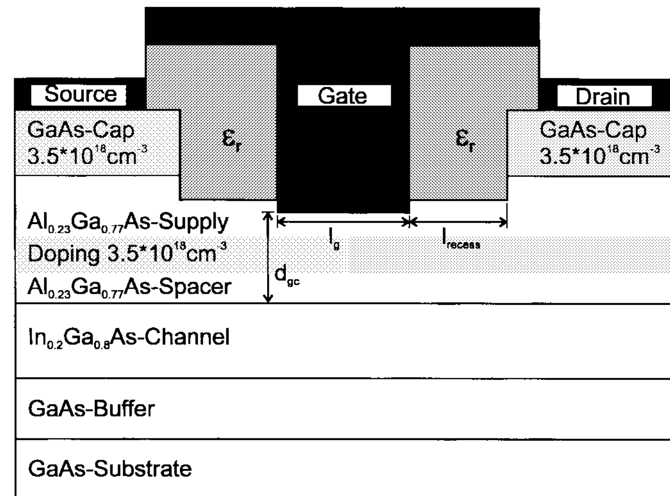

Fig. 1. Schematic cross section of the simulated HEMT's.

I. Introduction

PSEUDOMORPHIC high electron mobility transistors (PHEMT's) on Gallium-Arsenide (GaAs) substrate are now widely used for low noise and high power applications in the microwave and millimeter wave frequency ranges. Although still new record values of extrinsic transconductance $g_{m\,\mathrm{ext}}$ and current-gain cutoff frequency f_T are reported ($g_{m\,\mathrm{ext}} = 1070$ mS/mm and $f_T = 220$ GHz, for instance [1]), reliability and reproducibility of the process technology are becoming the key issues for the realization of cheap large-volume production. An optimized device design can reduce the technological effort, increase the yield, and, thus reduce the unit cost of the MMIC's. To achieve this optimum design, an exact device simulation can substantially support the technological development.

Today, most simulators are not able to simulate complicated heterostructure devices with an accuracy sufficient to still predict their performance even if the geometry is significantly changed [2]. This is because parameters of major models such as the electron transport or the electrical contact model to the channel [3] have to be fitted to the measurements individually for each device. In the literature, no simulations have been yet published which treat different devices with a single consistent set of parameters. However, this is a major requirement for reliable results.

Here, measurements and simulations of three PHEMT's for low-noise applications are presented. The devices differ with respect to their geometries but employ the same epitaxial structure. The program MINIMOS-NT used for the simulations has been described before [5]. In the present paper, the emphasis is on a detailed demonstration of optimization capabilities for HEMT's.

Details of the simulation are given in the next section. A description of the devices studied follows, and the expected impact of the different geometries on their properties is explained. After a discussion of the quality of the simulations, MINIMOS-NT is used to forecast the performances of devices not fabricated yet.

II. Simulation

The characteristics of a PHEMT are determined by the epitaxially grown structure and by the geometry defined by the manufacturing process. In PHEMT's, the electron channel is created by a semiconductor layer with narrow bandgap and high carrier mobility sandwiched between semiconductors with higher bandgaps. Fig. 1 shows a schematic view of the transistor investigated in this paper.

In the simulated devices, the source and drain contacts are placed on top of the cap layer, similar to the real device. To obtain an exact reproduction of the transfer characteristics, the channel must not be contacted by the source and drain

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TABLE I
PARAMETERS USED FOR SIMULATION

Energy relaxation time	0.3 ps
effective tunnel length	7 nm
insulator permittivity	7.0
interface charge density (insulator/semiconductor)	$2.3*10^{12}$ cm^{-2}

TABLE II
TRANSPORT PARAMETERS AND DOPING

	GaAs buffer/substrate	$Al_{0.23}Ga_{0.77}As$ supply GaAs cap	$In_{0.2}Ga_{0.8}As$ channel
μ_0 [cm^2/Vs]	3000	3000	6000
v_{sat} [10^7cm/s]	0.2	0.75	1.5
N_D[10^{18}cm^{-3}]	0.005	3.5	0.005

metals directly, as it has been the case in most published PHEMT simulations. Thus, all semiconductor interfaces that are crossed by the electrons between source and drain are realistically included in the calculations [3]. Abrupt interfaces are introduced by splitting the device into a number of different regions where different transport models and parameters can be applied. These regions are connected to each other by an interface model which describes the electron transport across the heterojunctions. Details of both bulk and interface models have been given earlier [5]. In the PHEMT channel, a hydrodynamic transport model is applied which includes the effects of velocity overshoot and real space transfer for the interface model. This model is essential for a realistic simulation of current saturation in the transfer characteristics [3] and geometry variations such as changes in gate length l_g and recess length $l_{\rm rec}$. In all regions outside the channel, a drift-diffusion model is applied. By this means, the computation time consuming hydrodynamic calculation is restricted to the most important region of the device [3]–[5]. In the simulations of the geometrically different PHEMT's, always the same set of parameters has been used. The most important of them are shown in Tables I and II. A more complete overview over the simulation parameters is given in [5].

III. PHEMT DEVICE STRUCTURE AND KEY PARAMETERS

The epitaxial structure common to all devices studied is shown in Fig. 1. From bottom to top the structure consists in a GaAs buffer on a S.I. GaAs substrate followed by a 12 nm $In_{0.2}Ga_{0.8}As$ channel layer, a 3 nm undoped $Al_{0.23}Ga_{0.77}As$ spacer layer, a 15 nm $Al_{0.23}Ga_{0.77}As$ layer with an active doping of 3.5×10^{18} cm^{-3} and a 7 nm undoped $Al_{0.23}Ga_{0.77}As$ Schottky barrier layer. The top layer is formed by a highly doped GaAs cap to facilitate the formation of the source and drain ohmic contacts. The different geometries of the three investigated PHEMT's A, B, and C are given in Table III.

Before presenting the results of the small-signal parameter extractions and the simulations, we will qualitatively discuss with simple arguments the differences that must be expected between the properties of devices A, B, and C.

One major figure of merit of a HEMT is its maximum transconductance $g_{m\,\max}$. Among the parameters given in

TABLE III
GEOMETRY PARAMETERS OF THE SIMULATED HEMT'S

	HEMT A	HEMT B	HEMT C
l_g [nm]	170	240	190
l_{rec} [nm]	135	135	60
d_{gc} [nm]	25	25	25 (23.3)

Table III, the most important one for $g_{m\,\max}$ is the gate-to-channel separation $d_{\rm gc}$. The critical technological step which determines the magnitude of $d_{\rm gc}$ is the gate recess. In the recess region, it is intended to remove the GaAs cap layer completely but to leave the AlGaAs Schottky barrier intact. In practice, this etching can only be performed with finite selectivity, and the effective recess depth can vary a few nanometers across the wafer or from one processing run to another. Therefore, small deviations in the order of 2 nm of the actual $d_{\rm gc}$ from the values given in Table III must be considered to be realistic. Deviations of the parameters l_g and $l_{\rm rec}$ from their nominal values in Table III are also technologically inevitable but do not have as large an influence on $g_{m\,\max}$ as $d_{\rm gc}$. The intrinsic $g_{m\,\max\,\rm int}$ (i.e., $g_{m\,\max}$ for vanishing source resistance R_S) of a PHEMT is given by [6]

$$g_{m\,\max\,\rm int} = \frac{q\mu n_{s0}}{l_g\sqrt{1+\left[\frac{q\mu n_{s0}(d_{\rm gc}+\Delta d_{\rm gc})}{\varepsilon v_{\rm sat} l_g}\right]^2}}. \qquad (1)$$

Here, ε, n_{s0}, μ, and $v_{\rm sat}$ are the permittivity of the semiconductor, equilibrium electron concentration, low field electron mobility, and saturation velocity in the channel, respectively, and $\Delta d_{\rm gc}$ is the distance between the channel/barrier heterointerface and the maximum of the electron probability distribution in the channel. Equation (1) demonstrates that $g_{m\,\max\,\rm int}$ is basically dependent on $d_{\rm gc}^{-1}$. This means that the effect of the same absolute variation of $d_{\rm gc}$ on $g_{m\,\max\,\rm int}$ increases for decreasing $d_{\rm gc}$.

Today, PHEMT's of interest have gate lengths below a quarter micrometer. For constant $l_g = 250$ nm, inspection of (1) reveals that $g_{m\,\max\,\rm int}$ is nearly independent of μ if μ is higher than 3000 cm^2/Vs which is usually the case in PHEMT's. On the other hand, (1) also states that $g_{m\,\max\,\rm int}$ depends only weakly on l_g for l_g below about 200 nm, and that it is reduced proportionally to l_g^{-1} in the range $l_g > 500$ nm. This establishes $d_{\rm gc}$ as the most important technological parameter for the transconductance of the PHEMT's investigated here.

Thus, only a small difference of $g_{m\,\max}$ must be expected between devices A and B of Table III, but a slightly higher value for device C due to a significantly shorter $l_{\rm rec}$ as R_S is reduced. The gate length variations are not likely to have a large impact on $g_{m\,\max}$ but will have other consequences. The short l_g of HEMT's A and C will lead to a small gate-source capacitance $C_{\rm GS}$ and, thus, to a higher f_T compared to HEMT B. However, further consequences of the parameter variations in Table III cannot be easily estimated quantitatively. Such consequences are the increase of the output conductance g_o (and the decrease of the voltage gain g_m/g_o) that is expected with a decrease of l_g or $l_{\rm rec}$. A small $l_{\rm rec}$ will cause a small R_S, but unfortunately, a large gate-drain capacitance $C_{\rm GD}$

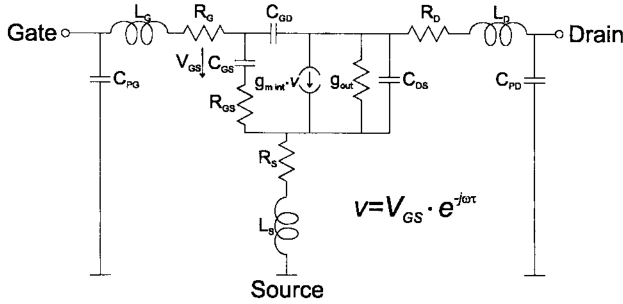

Fig. 2. Small-signal equivalent circuit used for parameter extraction.

undesirable for high f_T and high power-gain cutoff frequency $f_{\max}$. Numerical simulation is requested for the calculation of these effects.

IV. Small-Signal Parameter Extraction

S-parameter measurements were performed on HEMT A and B between 1 and 40 GHz. Contact pads and contacting microstrip lines are parasitic elements that are included in the measured results. The extraction of the intrinsic small-signal parameters $C_{\rm GS}$, $C_{\rm GD}$, and $g_{m\,\rm int}$ was performed for HEMT A according to [7], using the equivalent circuit shown in Fig. 2. This circuit takes the parasitic elements into account by introducing the capacitances $C_{\rm PG}$ and $C_{\rm PD}$ and the inductances L_G, L_S, and L_D. Thereby it is possible to separate the elements of the HEMT from the contacting network.

In the MINIMOS-NT simulations the total extrinsic gate capacitance C_G is determined by the quasistatic approximation

$$C_G(V_{\rm GS}, V_{\rm DS}) = \left.\frac{\partial Q_G(V_{\rm GS})}{\partial V_{\rm GS}}\right|_{V_{\rm DS}=\rm const} \quad (2)$$

with Q_G being the total charge on the gate metal surface at a given DC bias point.

V. Simulations and Measurements

All DC and RF measurements were performed on HEMT's with a gate width of $4 \times 40 = 160$ μm. First, the simulation of HEMT A was fitted to the measurements in the following way. For the low field mobility μ in the InGaAs channel, the value obtained from Hall measurements of an equivalent layer structure was adopted. The InGaAs saturation velocity $v_{\rm sat}$ was treated as a fitting parameter under the assumption that the velocity yielded by a HEMT delay time analysis is subject to an error of about 20% [8]. The actually used values of μ_0 and $v_{\rm sat}$ for InGaAs channel, AlGaAs supply, and GaAs substrate, buffer, and cap are listed in Table II. The saturation velocity assumed for GaAs is unrealistically low. This was deliberately chosen to compensate the overestimation of the buffer current which is a well known result of most simulations. As a physical reason, it is discussed that the carriers might be better confined to the channel due to quantization effects than assumed in the bulk model of the simulation [9]. However, the buffer current plays a minor role at the bias points of interest. Therefore, the method chosen to reduce the buffer current does not have a significant impact on the results of the simulation. Other main fitting parameters are $d_{\rm gc}$, the concentration of active dopant atoms and a constant interface charge density between the passivation and the semiconductor [10]. The data given in Table III lead to the best simultaneous fit to the DC measurements of threshold voltage V_T, drain current I_D and transconductance $g_{m\,\rm ext}$, and are well within their respective ranges of uncertainty.

A. Comparison of HEMT's A and B

Measured and simulated transfer characteristics of HEMT's A and B are shown in Fig. 3. Though the parameter fit procedure described above was only applied to HEMT A, also HEMT B is simulated precisely. Both measurements and simulations show that the drain current of HEMT A ($l_g =$ 170 nm) is larger than the current of HEMT B ($l_g = 240$ nm) by about 40 mA/mm. As can be seen in Fig. 4, also the maximum transconductance of HEMT A is superior to that of HEMT B by approximately 20 mS/mm, again measured as well as simulated. These results reflect the faster carrier transport due to the shorter gate of HEMT A. If the larger $g_{m\,\max\,\rm ext}$ of HEMT A would not be caused by accelerated transport but by a distance $d_{\rm gc}$ smaller than estimated in Table III, one would expect it to be correlated with a smaller I_D instead of a larger one. This comparison with experiment provides evidence that MINIMOS-NT is able to model $g_{m\,\rm ext}$ and I_D of both HEMT's in a consistent and realistic manner. However, there is also one small detail shown in Fig. 4 in which simulation and measurement do not agree completely: the gate-source voltage $V_{\rm GS}$ for which $g_{m\,\max\,\rm ext}$ is measured for HEMT B is slightly more negative than the simulated one. The reason for this behavior is not clear. As the two HEMT's were not fabricated in the same lot, small differences in the semiconductor passivation interface states could occur. On the other hand, the experimental observation that the transconductance of HEMT A decreases more rapidly with increasing positive $V_{\rm GS}$ than that of HEMT B is accurately reproduced by the simulation. The physical origin of this effect is the stronger real space transfer of electrons from the channel into the low-mobility barrier layer [3] in the device with the shorter gate (HEMT A). The increase of real space transfer in short channel devices is also leading to a higher output conductance. This will be discussed in Section VI.

Fig. 5 shows the simulated gate capacitances C_G of HEMT's A and B. For $V_{\rm GS}$ below pinchoff (i.e., $V_{\rm GS} < -0.9$ V), C_G consists of the gate-drain capacitance $C_{\rm GD}$ and parasitic contributions including the fringe capacitances. These values are very similar for both transistors. When $V_{\rm GS}$ increases, the longer gate of HEMT B manifests itself in a stronger increase ΔC_G compared to HEMT A. For HEMT B, $\Delta C_{\rm GB} \approx 520$ fF, and for HEMT A, $\Delta C_{\rm GA} \approx 350$ fF. The ratio $\Delta C_{\rm GB}/\Delta C_{\rm GA} \approx 520/350 \approx 1.48$ is close to the ratio of the gate lengths $l_{g\rm B}/l_{g\rm A} \approx 240/170 \approx 1.41$, as expected.

B. Comparison of HEMT's A and C

Initially, HEMT C was assumed to possess the same distance $d_{\rm gc} = 25$ nm as HEMT A but only a slightly longer $l_g = 190$ nm and a shorter $l_{\rm rec} = 60$ nm. When these values are used in the simulation, this results in a too negative

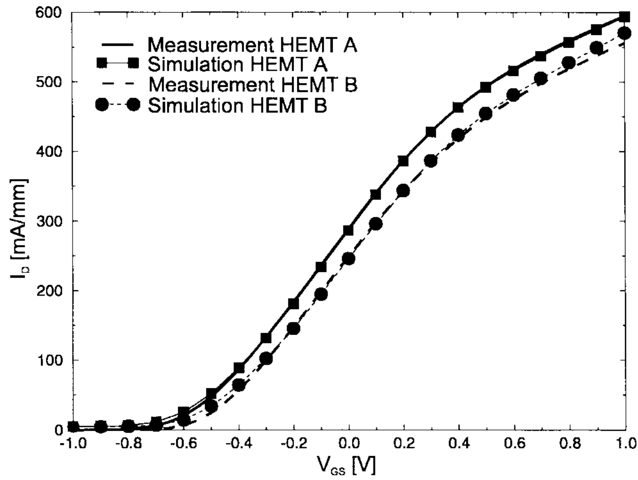

Fig. 3. Measured and simulated transfer characteristics of HEMT A and B at $V_{\rm DS} = 2.0$ V.

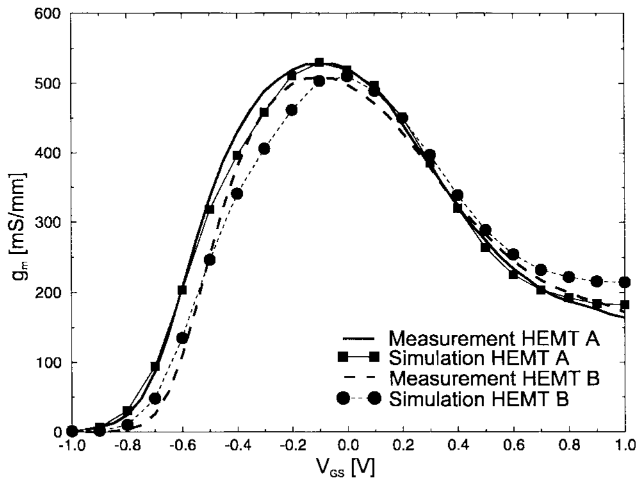

Fig. 4. Measured and simulated transconductance of HEMT A and B at $V_{\rm DS} = 2.0$ V.

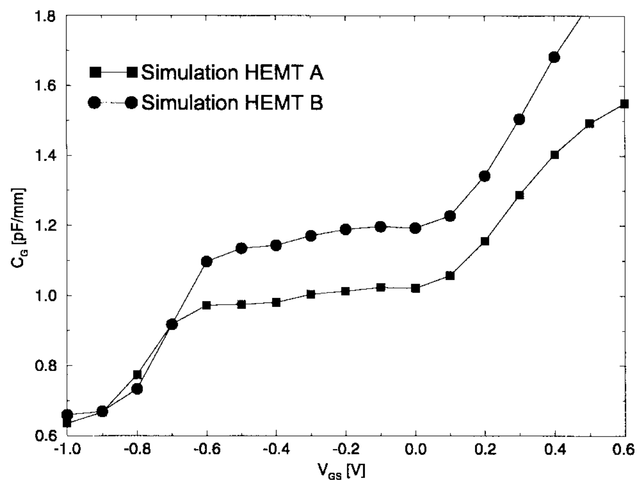

Fig. 5. Simulated C_G of HEMT's A and B at $V_{\rm DS} = 2.0$ V.

value of V_T and an overestimated I_D, as can be seen in Fig. 6. However, a reduction of $d_{\rm gc}$ by 1.7 nm leads to perfect coincidence of measured and simulated curves, as it is also shown in Fig. 6. Variations of $d_{\rm gc}$ of such small size

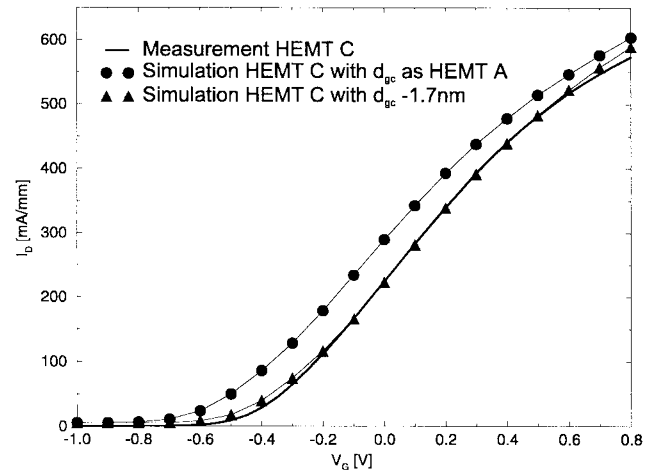

Fig. 6. Measured (bold line without symbols) and simulated transfer characteristics of HEMT C with the nominal $d_{\rm gc}$ (circles) and $d_{\rm gc} - 1.7$ nm (triangles) at $V_{\rm DS} = 2.0$ V.

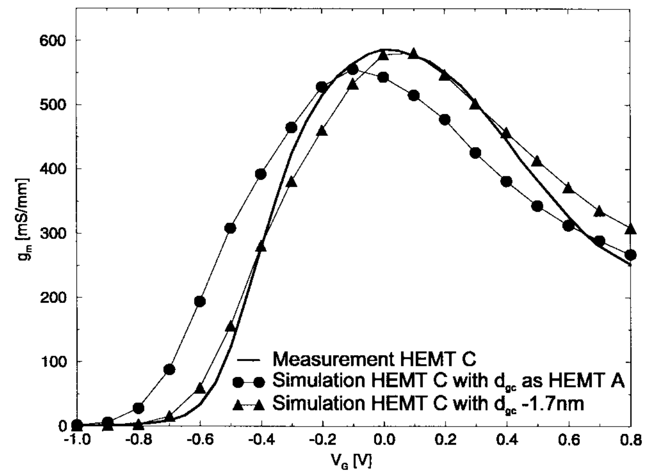

Fig. 7. Measured (bold line without symbols) and simulated transconductance of HEMT C with the nominal $d_{\rm gc}$ (circles) and $d_{\rm gc} - 1.7$ nm (triangles) at $V_{\rm DS} = 2.0$ V.

can easily occur in different technology runs. The agreement between measurement and simulation is even more evident for the transconductance shown in Fig. 7. Both the peak value $g_{m\ \rm max\ ext} = 580$ mS/mm and its occurrence at $V_{\rm GS} = 0$ V are simulated very well.

We now return to the initial simulation of HEMT C which was performed under the assumption that $d_{\rm gc}$ is equal to the value of HEMT A ($d_{\rm gc} = 25$ nm). When this simulation of a "hypothetical" HEMT C (circles in Fig. 7) is compared to the simulation of HEMT A in Fig. 4, it is found that the hypothetical device has a $g_{m\ \rm max\ ext}$ that is about 25 mS/mm larger than the value of HEMT A though its gate is 20 nm longer. This must be a consequence of $l_{\rm rec}$ which is 75 nm shorter and obviously overcompensates the small effect of the slightly longer gate. From the previous comparison between HEMT's A and B (which share the same $l_{\rm rec}$), we can estimate that an l_g increase of 20 nm only causes a negligible $g_{m\ \rm max\ ext}$ decrease of about 5 mS/mm. This independently confirms the conclusion drawn above: the reduction of $l_{\rm rec}$ had a stronger impact on the transconductance of HEMT C than the slightly longer l_g.

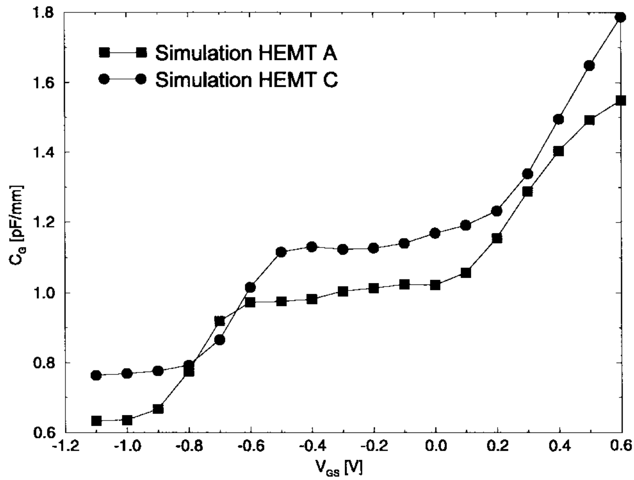

Fig. 8. Simulated C_G of HEMT A (squares) and HEMT C (circles) at $V_{\rm DS} = 2.0$ V.

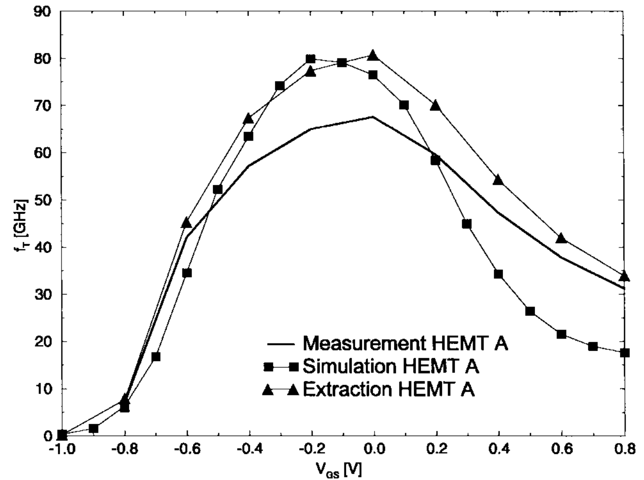

Fig. 9. Measured (bold line without symbols) and calculated f_T with simulated (squares) and extracted (triangles) C_G and g_m at $V_{\rm DS} = 2.0$ V.

A drawback of the shrinkage of $l_{\rm rec}$ is the increase of C_G. This can be seen in Fig. 8 which shows the simulated gate capacitance C_G of HEMT's A and C. For HEMT C, the whole function $C_G(V_{\rm GS})$ is shifted toward higher values by about 130 fF/mm as compared to HEMT A. As the shift is already completely present in the pinchoff region it can be entirely attributed to the increased coupling between the gate and drain contacts.

VI. Device Optimization

An important figure of merit of a HEMT is the current-gain cutoff frequency f_T approximately given by

$$f_T \approx \frac{g_m}{2\pi C}. \tag{3}$$

For the case of HEMT A, Fig. 9 shows a comparison of the functions f_T ($V_{\rm GS}$) determined in three different ways:

1) measured (i.e., obtained by S-parameter measurements);
2) calculated with (3) where $g_m = g_{m\,\rm int}$ and $C = C_{\rm GS} + C_{\rm GD}$ were obtained from extractions using the small-signal equivalent network shown in Fig. 2;
3) obtained from simulations also using (3) with $g_m = g_{m\,\rm ext}$ and $C = C_G$.

The last two cases offer the possibility to determine the device performances excluding the contacting network which is necessary for circuit design. As shown, the f_T calculated from extracted and simulated data agree reasonably well especially with respect to their maxima. The measured value is about 13 GHz lower than the calculated ones mainly due to the presence of the parasitic elements indicated in Fig. 2. The values of the small-signal circuit elements for HEMT A which are considered to be not bias dependent are given in Table IV.

In the following we want to examine the influence of the geometrical parameters l_g and $l_{\rm rec}$ on the magnitude of f_T simulated according to (3). The capacitance C_G entering the equation is greatly influenced not only by l_g and $l_{\rm rec}$, but also by the shape of the gate metal cross section (imagine, for instance, the case of a T-gate) and the dielectric constant ε_r of the passivation material that fills the space between

TABLE IV
Parasitic Small-Signal Parameters From Parameter Extraction of HEMT A with a Gate Width of 160 μm

C_{PD}=C_{PG} [fF]	22
L_G [pH]	16.5
L_D [pH]	13.1
L_S [pH]	3.0
R_G [Ω]	1.4
R_D [Ω]	3.4
R_S [Ω]	2.3

metal structure and semiconductor surface. Our simulator is able to take all these effects of surface topology fully into account. On the other hand, only in simulation it is possible to analyze the hypothetical case that the gate does not interact capacitively with the surrounding semiconductor surfaces or with the neighboring ohmic contacts, i.e., a non passivated device with an infinitesimally thin gate metal but negligible gate resistance. This can be achieved by choosing $\varepsilon_r = 0$ and leads to the determination of the theoretical maximum of f_T for given l_g and $l_{\rm rec}$.

A. Reduction of the Gate Length

When l_g is reduced, f_T will increase, but a simultaneous and undesirable increase of the output conductance g_o must be expected. In Fig. 10 the simulated parameter g_o (at the bias point $V_{\rm DS} = 2$ V, $V_{\rm GS} = 0$ V) is shown as a function of l_g and compared to the experimental DC values of HEMT's A and B which differ only with respect to l_g but not in any other geometrical dimensions. The simulation is able to reproduce g_o realistically.

As described in Section III, the increase of $g_{m\,\rm ext}$ is only small when l_g is reduced. The capacitance $C_{\rm GD}$ is nearly independent of l_g. The gate-source capacitance $C_{\rm GS}$ is only partly dependent on l_g: fringe and other parasitic contributions are independent of l_g, only the part due to the gate contact area is length dependent. Therefore, the improvement of f_T which can be achieved by a reduction of l_g, depends on the

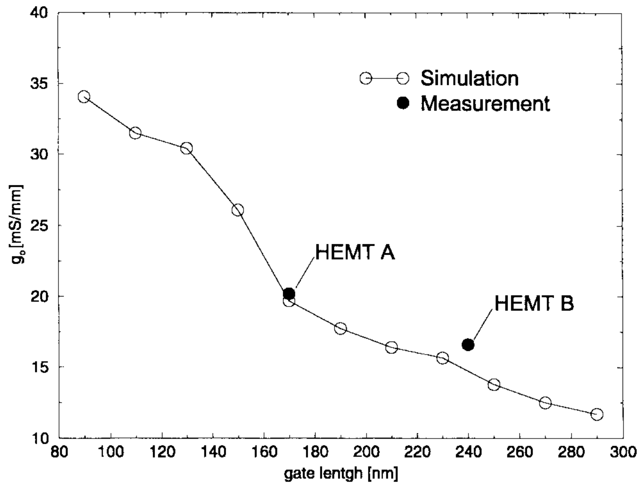

Fig. 10. Measured (filled symbols) and simulated (open symbols) output conductance g_o versus the gate length at the bias point $V_{\mathrm{GS}} = 0.2$ V and $V_{\mathrm{DS}} = 2.0$ V.

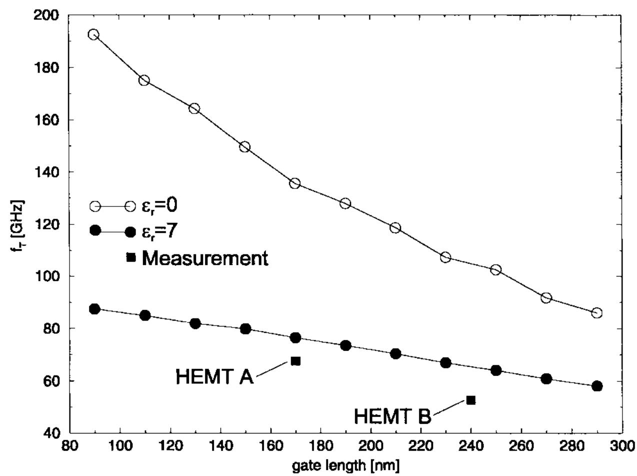

Fig. 11. Measured (filled squares) and simulated f_T versus l_g for a passivated HEMT with $\varepsilon_r = 7$ (filled circles) and $\varepsilon_r = 0$ (open circles) at $V_{\mathrm{GS}} = 0.2$ V and $V_{\mathrm{DS}} = 2.0$ V.

relative contribution of the parasitic (i.e., constant) part of the capacitance to the gate capacitance C_G. The dependence of f_T on l_g is shown in Fig. 11 for two examples: the limiting case of $\varepsilon_r = 0$ where the contribution of parasitics is reduced to the inevitable fringe capacitances at the gate edge, and the case of the presence of a medium with $\varepsilon_r = 7$ (a silicon nitride passivation layer, for instance) which fills the space between the T-gate overhang and the semiconductor surface in the manner sketched in Fig. 1. The measured values in Fig. 11 (which are taken from HEMT's A and B) are even below the ones calculated with complete T-gate structure and passivation nitride due to the presence of parasitic pad capacitances as discussed before.

Fig. 11 demonstrates clearly that the improvement of f_T achieved by a reduction of l_g depends strongly on the relative contribution of parasitic capacitive couplings to the total gate capacitance. The reduction of f_T in the presence of passivation layers has been experimentally observed for instance by Wu *et al.* [11]. To obtain an f_T of 100 GHz, a fully passivated

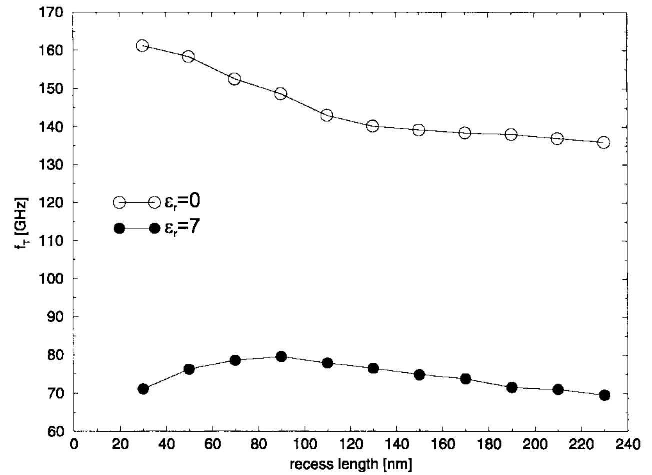

Fig. 12. Simulated f_T versus l_{recess} for a passivated HEMT with $\varepsilon_r = 7$ (filled symbols) and $\varepsilon_r = 0$ (open symbols) at $V_{\mathrm{GS}} = 0.2$ V and $V_{\mathrm{DS}} = 2.0$ V.

device of the general structure of HEMT A must be either supplied with a gate length below 100 nm, or the gate length is left as large as in HEMT B (240 nm) but no passivation is allowed at all. The case of an unpassivated device in air with $\varepsilon_r = 1$ is close to the idealized case $\varepsilon_r = 0$ plotted in Fig. 11. The two curves in Fig. 11 are calculated under the assumption of a constant interface charge density which is certainly an idealization when the unpassivated case is considered.

B. Reduction of the Recess Length

As demonstrated in Section V, $g_{m\,\mathrm{ext}}$ is increased when l_{rec} is reduced. The reason is a decrease of the ohmic resistance in the current path. Therefore, $g_{m\,\mathrm{ext}}$ is expected to depend roughly linearly on l_{rec}. We have found that the dependence of C_G on l_{rec} can be modeled by

$$C_G \propto C_{\mathrm{GS}} + \alpha + \frac{\beta}{l_{\mathrm{recess}}} \tag{4}$$

where α and β are constants. The simulated dependence of f_T on l_{rec} is plotted in Fig. 12. In the hypothetical situation $\varepsilon_r = 0$, there is almost no dependence of C_G on l_{rec}, and f_T increases monotonously with decreasing l_{rec} due to the improvement of $g_{m\,\mathrm{ext}}$. For the case that the gate and the adjacent device surfaces are encapsulated by a dielectric with $\varepsilon_r = 7$, the decrease of f_T on the left hand side of the maximum at $l_{\mathrm{rec}} \approx 90$ nm is caused by the rapidly increasing C_G. If a device passivation with a dielectric constant $\varepsilon_r < 7$ would be available, it is evident that f_T would be higher for any $\varepsilon_r < 7$ and the optimum of l_{rec} would be shifted toward smaller values.

VII. Conclusion

Simulations and measurements of three PHEMT's with the same epitaxial structure but different geometries are presented. The results of the simulation were fitted to experimental results obtained from one of the three devices by adjustment of the most important simulation parameters well within realistic ranges. With the same set of parameters, the remaining two

devices were also simulated. The calculated and measured DC characteristics of all three devices agree extremely well. For instance, this enables us to trace differences of the gate recess depths of the investigated HEMT's with an accuracy in the range of 1 nm. The calculated bias dependent current-gain cutoff frequency also agrees well with the values obtained from small-signal parameter extractions. This capability to model different HEMT's realistically is the basis for substantial predictions on the effect of geometrical variations that go beyond the ones already realized experimentally. These predictions include DC as well as RF properties. This qualifies simulation as a valuable tool for device optimization which can significantly reduce the number of technological runs inevitable for this purpose.

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