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Drive performance of an asymmetric MOSFET structure: the peak device

M. Stockinger[a,*], A. Wild[b], S. Selberherr[c]

[a]Institute for Microelectronics, TU Vienna, Gusshausstr. 27–29/E360, A-1040 Vienna, Austria
[b]Motorola, Tempe, AZ 85284, USA
[c]Institute for Microelectronics, TU Vienna, Gusshausstr. 27–29/E360, A-1040 Vienna, Austria

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Abstract

The drive performance of a new MOSFET structure, the peak device, resulting from recent doping profile optimizations of a 0.25 μm n-MOSFET for 1.5 V supply voltage, is investigated. Explanations for the improved performance are given using two-dimensional device simulation. With an analytical transistor model fitted to the two-dimensional device characteristics, the relevant physical effects are identified. It is shown that the superior drive performance of the peak device can mainly be addressed to the reduction of the effective gate length and the improved bulk effect. © 1999 Elsevier Science Ltd. All rights reserved.

1. Introduction

Recent channel doping profile optimizations of a 0.25 μm n-MOSFET for 1.5 V supply voltage showed that a narrow acceptor doping peak near the source, as shown in Fig. 1, offers superior drive performance with low drain-source leakage [1].

To achieve this result, a self-contained simulation-based optimization process was performed on the two-dimensional channel doping region. While the drive current (I_D for $V_G = V_D = V_{DD}$) was maximized, the leakage current (I_D for $V_G = 0$, $V_D = V_{DD}$) was kept below 1 pA. A sensitivity analysis was carried out on the resulting doping profile to find the relevant region. The doping in this region was substituted by an analytical implant with Gaussian shape, and a second optimization process was performed on the implant parameters.

The drive current was improved by 48% compared to a uniformly-doped device (UDD) delivering the same leakage current. A similar device structure, designated FIBMOS, was recently demonstrated experimentally in Ref. [2]. It also showed significant improvements in other device characteristics, e.g. output resistance, hot-electron degradation, punchthrough resistance and threshold stability.

In this work we give explanations for the superior drive performance of the peak device. We found out that the doping peak divides the device into two equivalent transistors where the higher doped one determines the overall performance. We discuss the optimized parameter values of the peak implant starting with a general investigation on the effects of gate length reduction. We show the connection between the vertical doping peak parameters and the subthreshold characteristics. Finally, an explanation for the lateral peak position is given using a three-transistor equivalent model.

2. Reducing gate length

The drain current of a MOSFET depends on its gate length in several ways. Considering a first order approximation, the current is inversely proportional to the gate length. Second order effects include velocity saturation, drain-induced barrier lowering (DIBL), and channel length reduction.

For drive current optimization under constant leakage current, gate length reduction is a possible choice. This becomes obvious when the drain current expressions for weak and strong inversion are taken into account. For weak inversion, the drain current depends exponentially on the threshold voltage, whereas for strong inversion the dependence is quadratic and becomes linear for short devices due to velocity saturation.

When gate length is reduced, both leakage and drive current will rise. Therefore, the threshold voltage has to be increased to keep the leakage current unchanged, and the drive current will rise because of its smaller threshold voltage dependence. However, there is a lower limit for the gate length where no further drive current improvements can be achieved because DIBL becomes significant.

* Corresponding author.
E-mail address: stockinger@iue.tuwien.ac.at (M. Stockinger).

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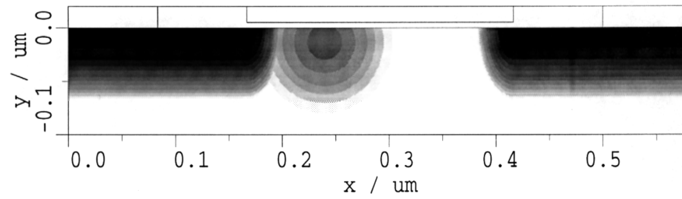

Fig. 1. The peak device resulting from two-dimensional optimization.

Fig. 2 shows the drive current versus gate length of a UDD with 5 nm oxide thickness and 1 pA/μm leakage current for 1.5 V supply voltage. Data were extracted in three ways: using two-dimensional device simulation with MINIMOS-NT [3]; a drain current model with DIBL (see Appendix); and the same model without DIBL. Threshold voltage adjustment was done by substrate-doping variation to keep the leakage current constant. The drain current model includes the following second order effects: DIBL (optionally), velocity saturation, and mobility reduction due to impurity scattering.

These results give an explanation for the superior drive performance of the peak device: the effective transistor is restricted to a short region near the source. The rest of the channel region works like a depletion-type cascode transistor which only sets the drain voltage of the effective transistor and does not influence its performance for the saturated case. Therefore, the advantages of a short transistor, as discussed above, also take effect on the peak device, even if the gate length of this device is large.

3. Improving subthreshold swing

When the gate oxide of a MOSFET becomes thinner, raising the substrate doping is necessary to keep the threshold voltage at a reasonably high level. As a result, the subthreshold swing will get worse due to the increased bulk effect. This can be omitted by lower substrate doping together with a doping layer near the surface to set the threshold voltage. The bulk depletion layer will then be deeper which decreases the subthreshold swing. The maximum doping should not be placed at the surface, because this would decrease the carrier mobility due to impurity scattering.

The optimized peak device structure shows similar properties: the doping peak has a finite depth and its maximum is slightly below the surface (see Fig. 1). Fig. 3 demonstrates the deterioration of the subthreshold swing for a peak device with infinite peak depth compared to the original device. (In practical cases, infinite means: down to the bulk bottom.) The subthreshold swings are 87 mV/dec and 74 mV/dec, respectively.

4. Lateral peak position

At first glance, the advantage of placing the doping peak close to the source may not be obvious. To investigate how the performance changes with the peak position, a three-transistor model was compared to results obtained from two-dimensional device simulation. A long peak device with 1 μm gate length was used to illustrate the effect of the peak position more clearly. Fig. 4 shows the device structure together with the three-transistor model. Transistor M2 has a fixed gate length and is equivalent to the doping

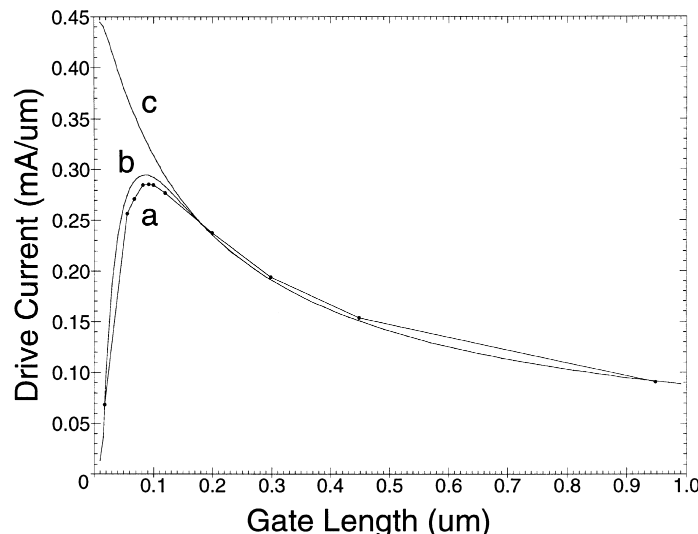

Fig. 2. Drive current versus gate length for a UDD. (a) Two-dimensional device simulation. (b) Model with DIBL. (c) Model without DIBL.

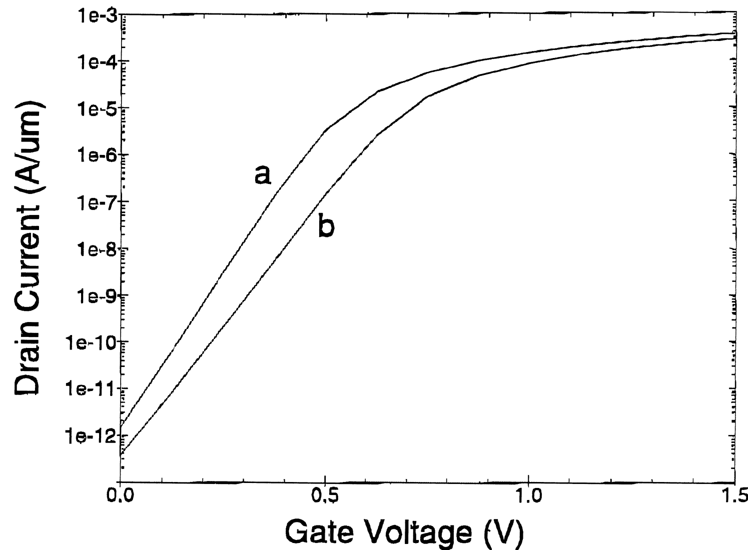

Fig. 3. Subthreshold characteristics of the peak device. (a) Finite. (b) Infinite peak depth.

peak, M1 and M3 represent the lightly-doped regions. Their lengths can be adjusted to track the variable peak position.

The peak position was varied from the source to the drain side, and the drive and leakage currents were simulated with MINIMOS-NT. The three-transistor model was calculated using a drain current model with DIBL (see Appendix). The model parameters were chosen to fit the results from the two-dimensional device simulations.

A good correlation of the tendency can be observed, even though the exact values differ, as depicted in Fig. 5. When the doping peak comes close to source or drain, its doping is more and more neutralized by the high donor doping, and the drain current rises because of the reduced threshold voltage. This effect is not covered by the three-transistor model.

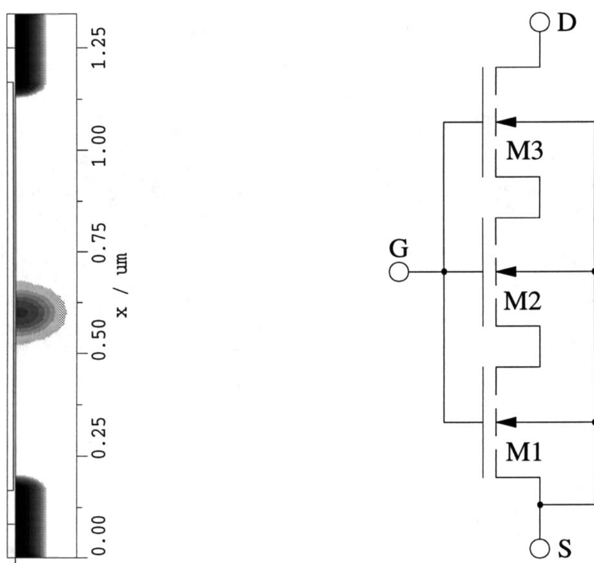

Fig. 4. A long peak-device structure and its three-transistor equivalent model.

While the leakage current remains rather constant, the drive current decreases as the doping peak moves towards the drain. The reason can be found in transistor M1 which works in the ohmic region and, therefore, as a series resistance to M2. When the source voltage of M2 rises due to the voltage loss over M1, the drive current decreases as the gate-source voltage of M2 becomes smaller. For the leakage current case, this effect cannot be observed because the drain current is too small to produce a significant voltage drop.

5. Conclusion

We investigated the superior drive performance of a peak device we obtained from two-dimensional channel profile optimization. We discovered a lower limit for the gate length of a UDD where no further improvements of the drive current can be achieved when leakage is kept constant. The effects of the vertical geometry parameters of the doping peak were shown. We also presented a three-transistor equivalent model to investigate device performance under changing lateral peak position, and found that the best position is close to the source.

The latest investigations proved that the same drive performance can be maintained if the region between the source and the doping peak is filled with acceptors, which is especially important considering manufacturability. For such a device with the peak implant extended into the source well, the doping could be brought in through the source window using common tilt-implant techniques.

Further performance improvements can be achieved by an even lower substrate-doping level. In this case, additional precautions have to be taken against punchthrough, e.g. a separate acceptor-doping implantation under the source well, or, simpler, a halo implant.

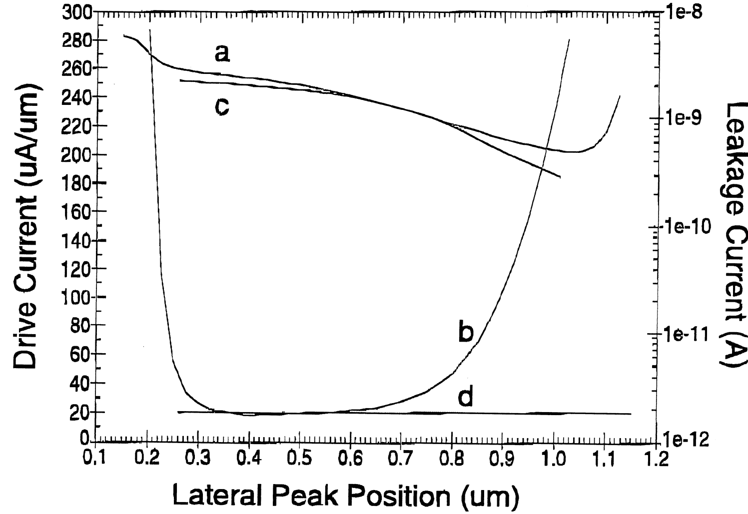

Fig. 5. Variation of the lateral doping peak position. (a), (b) Drive and leakage current from two-dimensional device simulation. (c), (d) Using the three-transistor model.

Appendix

The formulae to derive the drain current for the simple analytical model used in this work are listed below in a sequence suitable for computation purposes. Eqs. (A2)–(A7) are well-known formulae which are also used in common SPICE models [4]. Eq. (A10) and Eq. (A12) are, with some minor modifications, taken from Ref. [5]. All used constants and parameters are listed in Table A1.

The electron mobility is calculated using the ionized impurity scattering model by Scharfetter and Gummel [6]:

$$\mu = \frac{\mu_0}{\sqrt{1 + \frac{N_{\mathrm{sub}}}{3 \times 10^{16}\ \mathrm{cm}^{-3} + \frac{N_{\mathrm{sub}}}{350}}}} \tag{A1}$$

Table A1
Constants and parameters

Constants	
ϵ_{ox}	Permittivity constant in the oxide
ϵ_{si}	Permittivity constant in silicon
U_{t}	Temperature voltage
q	Electron charge
Parameters	
μ_0	Zero field, zero substrate-doping electron-mobility
N_{sub}	Substrate acceptor doping
t_{ox}	Gate oxide thickness
n_{i}	Intrinsic carrier concentration in the substrate
V_{contact}	Gate contact potential
v_{sat}	Electron saturation velocity
F_{DIBL}	DIBL factor (is set to 0 if DIBL is disabled)
E_{DIBL}	DIBL exponent
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage

The transconductance parameter is defined as

$$KP = \mu \frac{\epsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}} \tag{A2}$$

and ϕ, which has the value of twice the bulk Fermi potential, reads:

$$\phi = 2U_{\mathrm{t}} \ln \frac{N_{\mathrm{sub}}}{n_{\mathrm{i}}} \tag{A3}$$

The body effect parameter is calculated by

$$\gamma = \frac{t_{\mathrm{ox}}}{\epsilon_{\mathrm{ox}}} \sqrt{2q\epsilon_{\mathrm{si}} N_{\mathrm{sub}}} \tag{A4}$$

and the threshold voltage for zero drain source voltage by

$$V_{\mathrm{th,0}} = V_{\mathrm{contact}} + \frac{\phi}{2} + \gamma\sqrt{\phi} \tag{A5}$$

The bulk depletion width reads:

$$x_{\mathrm{dep}} = \sqrt{\frac{2\epsilon_{\mathrm{si}}\phi}{qN_{\mathrm{sub}}}} \tag{A6}$$

and the critical field for carrier velocity saturation is calculated by

$$E_{\mathrm{c}} = \frac{2v_{\mathrm{sat}}}{\mu} \tag{A7}$$

To include the DIBL effect, a DIBL-characteristic length is introduced

$$L_{\mathrm{DIBL}} = \sqrt{\frac{\epsilon_{\mathrm{si}}}{\epsilon_{\mathrm{ox}}} x_{\mathrm{dep}} t_{\mathrm{ox}}} \tag{A8}$$

and the effective threshold voltage is calculated by a formula similar to that used in the BSIM3v3 model [7]:

$$V_{\mathrm{th}} = V_{\mathrm{th,0}} - F_{\mathrm{DIBL}} V_{\mathrm{DS}} \left(\mathrm{e}^{\frac{-E_{\mathrm{DIBL}} L}{2L_{\mathrm{DIBL}}}} + 2\mathrm{e}^{\frac{-E_{\mathrm{DIBL}} L}{L_{\mathrm{DIBL}}}} \right) \tag{A9}$$

The slope factor is

$$n = \left(1 - \frac{\gamma}{2\sqrt{V_{GS} - V_{th} + (\gamma/2 + \sqrt{\phi})^2}}\right)^{-1} \quad \text{(A10)}$$

and a velocity saturation factor is introduced using the Heavyside function σ [8]:

$$F_{sat} = \left(1 + \frac{V_{GS} - V_{th}}{nE_c L}\right)^{-1} \sigma(V_{GS} - V_{th}) \quad \text{(A11)}$$

Finally, the drain current is calculated by

$$I_D = 2n \frac{W}{L} KPU_t^2 \ln^2\left(1 + e^{\frac{V_{GS} - V_{th}}{2nU_t}}\right) F_{sat} \quad \text{(A12)}$$

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