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An interpolation based MOSFET model for low-voltage applications

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Abstract

The development towards lower voltages and even ultra-low power (ULP) technologies [J.B. Burr, Symposium Record, Hot Chips V, 1993, pp. 7.4.1–7.4.12; D. Liu, Ch. Svensson, IEEE J. Solid State Circuits 28(1)(1993) 10–17; G. Schrom et al., 24th European Solid State Device Research Conference—ESSDERC'94, 1994, pp. 679–682] makes ever higher demands on compact device model accuracy. We present a new approach to dynamic MOSFET modeling, which is especially suited for the simulation of low-voltage mixed analog digital circuits. The model is based on the interpolation of terminal charges and conductive currents which are determined from transient current/voltage data which can be obtained through measurement or simulation of the devices. Using this model, a variety of analog and digital circuits was simulated, and selected results were verified against device-level circuit simulations. © 1998 Elsevier Science Ltd. All rights reserved.

1. Introduction

The concept of ultra-low power CMOS technology involves a substantial reduction of the supply and threshold voltages to reduce the power dissipation [11,13,14]. Parallel architectures are used to compensate for the speed reduction of individual gates, keeping up the overall systems performance. Going to very small voltages (well below 1 V), technology evaluation and optimization cannot just rely on traditional device parameters, but must be done at least on the circuit level. This requires very accurate device models for circuit simulation.

As a consequence of the low supply and threshold voltages, ULP devices operate in the transition region between weak and strong inversion, i.e. moderate inversion, which becomes predominant for the device behavior. Unfortunately though, this is a major weak point in most existing compact models. Similar problems arise when future VLSI technologies are to be investigated and the existing compact models are not yet refined to cover all relevant effects accurately.

The interpolation of terminal currents seems attractive, but very often the accuracy in the weak-inversion regime is insufficient. Early work in this field of so-called table look-up MOSFET modeling started with timing simulation [1,2], extending to general circuit simulation [3–5] and special techniques for scalability and data compression [6,7]. While these models serve well for strong inversion, no methods were given to handle the moderate and weak-inversion regime with high accuracy, and capacitance modeling is essentially restricted to analytical models.

In this work, we follow a new approach based on a special interpolation of terminal currents and charges with physically motivated functions, i.e. piecewise polynomial and/or exponential splines. This method ensures that various physical effects are accounted for implicitly. Using a simple transient method for device characterization, the input data for the model can be obtained from measurements or simulations without any a priori knowledge and parameter fitting. The primary aim of the model is to render the behavior of a given device in a direct way to a circuit simulator to obtain accurate circuit performance data, which can then be related to process parameters. Consequently, physical interpretability is abandoned in favor of accuracy and generality of the model.

2. Transient device characterization

The input data to the model, i.e. terminal currents and charges for a set of terminal voltages, can be obtained either by measurements or process and device simulations. In this work we used VISTA with MINIMOS [8] to obtain the device data by simulation. All conductive currents can be obtained directly from DC measurements. The charge data are computed from transient simulations, as shown in Fig. 1 for the case of a two-pole: the device is modeled as a quasi static black box which is equivalent to a non-linear conductance parallel to a non-linear capacitance $C(v) = dq/dv$. Applying a symmetrical trapezoidal voltage $v(t)$ to the

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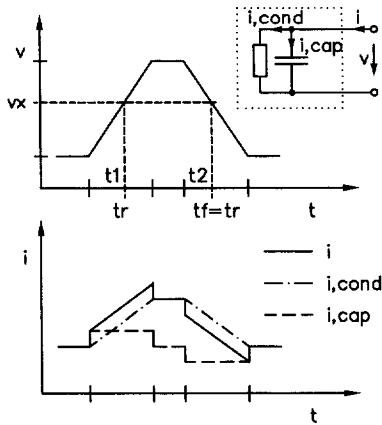

Fig. 1. Quasi-static black-box model of a two-pole: separation of capacitive and conductive currents

device will result in a current $i(t)$ which can be separated into a conductive and capacitive component,

$$i_{\mathrm{cond}}(v) = 1/2[i(t_1(v)) + i(t_2(v))]; \tag{1}$$

$$i_{\mathrm{cap}}(v) = 1/2[i(t_1(v)) - i(t_2(v))]$$

which is related to the charge by $i_{\mathrm{cap}}(v) = \mathrm{d}q/\mathrm{d}t = (\mathrm{d}q/\mathrm{d}v).(\mathrm{d}v/\mathrm{d}t)$. Thus, the charge can be determined as

$$q(v) = q_0 + \int_{v}^{2v_0} i_{\mathrm{cap}}(u)\mathrm{d}u \tag{2}$$

The charge offset q_0 can be determined from $q(0) = 0$. In the case of the MOSFET, we have a three-pole (assuming the source always grounded), one of the other terminals is ramped, and the currents at all terminals (including the ramped) are measured and subsequently converted to i/q-data.

To obtain a complete field of charge data, including the charge offset, a series of transient measurements/simulations is required, as shown in Fig. 2. According to the desired ranges and step sizes of V_{BS}, V_{GS} and V_{DS}, one transient in the 'V_{B}-direction', n transients in the 'V_{G}-direction', and $n \times m$ transients in the 'V_{D}-direction' are measured or simulated. The simulations in the 'V_{D}-direction' yield the main data set which is used for i/q extraction. The simulations in the 'V_{B}-direction' and 'V_{G}-direction' are required for the charge offset

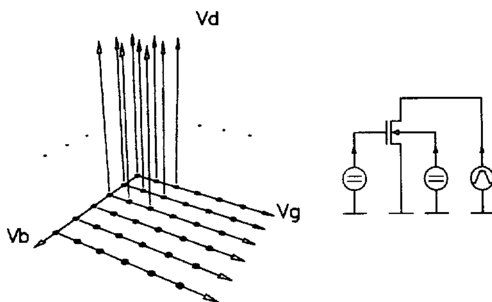

Fig. 2. Transient MOSFET simulations/measurements

computation. The steepness of the ramp determines the accuracy of the charge data and the influence of non-stationary effects accordingly. Both can be verified with single transient measurements, using the i/q-extraction software. For the simulation with MINIMOS, the input decks are generated automatically according to the range settings which also control the computation of the current/charge data. Fig. 3 shows a comparison with gate capacitance data obtained from accurate gate charge simulations using MINIMOS. Typically, the number of required simulations is $1 + n + nm = 1 + 5 + 5 \times 20 \sim O(100)$ with one simulation taking several minutes. The task can be run in parallel [8] so that characterization of one device requires less than 1 h.

3. Model function and simulation environment

The model function is based on a physically motivated interpolation of the terminal currents and charges of the device. The interpolation also supplies the derivatives, i.e. the conductance and capacitance matrices of the device. These data are directly interfaced to a new circuit simulator, MINISIM [9], which uses charge conservative capacitance modeling.

This approach rules out common problems, e.g. discrepancies between the AC-model conductance parameters and the derivatives of the DC-model currents.

The interpolation uses piecewise polynomial and/or exponential splines in each dimension (e.g. V_{B}, V_{D}: polynomial; V_{G}: exponential) to account for the physical nature of the quantities (especially the exponential dependence of the currents). The interpolation functions have the following form:

$$x < 0 : f(x) = g(x) \tag{3}$$

$$0 \le x \le 1 : f(x) = (1 - x).g(x) + x.h(x)$$

$$x > 1 : f(x) = h(x)$$

where the interval [0, 1] is the transformed target interval.

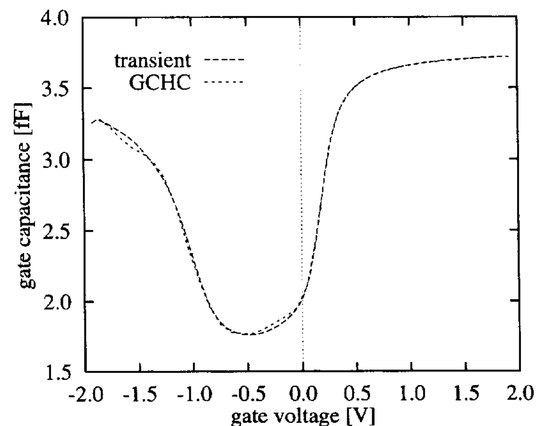

Fig. 3. Gate capacitance of an ULP n-channel MOSFET ($V_{\mathrm{BS}} = 0$ V) determined with the transient method ($t_{\mathrm{r}} = 3$ ns) and computed through accurate gate charge integration using MINIMOS's 'GCHC' option

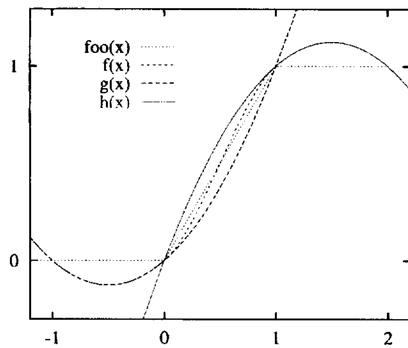

Fig. 4. Construction of the interpolation function $f(x)$ from the functions $g(x)$ and $h(x)$ to interpolate the function $foo(x)$ in the interval [0, 1]

The functions g and h depend on the type of the interpolation (cf. also Fig. 4):

$$\text{polynomial}: \; g(x)=a_0+a_1x+a_2x^2, \; h(x): \text{ dto} \tag{4}$$

$$\text{exponential}: \; g(x)=a_0+a_1.\mathrm{e}^{a_2x}, \; h(x): \text{ dto}$$

This ensures a continuous derivative, which is essential for simulator convergency. The exponential splines exhibit excellent extrapolation properties in the subthreshold region.

To determine the accuracy of the model, equation (5) was used as a test function (cf. the EKV model [10]). The worst-case interpolation error, i.e. the L_∞ norm of the relative error, was determined numerically as a function of the gate voltage (cf. Fig. 5). The modified exponential interpolation is clearly better than the cubic one, yielding an error of $< 0.2\%$ for the function value and $< 2.0\%$ for the derivative.

$$I_D=I_s\ln^2\left(1+\mathrm{e}^{\frac{V_{GS}-V_T}{2U_T}}\right) \tag{5}$$

As can be seen, the moderate-inversion region ($V_G{\sim}V_T$) is most critical. Fig. 6 shows the influence of noisy data on the interpolation error depending on the sampling interval. For a very small data sampling interval, ΔV, the error of the derivative actually increases as $1/\Delta V$. In practice, optimum values for ΔV are about 1–2 thermal voltages.

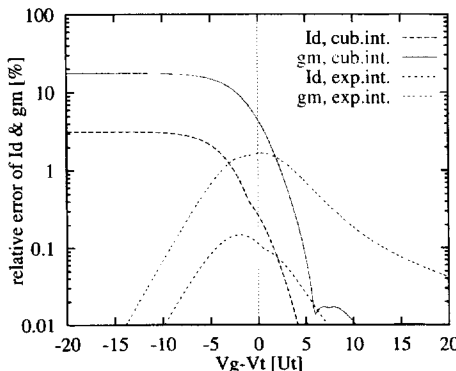

Fig. 5. Worst-case interpolation error of I_D and g_m using $I_D=I_s\ln^2\left(1+\mathrm{e}^{\frac{V_{GS}-V_T}{2U_T}}\right)$ as test function and a data sampling interval of $1.U_T$

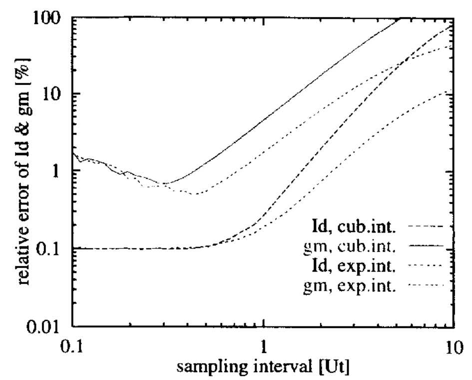

Fig. 6. Worst-case interpolation error of I_D and g_m versus the data sampling interval for noisy data ($n = 0.1\%$)

The maximum error of the output conductance g_o was determined numerically, using the following test expression:

$$I_D=I_s\left[\ln^2\left(1+\mathrm{e}^{\frac{V_{GS}-V_T}{2U_T}}\right)-\ln^2\left(1+\mathrm{e}^{\frac{V_{GS}-V_T-V_{DS}}{2U_T}}\right)\right](1+\lambda V_{DS}) \tag{6}$$

with $\lambda = 1/100$ V for long-channel transistors. The results are shown in Fig. 7: in strong inversion, the critical range of V_{DS} lies in the vicinity $V_{DS,sat}$, i.e. the transition between the linear and saturation region. In moderate to weak inversion, where the output curve becomes exponential, the critical range is 0 V to several U_T. In the critical V_{DS} range, the modified exponential interpolation with a maximum error of 4% performs better than the polynomial one. This may be important for some devices in analog circuits.

It is important to note that, although the polynomial interpolation used here is generally not monotonic for monotonic samples, the maximum error of the derivatives is well below

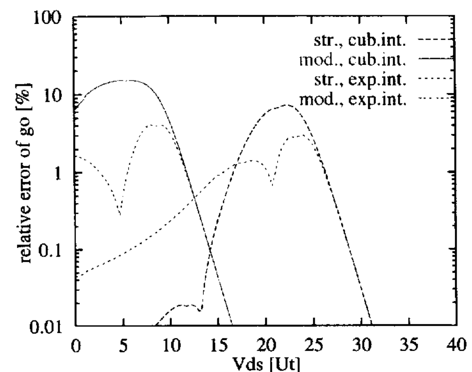

Fig. 7. Worst-case interpolation error of $g_o = \partial I_D/\partial V_{DS}$ in moderate inversion ($V_{GS} - V_T = 0$ V) and strong inversion ($V_{GS} - V_T = 20U_T$) [sampling interval = $1U_T$]

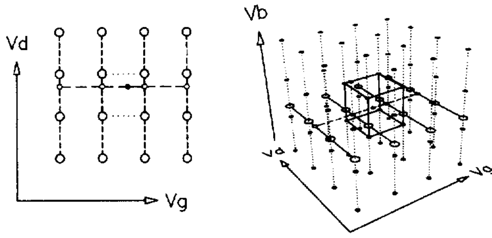

Fig. 8. Interpolation in two and three dimensions

100%. This is due to the fact that—apart from breakdown phenomena—terminal quantities of a MOSFET and their derivatives cannot quickly change arbitrarily with respect to the terminal voltages. Using equations (5) and (6), it can be shown that non-monotonicity cannot occur for a sampling interval of less than $1.94U_T$.

These one-dimensional interpolations are then combined to a two- or three-dimensional interpolation by nesting as shown in Fig. 8. A full three-dimensional interpolation requires 64 supporting data points around the target interval. First, the data are interpolated in the bulk-direction for 16 points in the V_D–V_G plane for the given V_B: second, the data are interpolated in the drain-direction for four points on the V_G line for the given V_D; and last, an interpolation is performed in the gate-direction for the given V_G. This algorithm is also employed for the computation of the derivatives. Although the partial interpolation of the derivatives is generally not consistent with the exact computation, the relative errors were found to be marginal ($< 10^{-4}$). The actual algorithm uses extensive pre-computation of polynomial coefficients to ensure high CPU efficiency of the program.

In the current implementation, one call to the model function takes 76 μs on an HP-PA 735 workstation. The memory consumption, taking typical numbers of $5 \times 20 \times 20 = 2000$ data points in V_{BS}, V_{GS} and V_{DS} directions, is about 80 kbytes per transistor type. Precomputed coefficients and decision flags could also be stored to speed up the execution at the expense of a higher memory consumption.

4. Applications

Fig. 9 shows the simulated switching transients of an RS flip-flop designed in a 0.5 V ultra-low power technology [11]. The same technology can be used to build OPAMPs, operating at even lower supply voltages.

In Fig. 10, simulation results of a ring-oscillator obtained with this model are compared against device-level simulations of the circuit with MINIMOS-NT [12]. The frequency error is 1.7% and the amplitude error is < 2 dB (1st–5th harmonic).

Due to its inherent accuracy, our new model could show the feasibility of ultra-low power OPAMPs working at supply voltages well below 1 V. To find the lower limits of the supply voltage, a set of basic circuits designed with dedicated digital ultra-low power (ULP) processes was simulated to determine the achievable performance.

Fig. 11 shows the simulated large signal step response of a two-stage OPAMP operating as a follower at $V_{DD} = 0.4$ V for two different loads. The frequency compensation is accomplished by wider output transistors (M7, M8), utilizing their internal capacitances rather than a separate

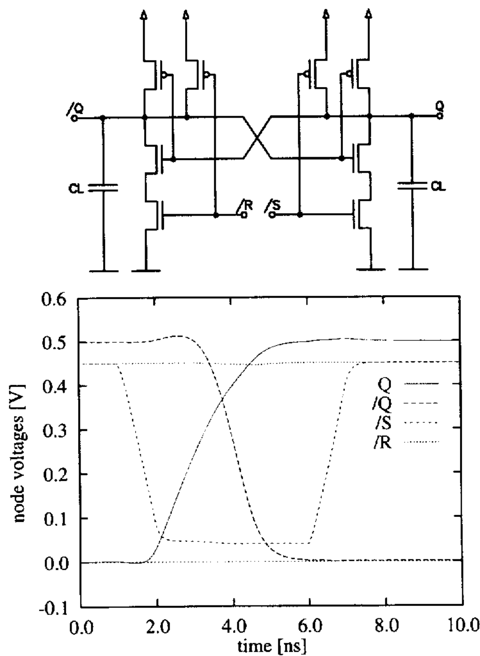

Fig. 9. RS flip-flop switching transients $V_{DD} = 0.5$ V

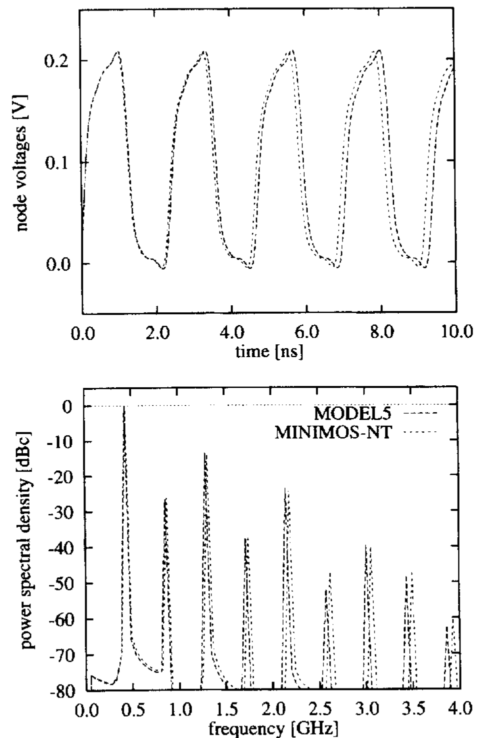

Fig. 10. Five-stage ring oscillator 0.2 V ULP technology: circuit simulation MODEL5 versus device-level simulation MINIMOS-NT

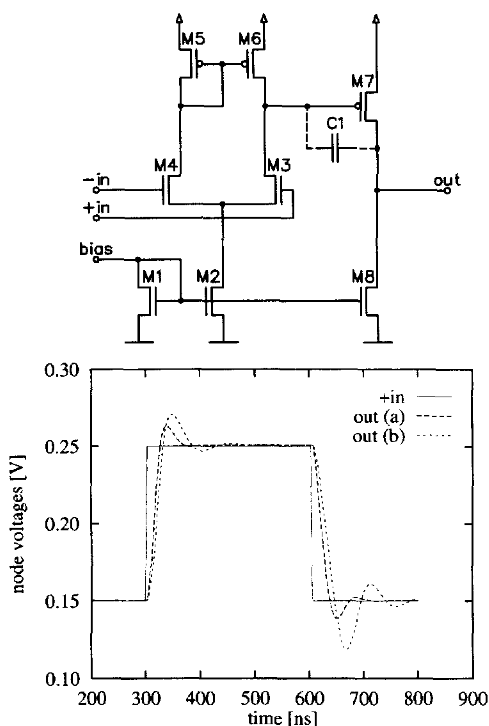

Fig. 11. Large-signal step response of a two-stage ULP OPAMP with a self-compensating output stage operating as a follower at $V_{DD} = 0.4$ V with (a) $C_L = 0$ pF and (b) $C_L = 1$ pF

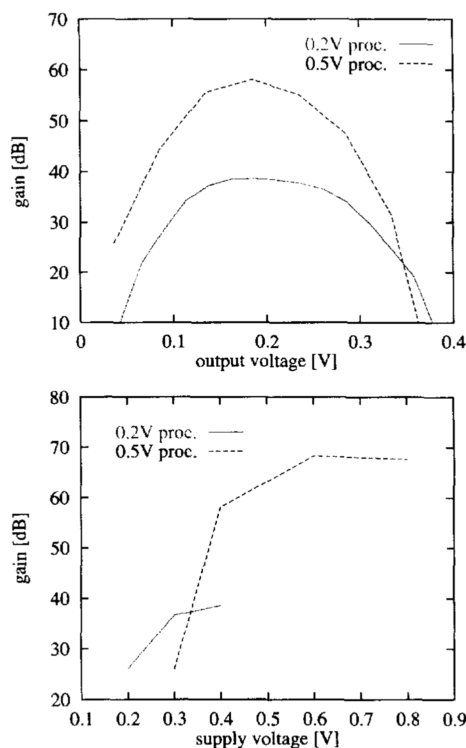

Fig. 13. Voltage gain versus V_{out} and maximum voltage gain versus V_{DD} of two-stage ULV OPAMPs operating at $V_{DD} = 0.4$ V as a function of the output voltage [0.2 V technology (a) and 0.5 V technology (b)]

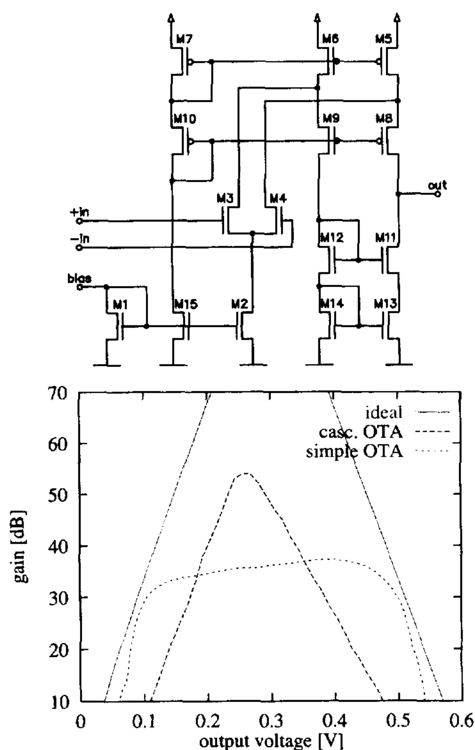

Fig. 12. Voltage gain of a simple OTA and a folded-cascode OTA (0.5 V technology), operating at $V_{DD} = 0.6$ V as a function of the output voltage

capacitor (C1). The OPAMP is biased for medium speed, consuming a total of 4.0 μW. Results from OTA simulations are shown in Fig. 12, indicating that cascoding is limited to $V_{DD} > 0.6$ V. Fig. 13 shows the achievable maximum voltage gain of two-stage OPAMPs, indicating that $V_{DD} = 0.5$ V could be a practical value for low-voltage mixed-analog-digital applications.

5. Conclusion

Our new low-voltage MOSFET modeling approach, together with the supporting software, enables the accurate simulation of modern mixed-analog-digital circuits directly from measured or simulated data. This can be profitably used for process evaluation and optimization on the circuit level without intermediate parameter fitting.

Acknowledgements

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