A Comparative Study of Single-Electron Memories

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***Abstract*—We study different memory cell designs and compare their advantages and disadvantages from an engineering point of view. We look at operational stability as a function of temperature and stray charge (random background charge), and discuss the issue of reliable mass production. We conclude that memories seem to be one of the most promising large scale single-electron tunnel applications, that lie, particularly when granular films are used, already in the range of today's process technology.**

***Index Terms*— Coulomb blockade, memory, quantum dot, single-electron, tunneling.**

I. Introduction

STARTING WITH the first observation and study of the Coulomb blockade by Gorter 1951 [1], the field of single-electronics has seen a huge development. Today the search for applications and feasible production techniques is in full motion. One of the most promising large scale applications is in our opinion a memory chip. The uniformity in structure of a memory chip lessens the interconnect problem which is one of the major issues any submicron technology faces today. Furthermore, bit errors are easier to correct in memory chips than in general logic circuits.

In Section II, we discuss several characteristics including operation temperature, error rate, and background charge dependence, which are crucial for robust mass production and reliable operation. In Section III, we review several memory designs, and we compare their characteristics in Section IV.

II. Characteristics of Single-Electron Memories

What are the criteria for a good single-electron tunnel (SET) memory design, which is fit for mass production? Such a SET memory should work at room temperature (300 K), or at least at liquid nitrogen temperature (77 K) with a reasonable bit error rate. It should have low power consumption and at the same time short read and write cycles. Robustness against random background charge is a prerequisite, and the SET device must be manufacturable with today's technology. Various designs have been proposed during the past years. To establish a better overview of the state-of-the-art of SET memories we analyzed six different designs with our single-electron device and circuit simulator SIMON [2], and discuss the results in view of the above stated criteria for a good SET memory cell.

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A. Operation Temperature

The smaller the capacitance C of the quantum dots or islands and the larger the quantum confinement energy E_p, the larger is the Coulomb energy E_c, and thus the larger is the operation temperature T:

$$E_p = \frac{\hbar^2 \pi^2}{2m^* l^2} \quad (1)$$

$$E_c = \frac{e^2}{2C} + E_p \gg kT \quad (2)$$

where

- m^* effective mass;
- l diameter (characteristic length) of the island or quantum dot;
- e elementary charge;
- k Boltzmann's constant.

The term $e^2/2C$ is the classical electrostatic charging energy, and E_p, the quantum confinement energy, is the characteristic spacing between two adjacent energy levels. To allow single-electron device operation, the Coulomb energy E_c must be the dominating energy in the system. How much larger the Coulomb energy should be compared to the thermal energy depends on the error rate one can afford. The range in the literature goes from $E_c > 3kT$ to $E_c > 100kT$. A straightforward way to increase E_c is to reduce spatial dimensions, because capacitance decreases and the quantum confinement energy increases. Other possibilities are to use different dielectric materials with a lower dielectric constant to reduce the capacitance, or materials that show much bigger quantum confinement energies than metals, such as semiconductors [3]. Fig. 1 shows a comparison between the classical electrostatic charging energy $e^2/2C$ and the quantum confinement energy for silicon and metals. We assume a sphere with diameter l and a surrounding material with a relative dielectric constant of $\epsilon_r = 10$, which has a self-capacitance of $C = 2\pi\epsilon l$. The graph shows that one needs a lithographic resolution better than 10 nm to achieve room temperature operation.

B. Error Rate/Probability

We have to distinguish between two error processes. One is a decay process where a stored bit of information changes its value over time. For example, a quantum dot may spontaneously discharge itself due to thermal agitation or co-tunneling [4]. The other one is that a write cycle may produce the wrong value, although the correct value was applied to the cell, or a read cycle may fail.

Bit Errors: The bit error rate is not an unequivocal criterion. An acceptable error rate for one application is not necessarily valid for another. However, we can make a practi-

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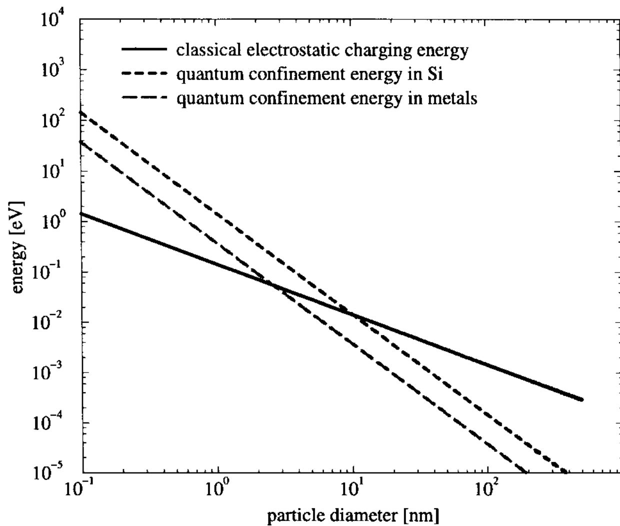

Fig. 1. Comparison between classical electrostatic charging energy and quantum confinement energy for silicon and metals.

cal estimation for memories. SET memory technology aims at the terabit (10^{12}) memory chip. If we assume that the whole information of such a chip is read or written every second for three years (10^8 seconds) with only one bit error, the probability for a bit error has to be below 10^{-20}:

$$P_{\rm err} \approx \exp\left(-\frac{E_c}{kT}\right) < 10^{-20} \Rightarrow E_c \approx 50kT. \quad (3)$$

This means that for room temperature ($T = 300$ K) the Coulomb energy E_c should be about 1 eV. According to Fig. 1 one needs a feature size in the nano-meter range for semiconductors. Error detecting and correcting schemes can obviously further reduce bit errors [5].

Read/Write Errors—Access Time: Due to the stochastic nature of the tunnel process, the exact time of tunneling of an electron is not known. One only knows rates and probabilities. Thus we need to wait considerably longer than the actual charging process would take, to assure with a certain error probability, that an electron actually tunneled. If we take typical values for tunnel resistance R and self-capacitance of a quantum dot C, we can calculate a characteristic charging time constant of

$$\tau = RC = 10^5 \cdot 10^{-18} = 0.1 \text{ ps}. \quad (4)$$

We assume an exponential distribution of the tunnel time of an electron. Then for the same upper bound of the error probability as above we get

$$P_{\rm err} \approx \exp\left(-\frac{t}{\tau}\right) < 10^{-20} \Rightarrow t > 44\tau. \quad (5)$$

Therefore one must wait about 5 ps for an electron to tunnel with an error probability lower than 10^{-20}.

C. Random Background Charge

This term denotes charged impurities located close to a quantum dot, as well as parasitic capacitances of other quantum dots which induce charges and often destroy the desired device function [4]. Currently there are three approaches under investigation that deal with this problem. One is to find process technologies which allow production of impurity free materials or materials where impurities accumulate in regions where they do not disturb device behavior. A second approach is to use SET features that are independent of random background charge, such as Coulomb oscillations. Such a design is reviewed in Section III-D. The third and for us most promising solution is to use, instead of a single island, an array of similar islands, so-called granular films, which show extraordinary insensitivity against random background charge. A design with these features is reviewed in Sections III-F and III-G.

D. Power Consumption

Because of the minuteness of capacitances and the low number of electrons involved in charging and discharging, the power consumption of SET memories is usually orders of magnitudes smaller than that of conventional memories. However, high integration densities and high switching speed may lead to unacceptable power dissipation of ~3 kW/cm^2 [6]. Any design which merely replaces FET's with SET transistors has a high power consumption since a constant static current is flowing. The energy dissipation of a single tunneled electron is of the order of the Coulomb energy, $e^2/2C$. With a tunnel rate of $\sim 1/eR_T$ the power dissipation of one SET transistor becomes $\sim e/2R_TC$, which is for typical parameters about 0.1 μW. Therefore integration densities of 10^{10}/cm^2 and more demand heat removal rates of kilowatts per square centimeter. Much better in this respect is SET logic, where a small number of electrons represent a logic state. No static current is flowing. Here again, one transferred electron dissipates roughly the Coulomb energy, $e^2/2C$, but this time the switching rate of gates is much lower than the intrinsic tunnel rate. With a switching time of 1 ns, the power consumption of one logic gate is about 10^{-10} W. Assuming the same integration density as before results in an acceptable power dissipation of ~1 W/cm^2 (see also [7]).

E. Manufacturability

To reliably and reproducibly manufacture structures of about 3-nm size or below is impossible with today's lithography techniques, and will not be possible for the next years or decades to come. But it is already feasible to produce particles of this small size and granular films consisting of such particles by employing self assembling material properties. With naturally formed tunnel junctions the position and exact size of individual granules is not controllable, but the set margins and the averaged characteristics are. In Sections III-F and III-H we review two cells built on this principle.

III. Single-Electron Memories

A. SET Flip-Flop

One design possibility is to mimic conventional memory design with SET devices, such as a static SET memory cell

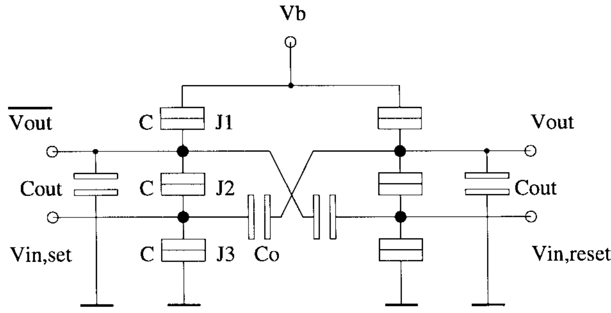

Fig. 2. Circuit diagram of a SET static memory cell (flip-flop).

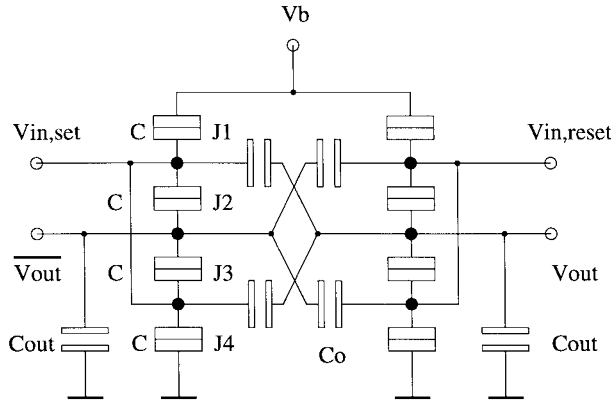

Fig. 3. Circuit diagram of a "complementary" SET static memory cell (flip-flop).

or flip-flop. Two designs were proposed by A. Korotkov *et al.* [8] (see Figs. 2 and 3). The operation is equivalent to a conventional flip-flop. In Fig. 2, junctions J_2 and J_3 form a SET transistor, J_1 is the load resistance. $C_{\rm out}$, the load capacitor, is much bigger than the characteristic capacitance C, which means that $C_{\rm out}/C$ electrons represent one bit of information. The "complementary" flip-flop of Fig. 3 replaces the load tunnel junction with a SET transistor, which makes it slightly more complex, but all its tunnel junctions are similar.

B. Electron Trap Memory

Nakazato and Ahmed [9], [10] proposed the idea of a dynamic memory cell pushed to its extreme. A small number of electrons, or even just a single electron, is stored on a single quantum dot. Their presence on the quantum dot QD corresponds to logical '1' and their absence to '0' (see Fig. 4). The line of tunnel junctions introduces an energy barrier for electrons entering or leaving QD. Thus, stored electrons reside in a local energy minimum. To write in this cell a voltage pulse is applied at V_g, which eliminates the energy barrier. A positive pulse V_g forces electrons to tunnel through junctions $J_6, J_5, \cdots, J_1$ onto island QD. A negative voltage pulse V_g forces electrons to tunnel off of QD to ground. The state of the quantum dot QD is sensed at $V_{\rm out}$. The more tunnel junctions are used the less likely it is that electrons escape from the storage node to ground, due to thermal agitation and co-tunneling. Amakawa *et al.* [11] showed, if one capacitively couples two traps, and stores electrons in one trap and holes

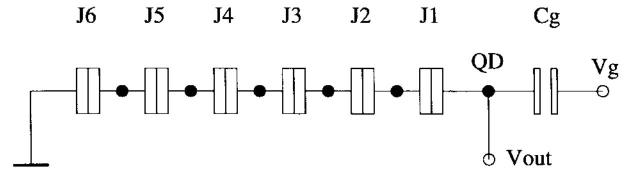

Fig. 4. Circuit diagram of an electron trap memory cell.

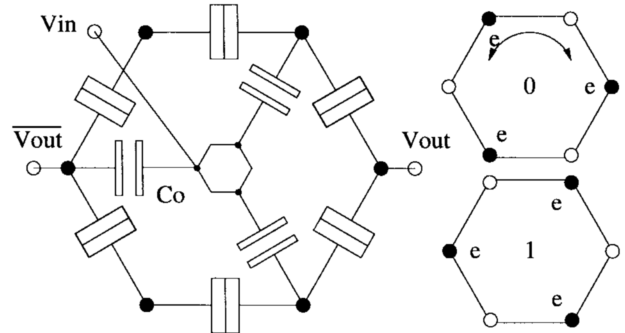

Fig. 5. Ring memory cell.

in the other, the stability of this 'dipole' is bigger than that of a single trap. In case of a single trap, at least two tunnel junctions are needed for a bistable behavior. We have chosen six tunnel junctions, so that flip-flop, electron trap memory and ring memory have the same number of junctions and are more comparable.

C. SET Ring Memory

A different idea which is a generalization of the bistable quantum cell for cellular automata by Lent *et al.* [12] is shown in Fig. 5. On the circuit level it is also similar to the electron trap memory, because it is a trap connected to a ring, a so called ring memory cell. However the operation is different. An even number n (in our case $n = 6$) of tunnel junctions is connected to a ring, and $n/2$ electrons are inserted into the ring. Due to their Coulomb interaction, they will repel each other and thus can form two stable configurations (see Fig. 5). Applying positive or negative voltage pulses on $V_{\rm in}$ will switch the state of the ring to either one of the stable configurations. The capacitors C_0 should be small compared to the capacitances of the tunnel junctions, so that the electrons have a large influence on their neighbors and keep their distance.

D. Q_0-Independent Memory

The first random background charge or Q_0-independent memory was proposed by Likharev and Korotkov [13]. The basic idea is the following. Electrons are stored on an island or floating gate $\rm QD_1$ (see Fig. 6). Electrons are moved through a tunnel junction J_g on or off the floating gate. An SET transistor $(J_1, J_2, {\rm QD}_2, C_g)$ which is very charge sensitive on its gate, is used to sense the changes of charge on the floating gate. The trick to achieve the Q_0-independence is not to sense any absolute charges, but to sense the relative change in charge, which causes current oscillations in the

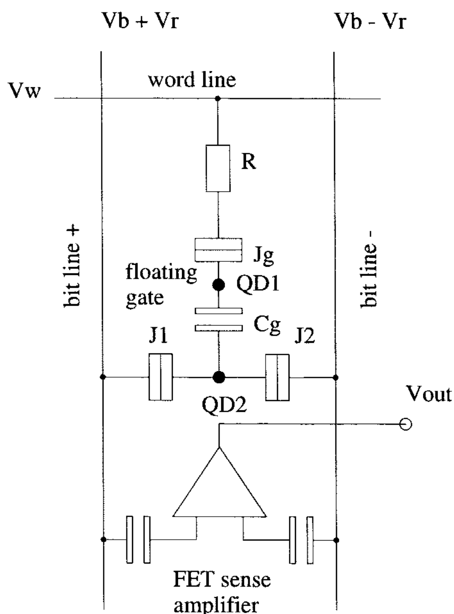

Fig. 6. Circuit diagram of a random background charge independent memory cell.

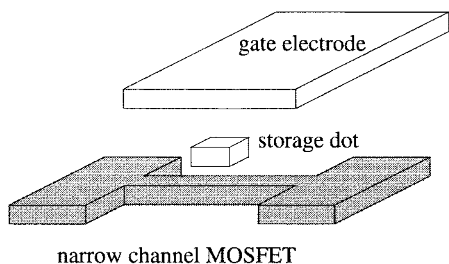

Fig. 7. Single island memory.

SET transistor, with a FET amplifier. In other words, the charge change on the floating gate induces oscillations in the current flowing through J_1 and J_2. These oscillations occur at any background charge. Only the phase, not the amplitude is background charge dependent. A disadvantage is that the cell can only be read destructively by discharging the floating gate. If the FET sense amplifier picks up current oscillations, then the floating gate was charged with electrons. If no oscillations are detected no charge was stored on the floating gate.

E. Single Island Memory

Recently, two groups [14], [15] suggested using a single floating Coulomb island in close proximity to a narrow conducting channel as a memory cell (see Fig. 7). Electrons which tunnel to the floating quantum dot, due to an appropriate voltage on the gate electrode, change the threshold voltage of the narrow channel. The quantum dot stores charge even after reducing the gate voltage. This hysteresis can be exploited for a memory cell.

F. Multiple Island Memory

A very promising design of a memory cell was proposed by Yano *et al.* [16], [17]. This design fulfills three major criteria: it works at room temperature, is random background charge independent and is manufacturable with today's process technology. The idea is similar to the previous one, in that a flash-memory-like device is considered. With a gate electrode charges are trapped in a granular film, which modulate the current through the same granular film (see Fig. 8). But the independence of random background charge is achieved in a different way, namely the use of many interconnected similar islands formed by a granular film, for instance, polysilicon. A simplified qualitative explanation for Q_0-independence is as follows. Consider a piece of granular film across which we apply a small bias voltage V_b (see Fig. 9). In the case of zero background charge ($Q_0 = 0$) no current will flow, due to the Coulomb blockade [see Fig. 9(a)]. If one increases the bias voltage further, then at one point a conducting path will form and current will flow [Fig. 9(b)]. If $Q_0 \neq 0$ single regions will exhibit no Coulomb blockade, due to the background charge, and others will show an increased Coulomb blockade (in Fig. 9(c) some paths conduct, others do not). But overall no conducting path has formed, thus the Coulomb blockade is still present. Increasing V_b will finally lead to a conducting path. Fig. 10 shows that the Coulomb blockade of an array of tunnel junctions is more or less independent of random background charge and similar to that of a single island transistor consisting of two tunnel junctions with the same parameters. The threshold voltage $V_{\rm th}$ will be different, but not necessarily smaller or bigger.

A disadvantage of this design is that the storage nodes, and the current path which is modulated by the charge on the storage nodes, are located in the same granular film. This prohibits an independent tuning of performance characteristics.

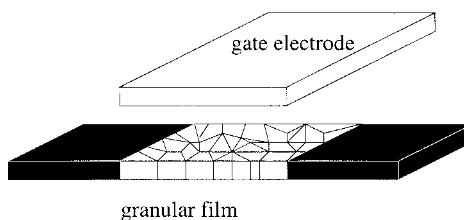

Fig. 8. Multiple island memory.

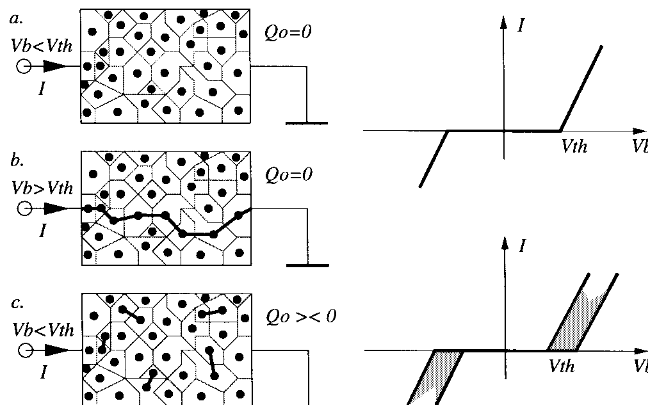

Fig. 9. A granular film exhibits a Coulomb blockade regardless of the background charge Q_0. The threshold voltage $V_{\rm th}$ will change a little if the background charge is changed.

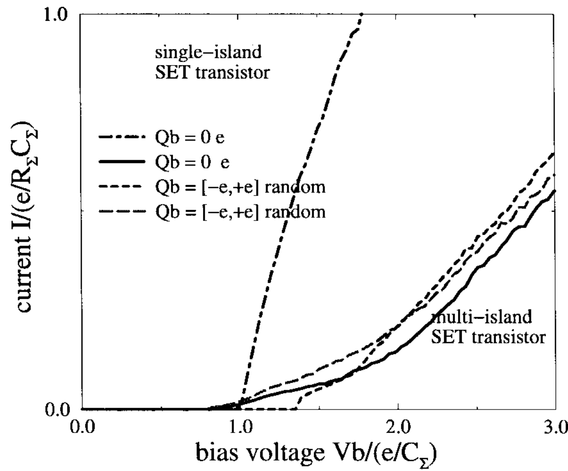

Fig. 10. I–V characteristics of single island SET transistor and multiple island SET transistor consisting of 50 islands.

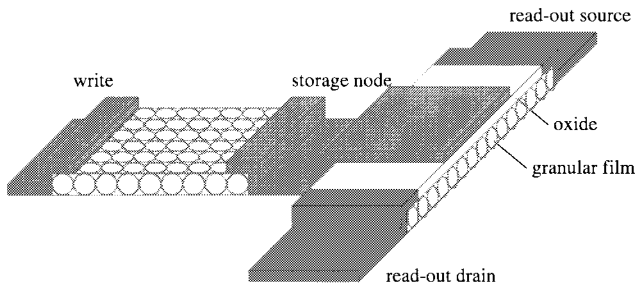

Fig. 11. T-memory cell.

G. T-Memory Cell

Recently we proposed a so-called T-memory cell which employs granular films in a different way [18]. Two granular film batches are arranged in a T-shape (see Fig. 11). The cross-bar of the T is a multi-island transistor which is controlled by a gate electrode which stores either a number of electrons or a number of holes. Writing a "1" or "0" is done by applying a positive or negative voltage pulse at "write." This will charge the gate electrode which has a function like the floating gate in a flash memory cell. Thus in our example a positive write pulse on "write" will store some holes on the gate electrode representing "1," and a negative write pulse will store some electrons on the gate electrode representing "0." The memory cell is read destructively by applying for example a negative voltage pulse at "write" and sensing current oscillations at "read-out." If oscillations are present the cell held a "1." If no oscillations are picked up the cell held a"0." The contents of the cell have to be restored accordingly.

The T-cell can be viewed as a combination of the electron trap memory and the Q_0-independent memory cell, with the difference that tunnel junction arrays are used instead of single tunnel junctions. This makes the T-memory cell much easier to manufacture. In fact, since the granular film batches can have dimensions in the 100 nm regime, state-of-the-art optical lithography is sufficient to produce such memory cells.

The access time of the T-memory cell depends on the resistance of the tunnel junction arrays. The tunnel junction array forming the trap should have a relative high resistance in order to store electrons for a long time (low co-tunnel rates). But too high a resistance would either make high read and write voltages mandatory or would result in a long access time. The read-out tunnel junction array should have a lower resistance, since enough electrons have to travel through the array in order to sense the relative charge change reliably. Thus, the tuning of the resistances will be a crucial part in the optimization of the T-memory cell.

TABLE I
COMPARISON OF MAXIMUM OPERATION TEMPERATURE $T_{\max}$ FOR A TUNNEL JUNCTION CAPACITY OF 0.35 aF, RANDOM BACKGROUND CHARGE DEPENDENCE, AND COMPLEXITY OF SIX MEMORY DESIGNS

memory design	T_{max}	background charge dependence	number of elements
flip-flop	17 K	yes	10–14
electron trap	74 K	yes	7
ring memory	34 K	yes	12
Q_0-independent memory	315 K	no	4
single island memory	300 K	yes	3
multiple island memory	86 K	no	NA
T-memory	120 K	no	NA

IV. COMPARISON OF MEMORY DESIGNS

All designs, except the last two—multiple island memory and T-memory—require the fabrication of one or more quantum dots with specific characteristics at a certain location. This has two disadvantages. First, a reliable industrial mass production of nano-scale quantum dots (∼3 nm) is not possible today. The National Technology Roadmap for Semiconductors [19] suggests that such a fine lithographic resolution will not be likely to happen in the next two decades. Second, designs which rely on a certain amount of charge on particular quantum dots are prone to failures caused by random background charge. Designs which use many similar quantum dots, that is granular films, show in this respect more promise.

We studied the dependence on the operation temperature and on the random background charge of the memory designs by simulation. Our single-electron device and circuit simulator SIMON is based on a Monte Carlo method. The change in Helmholtz's free energy for one tunnel event determines the associated probability. Among all possible tunnel events one is, according to their probabilities, randomly chosen as the actual one. By doing this many times, the transport of electrons through the circuit is simulated. SIMON features among others a graphical user interface, a graphical circuit editor, the inclusion of co-tunneling, and transient and stationary simulation modes. For further details, refer to [2], [20], and [21].

We did not set an error limit to define the operation temperature, but measured at which temperature the functioning of the memory stops. Usually this point is very pronounced. Raising the temperature produces more and more errors until the desired behavior vanishes. The maximum temperature given in Table I is the maximum operation temperature achievable with a characteristic capacitance of 0.35 aF. Reducing the size of the tunnel junctions and thus their capacitance will shift all operation temperatures to higher values. The dependence

on random background charge was determined at half the maximum operation temperature. For the simulations done here all capacitances are 0.35 aF and all tunnel resistances are 10^5 Ω, if not stated otherwise.

As can be seen in Table I, the straightforward copy of conventional design, as was done with the flip-flop, is the worst choice. The operation temperature is low, because the capacitors C_0 which cross-connect both inverters have to be about a factor three bigger than the capacitance of the tunnel junctions. This increases the capacitance of the quantum dots. The next best choice is the ring memory and the electron trap memory. Both are similar in design, but the electron trap memory has twice as high an operation temperature. This can be understood as follows. To introduce an error in the electron trap memory, at least one electron has to tunnel from the quantum dot QD all the way to ground. That is, it has to pass six tunnel junctions in our example. In the case of the ring memory two electrons have to tunnel only through a single junction to change the state of the cell, because once two electrons tunnel in the same direction it is energetically favorable for the third electron to tunnel, too. Thus the electron trap memory has a bigger barrier against thermal fluctuations. All three—flip-flop, electron trap memory, and ring memory—are very sensitive to random background charge. Therefore, as long as the available process technology cannot provide impurity free materials, these designs have limited practical value. The single Coulomb island memories combine a quantum dot with a narrow channel MOSFET. For a small dot room temperature operation is possible. Unfortunately, they are prone to random background charge and difficult to manufacture reliably, because of the reliance on a single quantum dot.

The Q_0-independent memory, the multiple island memory, and the T-memory are very interesting alternatives. All three show the crucial independence to random background charge. The Q_0-independent memory has a big advantage in operation temperature. The reason is that the Coulomb oscillations are visible at much higher temperatures than is a Coulomb blockade. In the case of the T-memory cell which also uses the Coulomb oscillations, the maximum operation temperature is about a factor two smaller than the maximum operation temperature of the Q_0-independent memory. The reason for this is that a quantum dot in a two-dimensional array has more neighbors than in a linear arrangement, which increases the capacitance and thus reduces the operation temperature.

An important issue for the fabrication and the achievable integration density (bits/cm^2) is the complexity and size of the various memory cells. The SET flip-flop shows the highest complexity with ten elements (six tunnel junctions and four capacitors) with varying element parameters, or in the case of the complementary design even 14 elements (eight tunnel junctions and six capacitors). Ring memory and electron trap memory, which employ 12 and seven elements, respectively, are simpler in design. Their elements have similar parameters and the interconnection is less complex. Especially in the case of the electron trap memory the connection problem is considerably reduced, since only one island has to be connected to the outside, and the number of tunnel junctions is not crucial. The Q_0-independent memory has only four elements (two tunnel junctions, a floating gate and a port to the floating gate) plus a FET sense amplifier which can be responsible for many memory cells. Single Coulomb island memory, multiple island memory, and the T-memory have a relatively simple structure.

Cell sizes of 50 by 50 nm and below are possible, which would result in an integration density of 4×10^{10} bits/cm^2.

V. Outlook

The production of SET memory chips which work at room temperature is possible in the near future. One needs the ability to produce granular films with grains of nanoscopic size, or another process with which it is possible to fabricate nanometer particles or quantum dots. Advanced lithography techniques with feature sizes below 50 nm, like e-beam, X-ray, or nano-imprint [22], are favorable for the definition of the bigger cell structures, but are not mandatory, since the essential tiny island size can be provided by granular film technology. Based on the multiple island memory or the T-memory, gigabit memories are feasible with 200-nm lithography resolution, and terabit memory chips are in reach as soon as advanced lithography techniques find their way from the laboratory to the industry.

VI. Conclusion

We simulated different memory designs and studied their maximum operation temperature and their dependence on random background charge. Room temperature operation is possible with feature sizes below 3 nm. The critical problem of random background charges appears to be solvable. Granular films reduce the burden on lithographical resolution and alleviate problems with uncontrollable background charges, thus making them likely candidates for application in future SET memory chips.

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