Single-Electron Memories with Terabit Capacity and Beyond

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1. Introduction

The need for more information storage capacity in the near future is evident. The lasting trend to mobile electronics (palm computers, cellular phones, video cameras, still cameras, etc.) demands high density and low power storage devices. Take for example a high resolution color still image (1024 x 764 x 24 bit). Without compression one requires almost 20 Mbit storage capacity for a single image. This relates to about 2 Gbit for a still camera capable of storing 100 images, and to almost 4 Tbit for a 2 hour high resolution video (30 frames/second). Certainly intelligent compression techniques can reduce these numbers considerably. We mention them here to give the reader a feeling for the magnitudes involved. Or look for example at software packages. They need frequently more than 1 Gbit storage capacity, and the exponential growth continues. In order to meet these demands and to provide product engineers with the desired memory components, a fast, high density, low power and possibly nonvolatile memory technology is required. A solid state solution has a clear speed (access time) and miniaturization advantage over magnetic or optical solutions. However, conventional solid state memory has a storage size, power consumption, and cost/bit disadvantage to other technologies. Single-electron technology provides great prospects to meet these challenges. Thus, we will present a single-electron memory cell, our T-memory cell, which can be integrated with today's process technology to produce memory chips of 1 Tbit storage capacity and beyond. At the same time power consumption is reduced by orders of magnitude and an access time of about 1 ns seems possible.

Although single-electron technology seems today to be more appropriate for memories, a new promising scheme for single-electron logic has been proposed.[1] Especially its reduced sensitivity to random background charge gives hope for large scale integrated single-electron logic devices.

In Section 2 we give a brief introduction to single-electronics. In Section 3 we present our analysis tool, SIMON, a single-electron device and circuit

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simulator. In Section 4 we discuss the operation, production, advantages and disadvantages of the T-memory cell.

2. Short introduction to single-electronics

Quantization of charge in metallic or semiconductor islands (quantum dots, granules) is usually not directly noticeable. However, when the size of such islands is in the nanometer regime, that is when the total capacitance becomes very small and the charging energy is larger than the thermal energy, then the change in free energy associated with the addition or subtraction of a single electron from an island, or a quantum dot, becomes significant.

New phenomena appear, such as the Coulomb blockade, which is a suppression of current flow at low voltage bias, and Coulomb oscillations, a time or space correlated transfer of electrons through tunnel junctions. With these new quantum effects it is possible to control the movement and position of single electrons. Beside the desired characteristics of controlled transfer of single electrons, undesirable effects arise, too. Among these, co-tunneling and the sensitivity to uncontrollable impurities and stray charges are the most critical ones. Co-tunneling, a simultaneous tunneling of two or more electrons in different tunnel junctions, provides a path for electrons to escape the Coulomb blockade and thus "weakens" the Coulomb blockade. Co-tunneling often plays an important role in the lifetime of stable electron states, for example stored electrons representing a bit of information, and in leakage currents. The sensitivity to uncontrollable impurities and stray charges, which is referredto as sensitivity to random background charges, introduces another serious handicap. Random background charge directly "attacks" the size of the Coulomb blockade and can in certain cases eliminate the Coulomb blockade completely. Whereas the amount of co-tunneling can be engineered, by introducing less transparent tunnel junctions or introducing more tunnel junctions in series, random background charge is much more difficult to deal with. In the case of single-electron memories practical ideas to eliminate the random background charge problem exist, as will be explained later, but for single-electron logic no real practical approach has been developed.

A general introduction to the field of single-electronics can be found for example in Ref. 2 and a very detailed and comprehensive one in Ref. 3.

3. Analysis tool — SIMON

To conduct our analyses we developed a simulation tool. SIMON is a single-electron device and circuit simulator based on a Monte Carlo method, where the free energy before and after any particular tunnel event determines the probability for tunneling. Among all possible events one is chosen as the winner according to the computed probability distribution and the state of the circuit is updated. By simulating many tunnel events the macroscopic device characteristics are obtained. In the same manner co-tunneling can be accounted for, by allowing two or more

tunnel events to happen at the same time. One important condition underlying the successful operation of single-electron devices and also underlying this simulation method is that electrons have to be well localized on the islands. This condition means that all tunnel resistances have to fulfill

$$R_T > \frac{h}{e^2} \equiv 25813\,\Omega \tag{1}$$

$$\Gamma(\Delta F) = \frac{1}{e^2 R_T}\left(\frac{-\Delta F}{1 - e^{\frac{\Delta F}{k_B T}}}\right) \tag{2}$$

$$\Gamma^{(N)} = \frac{2\pi}{\hbar}\left(\prod_{i=1}^{N}\frac{\hbar}{2\pi e^2 R_{Ti}}\right)\left[\sum_{\mathrm{perm}(k_1,\ldots,k_N)}\left(\prod_{k=1}^{N-1}\frac{1}{\Delta F_k - \frac{k}{N}\Delta F_N}\right)\right]^2 \times$$
$$\times \frac{\Delta F_N}{(2N-1)!\left(e^{\frac{\Delta F_N}{k_B T}} - 1\right)} \prod_{i=1}^{N-1}\left((2\pi k_B T_i) + \Delta F_N^2\right) \tag{3}$$

$$\tau = -\frac{\ln(r)}{\Gamma} \tag{4}$$

where ΔF is the change in free energy caused by a single tunnel event, Γ is the tunnel rate for normal tunnel events, $\Gamma^{(N)}$ is the tunnel rate for N^{th}-order co-tunneling, τ is the time duration between two consecutive tunnel events, and r denotes a uniformly distributed random number in the interval [0, 1]. More information on the simulation of single-electron devices and circuits can be found in Ref. 4.

SIMON features a graphical circuit editor that is embedded in a graphical user interface (Fig. 1). This interface allows easy use and quick circuit design. An interactive simulation mode is provided, where electrons can be forced to tunnel through particular junctions. Node charges, node voltages, tunnel rates and energy differences can be studied interactively. This mode allows a very detailed analysis of single-electron circuits. SIMON is publicly available. For further information see Refs. 5-7.

4. T-memory

High-density memories are a very suitable application for single-electron devices. The storage of binary information using Coulomb-blockade phenomena has been demonstrated in theory[3,8] and in practice.[9-12] Just recently, at the 1998 International Solid State Circuits Conference, Yano *et al.* presented a 128 Mbit early prototype for gigascale single-electron memory.[13] This chip is so far the biggest single-electron memory fabricated. However, several issues were identified

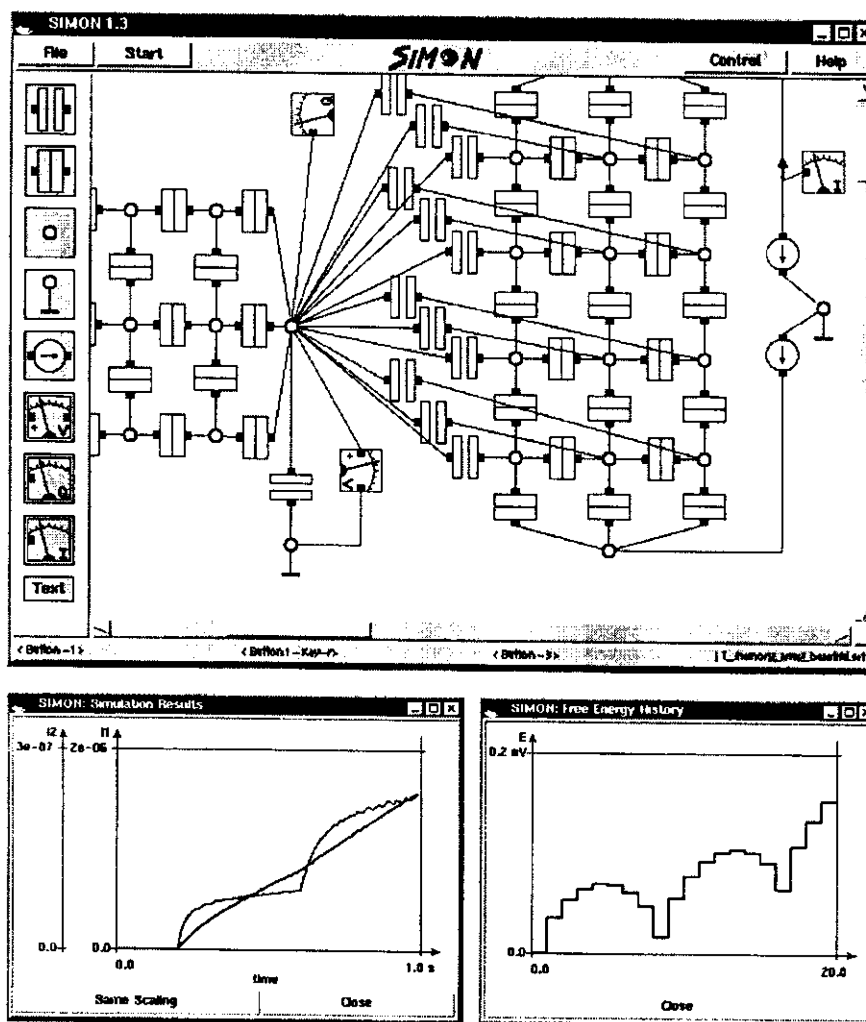

Figure 1. Screen shots of SIMON. The top picture shows the graphical circuit editor. In the lower left picture the I-V characteristics of a symmetric and asymmetric single-electron transistor are shown. In the lower right picture the change in system energy for the charging of a single-electron trap is shown.

that make a large scale integration of single-electron memory cells with today's process technology very difficult. The most notable of these problems are the achievement of room temperature operation, which demands lithographic resolution of less then 10 nm, and the sensitivity to random background charge, which demands perfectly clean production processes. Considering the current ULSI trends, neither of these issues will be resolved in the near future.

Summarizing, the main requirements to make single-electron circuits feasible for industrial application today are:

- room temperature operation → islands smaller than 10 nm
- insensitivity to random background charge
  → absolutely clean production processes
  → Coulomb oscillations instead of Coulomb blockade
- mass production → optical lithography

All of these requirements can be met by using granular films. Their usage eliminates the necessity for nanolithography, since nanoscopic tunnel junctions and granules are formed naturally. Additionally, granular films provide an averaging of the Coulomb blockade, alleviating the background charge problem.

Several production methods for two-dimensional granular films spanning a wide variety of material systems have been developed and many more are under development. Metallic granular films can be produced by condensing Al or Au on a substrate.[14] Several methods exist in which semiconducting granular films are formed.[15-17] Employing molecular beam epitaxy, nanoscopic InGaAs or InP dots or pyramids can be grown.[18,19] Colloidal deposition can be used to first form granules, which are afterwards deposited on a substrate.[20,21] This process is possible for metallic and semiconducting materials. Since single-electronics requires only small conducting granules separated by thin nonconducting tunnel barriers, more exotic material systems are equally interesting. For example, polymers of which some forms can conduct current could be used. Or even organic films would be a possibility. This latitude in material systems gives great promise as well as a lot of work for the future of single-electronics.

Several memory designs were analyzed with SIMON.[22] In consequence of these investigations, we proposed a new memory design called T-memory. This cell consists of two granular film batches that are arranged in T-form and that are capacitively coupled at their junction. Figure 2 shows two possible realizations.

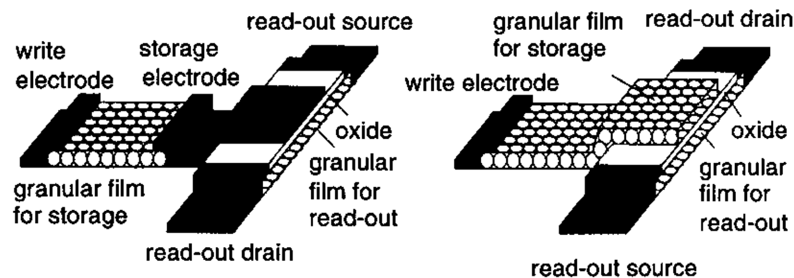

Figure 2. The T-memory consists of two granular film batches that are capacitively coupled. On the left side the capacitive coupling is achieved with a separate electrode. On the right side, an alternative realization, the two granular film batches directly overlap.

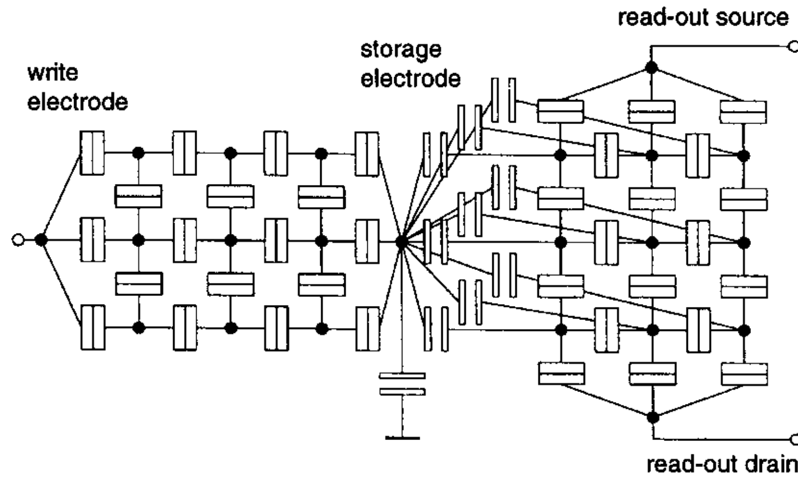

Figure 3. Equivalent circuit of the T-memory cell.

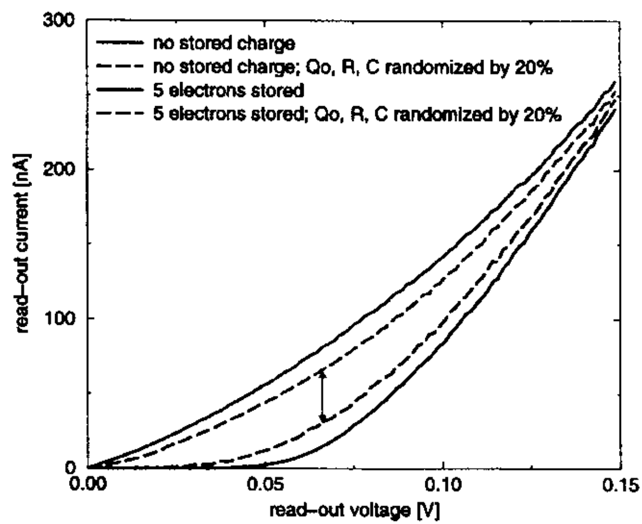

Figure 4. Charge dependence of the $I(V)$ characteristic of the granular film electrometer (transistor).

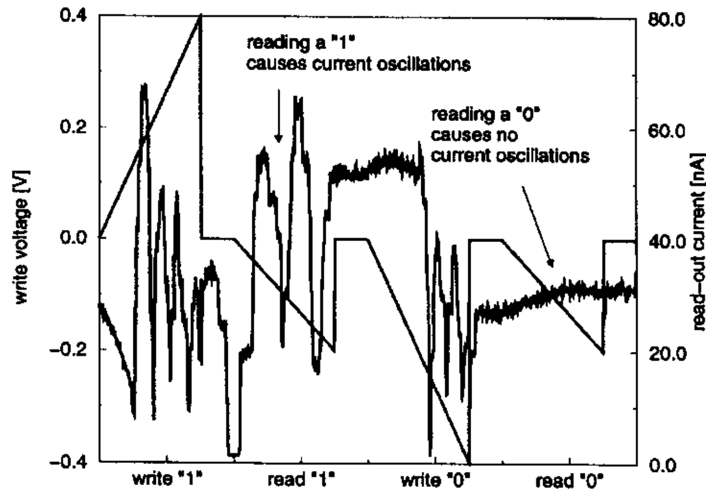

Figure 5. Second read-out mechanism employing Coulomb oscillations. The stored information can be retrieved by discharging the storage electrode.

Figure 3 depicts the equivalent circuit of the T-memory cell. It turns out that using two granular films, one for storing charge and the other to read out the stored information, gives the designer great flexibility in optimizing the cell. This flexibility enables one to tune storage time to achieve, for example, a nonvolatile memory and at the same time to optimize read-out characteristics for reliable information retrieval.

The granular batch representing the cross-bar of the T can be viewed as a multi-island single-electron electrometer (transistor). The other granular batch is the port to charge or discharge the storage electrode that influences the electrometer.

Two different read-out mechanisms are imaginable for the T-memory cell. The first one makes use of the dependence of the static $I(V)$ characteristic of the read-out electrometer on the stored charge. Figure 4 shows the dependence of the $I(V)$ characteristic on the charge stored in the storage electrode.

The other mechanism is a destructive read-out, which was first published by Likharev and Korotkov.[23] One attempts to discharge the storage node. If current oscillations are sensed with the read-out electrometer, the cell was charged (state 1), otherwise it was empty (state 0). Accordingly, the contents of the cell have to be restored. This operation is similar to a refresh cycle in DRAMs. Figure 5 shows the signals when reading a 1 and a 0.

Arranging several T-memory cells in matrix form results in a bit-addressable memory chip. Applying at the same time a positive voltage pulse at a word line and a negative pulse at two adjacent bit lines (or *vice versa*, a negative pulse at the

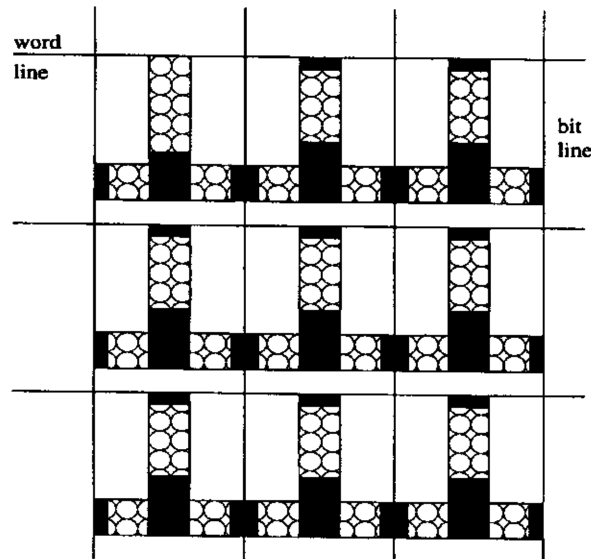

Figure 6. Bit-addressable T-memory. Applying at the same time a positive voltage pulse at a word line and a negative pulse at two adjacent bit lines addresses one cell, which can be written or read.

word line and a positive pulse at the bit lines) addresses one cell, which can be written or read (see Fig. 6). The bit-addressability is only possible if the Coulomb oscillation read-out mechanism is used.

5. Conclusion

Attempting to solve the main challenges, which are room temperature operation, random background charge independence, and industrial mass fabrication with today's process technology, we have proposed the T-memory cell. This memory cell employs two capacitively coupled granular films. The films can be made from various materials ranging from metals and semiconductors to polymers and organic substances. Nanometer granules that make up the granular film provide a Coulomb blockade large enough for room temperature operation. Granules form naturally, thus there is no need for nanolithography. Read-out by Coulomb oscillations and the randomizing statistical properties of granular films provide considerable insensitivity to random background charges. Thus the T-memory cell can be integrated with today's process technology for terabit memory chips.

References

1. T. Oshima and R. A. Kiehl, "Operation of bistable phase-locked single electron tunneling logic elements," *J. Appl. Phys.* **80**, 912 (1996).
2. K. K. Likharev, "Correlated discrete transfer of single electrons in ultrasmall tunnel junctions," *IBM J. Res. Develop.* **32**, 144 (1988).
3. H. Grabert and M. H. Devoret, eds., *Single Charge Tunneling—Coulomb Blockade Phenomena in Nanostructures*, New York and London: Plenum Press and NATO Scientific Affairs Division, 1992.
4. C. Wasshuber, *About Single-Electron Devices and Circuits*, Ph.D. thesis, Technische Universität Wien, 1997.
5. C. Wasshuber, H. Kosina, and S. Selberherr, "SIMON—a simulator for single-electron tunnel devices and circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.* **16**, 937 (1997).
6. C. Wasshuber and H. Kosina, "A single-electron device and circuit simulator," *Superlatt. Microstruct.* **21**, 37 (1997).
7. Information available at http://www.iue.tuwien.ac.at/.
8. K. Nakazato, R. J. Blaikie, and H. Ahmed, "Single-electron memory," *J. Appl. Phys.* **75**, 5123 (1994).
9. K. Yano, T. Ishii, T. Hashimoto, *et al.*, "Room-temperature single-electron memory," *IEEE Trans. Computer-Aided Design* **41**, 1628 (1994).
10. N. J. Stone and H. Ahmed, "Silicon single-electron memory structure," *Microelectronic Engineering* **41/42**, 511 (1998).
11. C. D. Chen, Y. Nakamura, and J. S. Tsai, "Aluminum single-electron nonvolatile floating gate memory cell," *Appl. Phys. Lett.* **71**, 2038 (1997).
12. A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, "Room temperature operation of Si single-electron memory with self-aligned floating dot gate," *Appl. Phys. Lett.* **70**, 1742 (1997).
13. K. Yano, T. Ishii, T. Sano, *et al.*, "128 Mb early prototype for gigascale single-electron memories," *Proc. IEEE International Solid-State Circuits Conference* (1998), p. 344.
14. W. Chen and H. Ahmed, "Fabrication and physics of ~2 nm islands for single electron devices," *J. Vac. Sci. Technol. B* **13**, 2883 (1995).
15. Y. Ishikawa, N. Shibata, and S. Fukatsu, "Creation of highly-ordered Si nanocrystal dots suspended in SiO_2 by molecular beam epitaxy with low energy oxygen implantation," *Jpn. J. Appl. Phys.* **36**, 4035 (1997).
16. A. Dutta, M. Kimura, Y. Honda, *et al.*, "Fabrication and electrical characteristics of single electron tunneling devices based on Si quantum dots prepared by plasma processing," *Jpn. J. Appl. Phys.* **36**, 4038 (1997).
17. T. Nakanishi, B. Ohtani, and K. Uosaki, "Construction of semiconductor nanoparticle layers on gold by self-assembly technique," *Jpn. J. Appl. Phys.* **36**, 4053 (1997).
18. M. Kawabe, Y. J. Chun, S. Nakajima, and K. Akahane, "Formation of high-density quantum dot arrays by molecular beam epitaxy," *Jpn. J. Appl. Phys.* **36**, 4078 (1997).

19. H. Fujikura, M. Araki, Y. Hanada, M. Kihara, and H. Hasegawa, "Formation of two-dimensional arrays of InP-based InGaAs quantum dots on patterned substrates by selective molecular beam epitaxy," *Jpn. J. Appl. Phys.* **36**, 4092 (1997).
20. C. Lebreton, C. Vieu, A. Pepin *et al.*, "Coulomb blockade effect through a 2D ordered array of Pd islands obtained by colloidal deposition," *Microelectronic Eng.* **41/42**, 507 (1998).
21. M. Mejias, C. Lebreton, C. Vieu *et al.*, "Fabrication of Coulomb blockade devices by combination of high resolution electron beam lithography and deposition of granular films," *Microelectronic Engineering* **41/42**, 563 (1998).
22. C. Wasshuber, H. Kosina, and S. Selberherr, "A comparative study about single-electron memories," to appear in *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.* (1998).
23. K. K. Likharev and A. N. Korotkov, "Analysis of Q_0-independent single-electron systems," *Proc. Intern. Workshop Computational Electronics* (1995), p. 42.