Propagation of RF Signals in Microelectronic Structures

Rainer Sabelka Christian Harlander Siegfried Selberherr

Institute for Microelectronics, TU Vienna

In deep submicron ULSI designs the overall circuit behavior is significantly determined by the on-chip interconnect structure. Due to the steady increase in device speed and clock frequencies in the GHz regime, integrated circuits will behave more and more like microwave circuits. The electrical characteristics of the interconnects is becoming more important as designs with reduced safety margins close to the physical limits require highly accurate models.

While most models are limited to the interconnects resistance and capacitance, with higher operating frequencies inductive effects gain importance. This is especially true for long interconnect lines as used for clock and power distribution, global busses and other long low-resistance interconnects optimized for high performance [1]. During the design phase care must be taken on various parasitic effects, like:

- attenuation caused by resistive voltage drops,
- delay times,
- crosstalk (caused by capacitive or inductive coupling or by the substrate),
- reflections incurred by discontinuities,
- skin-effect and eddy currents (e.g. in spiral inductors).

The conventional approach to model the interconnects parasitics is to extract global electric parameters (resistance, capacitance, inductance) and build a lumped model that approximates the characteristics of the interconnect to a certain extent. This model can then be simulated with a circuit simulator like SPICE.

Accurate Parameter extraction is key for a successful simulation. An immense number of such extraction methods have been reported in the literature - the next few paragraphs shall give a short summary.

Capacitances can either be calculated

- analytically, which is only possible for very simple structures (e.g an infinitely long straight line over a ground plane [2]),
- with geometrical models, which is very fast, but inaccurate for complex geometries with many layers [3], or
- with numerical methods, based on the solution of the Laplace equation, which have naturally a higher CPU-time and memory consumption.

The two most popular numerical techniques are the boundary element method (BEM, e.g. in [4]) and the finite element method (FEM, e.g. in [5]).

BEM:
- kernel of the PDE must be known
- small but full system matrix
- most efficient for regular stratified dielectrics
- acceleration possible with multipole method
- acceleration possible by neglecting influence of far apart conductors

FEM:
- large, but sparse matrix
- fast, iterative solvers can be used
- most flexible

A combination of BEM and FEM, the so-called hybrid method, combines the advantages of both [6]. Areas with stratified layers are calculated with the BEM, for non-planar regions the FEM is used. Special care must be taken at the interfaces.

The interconnect resistance can either be approximated with polygonal decomposition models (e.g. by "counting squares"), or a numerical technique like BEM or FEM. Here, the FEM seems to be most accurate and robust, however at the cost of an higher computational effort. Speedups can be obtained by

optimizing the elimination order of the Gaussian solver and by introducing articulation nodes. Substrate Resistance calculation is also performed with BEM, FEM, or geometric models [7].

Most inductance calculation methods are based on a numeric solution of the integration of Neumann's formula for a precalculated current density distribution. The current density is calculated either statically by solving the Poison equation, or in time-harmonic domain. The integration can either be carried out analytically for simple geometries, numerically, where special attention has to be paid on the singularities of the integrand, or with the Monte Carlo method. The partial element equivalent circuit (PEEC) method should also be mentioned in this context [8].

For certain applications lumped models based on extracted parameters are not adequate to describe the circuit behavior and the coupled system must be examined. For long low-resistance interconnects in TEM or quasi TEM configurations transmission line models based on the telegraph equation do a good job. At high frequencies and steep current ramps models based on a static current distribution may not be accurate enough and a full 3d transient analysis is required e.g. by a quasi-stationary approximation of Maxwell's equations, that excludes the formation of electromagnetical waves. It may even be necessary to simulate the whole set of Maxwell's equation, however, this can only be done for a very small area of the chip because of the enormous computational effort.

In summary, we can find three starting points for further reducing parasitic effects namely design, simulation, and materials.

During the design new routing strategies that better account for transmission line effects, the introduction of ground planes or shielding wires will help to control on-chip inductive effects.

New simulation methods are required that are accurate, efficient, robust, and flexible. The accuracy should be known and controllable (tradeoff between accuracy and runtime), the user interaction should be minimized.

The migration from Aluminum to Copper lowers the interconnect resistivity significantly. Together with the introduction of low-k dielectrics the RC time constant can be reduced by a factor of 5. However, decreased resistance and capacitance will bring out inductive effects more intensively, thus still increasing the importance of numerical inductance extraction methods.

References

[1] A. Deutsch, G. V. Kopcsay, C. W. Surovic, B. J. Rubin, L. M. Terman, R. P. Dunne, Jr., T. A. Gallo, and R. H. Dennard, "Modeling and characterization of long on-chip interconnections for high performance microprocessors," *IBM J.Res.Dev.*, vol. 39, pp. 547–567, Sept. 1995.

[2] A. Ringhandt and H. Wagemann, "An exact calculation of the two-dimensional capacitance of a wire and a new approximation formula," *IEEE Trans.Electron Devices*, vol. 40, no. 5, pp. 1028–1032, 1993.

[3] S.-C. Wong, P. S. Liu, J.-W. Ru, and S.-T. Lin, "Interconnect capacitance models for VLSI circuits," *Solid-State Electronics*, vol. 42, no. 6, pp. 696–977, 1998.

[4] F. Beeftink, A. J. van Genderen, N. P. van der Meijs, and J. Poltz, "Deep- submicron ULSI parasitics extraction using space," in *Design, Automation and Test in Europe Confere, Designer Track*, pp. 81–86, Feb. 1998.

[5] A. Hieke, "Simple ADPL implementation of a 3d FEM simulator for mutual capacitances of arbitrary shaped objects like interconnects," in *Proc. 2nd Int. Conf. on Modeling and Simulation of Microsystems*, (San Juan, Puerto Rico, USA), pp. 172–175, Apr. 1999.

[6] E. B. Nowacka and N. P. van der Meijs, "The hybrid element method for capacitance extraction in a VLSI layout verification system," in *Proc. Software for Electrical Engineering Analysis and Design* (P. P. Silvester, ed.), (Pisa, Italy), pp. 125–134, Computational Mechanics Publications, May 1996.

[7] T. Li, C.-H. Tsai, E. Rosenbaum, and S.-M. Kang, "Substrate modeling and lumped substrate resistance extraction for CMOS ESD/latchup circuit simulation," in *Proc. 35th Design Automation Conference*, (New Orleans, Louisiana), pp. 549–554, ACM, June 1999.

[8] P. Brennan, N. Raver, and A. Ruehli, "Three-dimensional inductance computations with partial element equivalent circuits," *IBM J.Res.Dev.*, vol. 23, no. 6, pp. 661–668, 1979.