Minimizing Thick Resist Sidewall Slope Dependence on Design Geometry by Optimizing Bake Conditions

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We successfully optimized the sidewall slope of a 2.5 μm thick photoresist. We found that the sidewall slope strongly depends on the pattern size and thickness of the photoresist. By optimizing the hard-bake process conditions it was possible to minimize this sidewall dependence and therefore to improve the implant blocking capability at the resist corners. As a result of this improvement we could obtain a higher process margin for the isolation spacing for CMOS inverter structures. We present simulation data which clearly show the impact of insufficient blocking capability on the final device structure.

1. INTRODUCTION

Despite the global trend of reducing junction depth and transistor sizes there are still numberous applications in CMOS technology which require high energy implants. A retrograde well scheme has significant advantage over previously used lightly doped well techniques [1]. These well implants are usually masked and require thick photoresists to completely block the implant, which increases the complexity of the coating and baking process. Recently, buried layer implants were introduced to increase latchup immunity. These applications require ion implant energies ranging from $200keV$ up to $1.5MeV$ and implant doses ranging from $1e12cm^{-2}$ to $1e15cm^{-2}$. The use of these high energy implants demands new challenges for the masking materials. Bake treatments are necessary prior to the implant to avoid thermal effects such as pattern deformation, blistering and cracking in the photoresist [2] [3]. Degradation of the photoresist polymer chains during implantation leads to outgassing and the formation of hardened, carbonized layers in the resist. These carbonized layers are generally difficult to strip. In this work we have optimized the bake treatment with regard to the resist sidewall slope dependence and the impact on the blocking capability of the photoresist.

2. EXPERIMENTAL CONDITIONS

We used standard R&D test wafer structures to investigate the sidewall slope of a $2.5\mu m$ thick I-line Shipley Novilac photoresist. Therefore the post development bake temperature was varied from $110°C$ to $120°C$ and $140°C$, respectively. Figures 1-3 show the different sidewall profiles for different resist patterns and post development bake temperatures. The large pattern sizes show extremely tapered edge profiles for high post development bake temperatures where dopants can easily penetrate during the subsequent ion implantation step. Figure 4 exhibits counterdoping leakage pathways within a common drain NMOS structure. By using a selective etch analysis technique the n-doped regions are displayed as ridged structures. Even the shape of small resist features are impacted by the post development bake temperature. In the $140°C$ case the small feature are melted and the surface tension forms resist spheres.

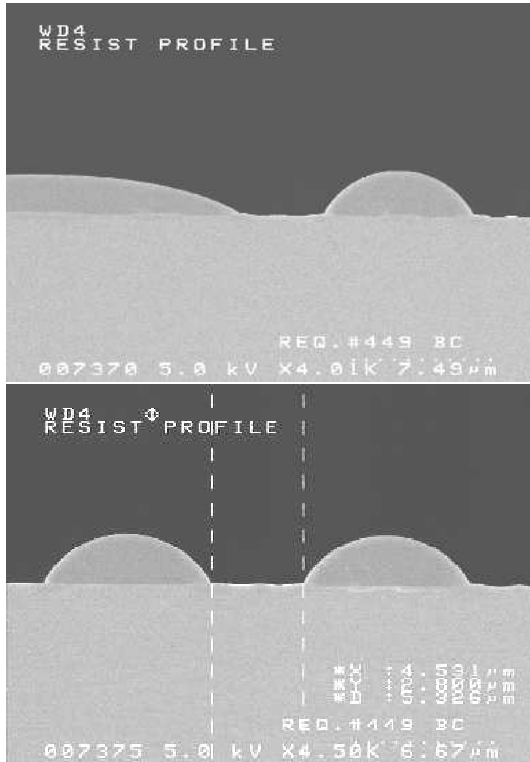

Figure 1. Resist sidewall slope for a large resist area at the edge of a high density memory cell (top) as well as within the center area (bottom) for $140°C$ bake temperature. Severe tapering of the resist mask is observed at $140°C$ bake temperature for the large resist pattern at the transition area.

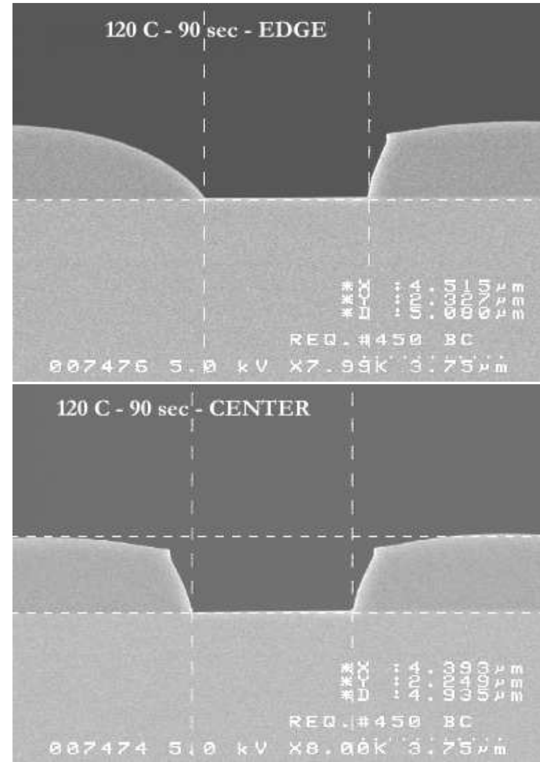

Figure 2. Resist sidewall slope for a large resist area at the edge of a high density memory cell (top) as well as within the center area (bottom) for $120°C$ bake temperature. The tapering of the resist mask is reduced at $120°C$ compared to $140°C$ bake temperature for the large resist pattern at the transition area but still unacceptable.

Figure 5 gives the temperature dependence of the sidewall slope for large as well as small resist patterns. Significant improvement is achieved when the post development bake temperature is reduced. By reducing the post development bake temperature the resist density is influenced, which makes the resist more prone to outgassing effects. To investigate the impact of the temperature reduction on the outgassing behavior of the resist the pressure change during the subsequent ion implantation as well as the sheet resistance were monitored. Both parameters did not show significant changes when the bake temperature was varied within the range of this study.

3. SIMULATION EFFORTS

We used process simulation tools [4] to validate the ion penetration through the tapered resist mask and to assess the amount of counterdoping in the channel area for the NMOS devices. Figure 6 gives the initial simulation geometries for a $120°C$ (left) and a $110°C$ post development bake temperature resist mask extracted from SEM pictures. This specific mask geometry was used to simulate the n-well implantation process by applying analytical ion implantation and dual Pearson distribution functions.

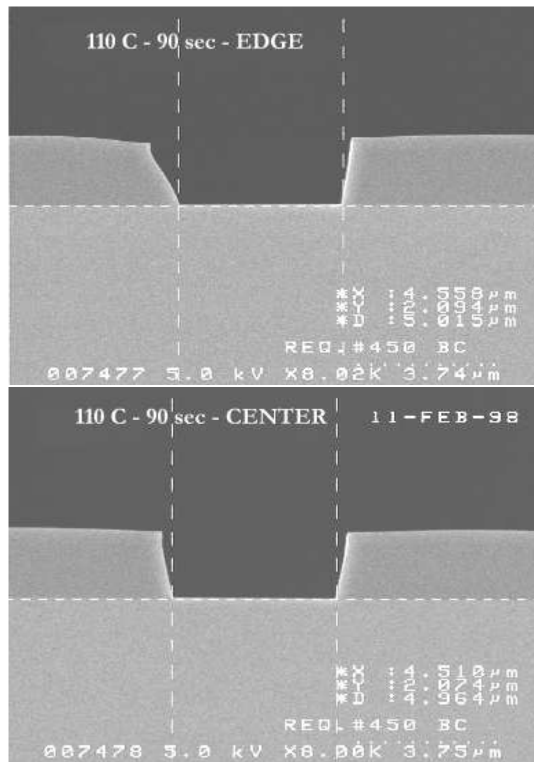

Figure 3. Resist sidewall slope for a large resist area at the edge of a high density memory cell (top) as well as within the center area (bottom) for $110°C$ bake temperature. The tapering of the resist mask is significantly reduced at $110°C$ bake temperature.

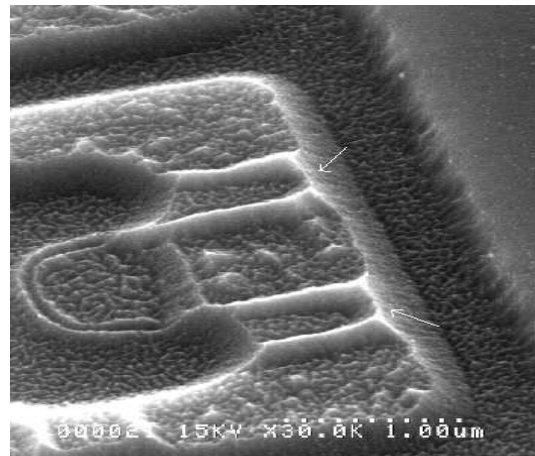

Figure 4. Selective etch analysis for a NMOS array. The ridged structures refer to n-doped regions. The arrows point to the ends of the NMOS channels, which are usually p-doped areas. The counterdoping at the channel ends is caused by resist tapering. This results in threshold voltage lowering and increased leakage current.

After performing the n-well implantation through such tapered masks the impact on the doping profile at the end of the whole fabrication process is depicted in Figure 7. The low temperature mask sample completely blocks the n-well dopant from reaching the channel area of the adjacent n-channel device while the tapered mask cannot prevent the phosphorus dopants from penetrating the n-well mask and counterdoping the n-channel device. This has a severe impact on device performance because the threshold voltage is drastically reduced and leakage currents are increased by orders of magnitude even at 0V gate bias for the n-channel transistor. Therefore, the "sloppy" resist sidewall has a detrimental effect on minimum n-well to n+ diffusion spacing. In order to further reduce isolation spacings in STI (shallow trench isolation) or LOCOS isolation structures the resist sidewalls have to be optimized to avoid counterdoping, punchthrough failures and static Idd failures. Special attention needs to be devoted to areas were pattern density changes occur. Although the resist pattern are nearly spheres in high density areas, the blocking capabilities are still sufficient to avoid counterdoping. In density transition areas (edge of memory cells or guard rings) the dopant penetration can cause severe malfunction of the peripheral devices.

4. CONCLUSIONS

The post development bake temperature has a strong impact on the final resist sidewall shape of thick photoresist layers. At high bake temperatures ($140°C$) small resist features melt and the surface tension forms surface spheres. Large resist features exhibit severe resist tapering at the corner regions. This tapering causes dopant pen-

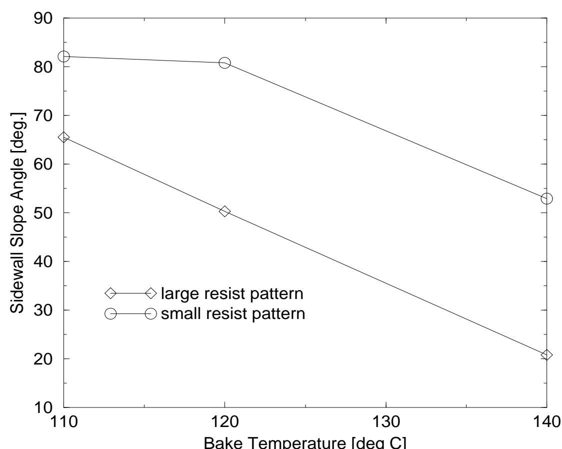

Figure 5. Sidewall slope vs. bake temperature dependence for small ($< 10\mu m$) and large ($> 50\mu m$) resist patterns. Significant improvement is achieved when the post bake temperature is reduced. All patterns were baked for 90sec.

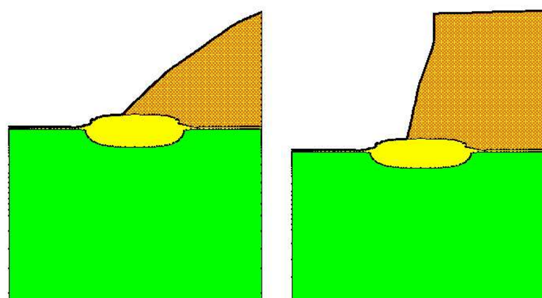

Figure 6. Simulation geometries extracted from SEM pictures for small and large n-well resist patterns used for penetration studies.

etration issues at subsequent implantation steps in the manufacturing process. In order to establish nearly perpendicular resist sidewalls for thick photoresists the post development bake temperature has to be lowered. As an alternative treatment an UV-cure process can be used to strengthen the resist patterns after development.

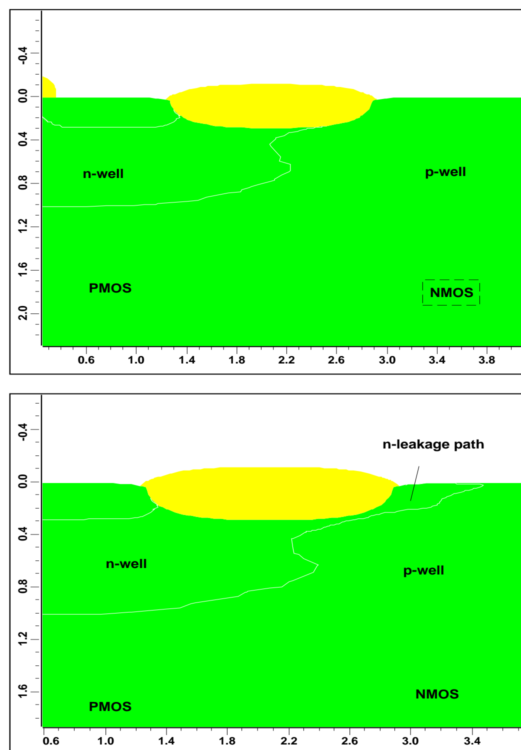

Figure 7. Final doping junctions for an inverter structure separated by a field isolation. In the tapered mask case (bottom) the n-well implant punches through the resist mask causing a static Idd failure for SRAM devices. The sample with the improve resist sidewall (top) shows no counterdoping in the NMOS area.

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