The State of the Art in Interconnect Simulation

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Abstract—**Until recently most interconnect models took into account capacitances and resistances only. With operating frequencies in the GHz regime the effect of the magnetic field can no longer be neglected. Inductances, skin effect, and transmission line behavior have to be considered carefully. For many complicated topographies, where lumped or one-dimensional distributed models do not reach the required accuracy, three-dimensional quasi-static or even full-wave models are required. Since the amount of power dissipated in the interconnect structures is increasing, thermal interconnect modeling is also gaining importance, especially for Silicon-On-Insulator chips and low-k materials. We shall demonstrate how simulation tools keep pace with these demands.**

I. Introduction

In modern deep submicron VLSI circuits interconnects play an increasingly important role. Due to the steady increase in device speed and clock frequencies in the GHz regime the influence of the interconnects parasitics on circuit behavior becomes significant, sometimes even dominant. Hence, highly accurate interconnect analysis has become essential.

In the 1980's interconnect line widths were around 1 μm and their resistance was not a major concern. The line was modeled as a single lumped capacitor, with a capacitance value proportional to the area of the wire (plate capacitor model). Because the aspect ratio of the wires was low, coupling between adjacent wires could be neglected. As the line widths got smaller the resistance of the interconnects increased and had to be considered during circuit simulation. The signal delay was calculated with a single RC time constant (Elmore delay). More accurate capacitance models had to be developed, that included fringing fields. With high aspect ratios, crosstalk between neighboring lines becomes significant and has to be implemented in the models. Taking into account the distributed nature of the capacitance and resistance, extraction of coupled RC-networks with many lumps has become necessary. Inductance has been considered in printed circuit board and package design for a long time. With higher frequencies transmission line effects occur, hence, inductance of on-chip interconnects can no longer be neglected. This is especially true for long interconnect lines as used for clock and power distribution, global busses, and other long low-resistance interconnects optimized for high performance. Although global interconnects represent only a small percentage of the total wiring, many of these nets are "critical paths" and the delay on these lines has a direct influence on the system cycle time. More complex models for delay and impedance have been developed, that account for self-inductance and inductive cross-talk. As the wave-lengths of the signals reach the geometric feature sizes of the interconnects, quasi-static simulation becomes too inaccurate and full-wave models are required. The gap between digital and microwave designs is becoming narrow.

Higher current densities make the interconnects vulnerable to electromigration which has to be considered during the design and verification process. A significant amount of the total power is dissipated in the interconnects. Therefore, also thermal interconnect models are needed to prevent elevated temperature and guarantee system reliability.

II. Interconnect Modeling

Parasitic interconnect effects, like attenuation caused by resistive voltage drops, delay times, crosstalk (caused by capacitive or inductive coupling or by the substrate), reflections incurred by discontinuities, skin-effect, eddy currents (e.g. in spiral inductors) and electromagnetic radiation can be characterized by calculating the electric and magnetic fields. This is done by solving Maxwell's equations or some simplification thereof, either in time- or frequency domain. Time domain models can easily include non-linear parts of the system and are commonly used in circuit simulators (e.g. SPICE). The computation time is proportional to the period of time that has to be simulated and the maximum frequency. Therefore these methods get inefficient when very high frequencies occur. It is not possible to consider frequency dependent material properties (permittivity) with time domain methods. On the other hand, frequency domain models cannot handle strong nonlinearities.

The conventional approach to model the interconnects parasitics is to extract global electric parameters (resistance, capacitance, inductance) and build a lumped model that approximates the characteristics of the interconnect to a certain extent. This model then can be evaluated with a circuit simulator like SPICE. With higher operating frequencies more accurate results can be obtained with distributed models in one (transmission lines) or three dimensions.

III. Parasitics Extraction

Accurate parameter extraction is key for a successful simulation. An immense number of such extraction methods have been reported in the literature—the next subsections shall give a short summary.

A. Capacitance Extraction

Capacitances can either be calculated analytically, which is only possible for very simple structures (e.g an infinitely long straight line over a ground plane [1]), with geometric models or pattern matching methods which are very fast, but inaccurate for complex geometries with many layers [2–6], or with numerical

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methods based on the solution of the Laplace equation, which have naturally a higher CPU-time and memory consumption.

The two most popular numerical techniques are the boundary element method (BEM) and the finite element method (FEM). The BEM [7–9] uses an integral formulation based on Green's functions. It results in a small but full system matrix and is most efficient for regular stratified dielectrics. Acceleration is possible with the multipole method or by neglecting the influence of far apart conductors [10–12].

The FEM [13] discretization gives a large, but sparse matrix. Therefore fast, iterative solvers usually are applied. It is most flexible and exhibits a good numerical stability.

A combination of BEM and FEM, the so-called hybrid method, combines the advantages of both [14]. Areas with stratified layers are calculated with the BEM, for non-planar regions the FEM is used. Special care must be taken at the interfaces.

Another approach to combine the advantages of volume oriented methods like FEM and the boundary element method is called measured equation of invariance. This method achieves a small but also sparse system matrix. The numeric effort is dominated by the evaluation of Green's functions. A speedup can be obtained by a variant, called geometry independent measured equation of invariance [15].

Capacitance can also be calculated with stochastic techniques, like the random walk method [16, 17]. It's low memory consumption makes it suitable for full-chip extraction.

B. Resistance Extraction

The interconnect resistance can either be approximated with polygonal decomposition models [18] (e.g. by "counting squares"), or calculated numerically with FEM. Here, the FEM seems to be most accurate and robust, however at the cost of a higher computational effort. Speedups can be obtained by optimizing the elimination order of the Gaussian solver [19] and by introducing articulation nodes [20].

C. Substrate Resistance

Crosstalk can be caused by coupling over the substrate. Therefore it is necessary to extract the substrate resistance. Coupling to the substrate can be caused by the bulk contact of transistors, diffused resistors, interconnects with a large substrate capacitance, or noisy supply lines with substrate contacts. Sensitive parts of the circuit may be influenced, especially in mixed-signal applications. Substrate resistance calculation is also performed with FEM, BEM [21–23] or geometric models [24].

D. Inductance Extraction

Strictly speaking inductance is defined only for closed current loops. Therefore the inductance of a wire depends on the current return path (and thereby on the signal frequency) which may be unknown. Assuming that the return-path is in the substrate gives at least a worst-case estimation. Another approach is the definition of partial inductances, where an infinitely far return path is assumed. Partial inductances may be included into circuit simulations, but will increase the system matrix size significantly.

Most inductance calculation methods are based on a numeric solution of the integration of Neumann's formula for a precalculated current density distribution. The current density is calculated either statically by solving the Poison equation, or in time-harmonic domain. The integration can either be carried out analytically for simple geometries, numerically, where special attention has to be paid on the singularities of the integrand [25], with the Monte Carlo method [26], or by calculating directly the magnetic vector potential [27].

The partial element equivalent circuit (PEEC) method can be used for inductance-only extraction as well as for combined RLC extraction [28–31].

If execution speed is not the major concern simulators based on the FEM reach the highest flexibility since they may be applied for nonlinear, inhomogeneous problems and achieve high accuracy for all above given applications.

IV. Transmission Line Models

For certain applications lumped models based on extracted parameters are not adequate to describe the circuit behavior and the coupled system must be examined. For long low-resistance interconnects in TEM or quasi TEM configurations transmission line models based on the telegraph equation do a good job [32, 33]. These models rely on the distributed resistance, capacitance, inductance, and conductance of the line. For higher frequencies skin effect may occur and these parameters get frequency dependent [34, 35]. When the inductivity is neglected the telegraph equation becomes an diffusion equation and the solution can be calculated in time domain analytically [36]. The transmission line model can be extended to include crosstalk between multiple lines or lines over lossy substrate [37]. Transmission line models are usually evaluated in the frequency domain. For practical applicability in circuit simulations approximations in time domain can be derived [38–40].

V. Three-Dimensional Analysis

For most accurate results Maxwell's equations have to be solved in three dimensions. Depending on the problem certain simplifications can be made: *Quasi-electrostatic simulation* can be applied when the effects of the magnetic field can be ignored (i.e. the resistance dominates over inductance). Therefore the electric field is assumed to be irrotational and is expressed by a scalar potential. *Quasi-magnetostatic simulation* is used when the capacitive displacement current can be neglected (i.e. inductance dominates over capacitance). This approach is commonly used for the calculation of inductances under the influence of the skin-effect. *Quasi-static simulation* combines the first two methods. Only the time-derivative of the electric displacement is neglected in the first of Maxwell's equation. Thereby a formation of electromagnetic waves is not possible. This method is applicable when the geometric dimensions of the simulated structure are small compared to the wavelength in the direction

perpendicular to the signal propagation. All of the above simulation modes can be expressed by Poisson equations, which can be solved with finite element or finite difference discretization schemes.

Full-wave simulation takes the complete set of Maxwell's equations into account. Usually the equations are solved in the frequency domain. Time domain solutions are possible but may lead to numeric instabilities and boundary conditions may be difficult to model, especially for radiation. The method is very CPU intensive and only small parts of the layout can be simulated. Hybrid methods based on model-reduction techniques [41] have a better performance.

VI. Model-Order Reduction

The discretization of three-dimensional partial differential equations leads to a large algebraic system which cannot efficiently be incorporated into a circuit simulation. Its representation must be considerably compressed through reduced order modeling techniques to generate a macromodel with a lower complexity. The reduced order model should capture with sufficient accuracy the input-output behavior of the original system in the desired frequency range and should have efficient representations in both time and frequency domains. Model-order reduction is usually performed by projecting the system matrices into smaller "sub-spaces" e.g. by Padé approximation [42, 43]. These methods do not maintain passivity of the reduced model. A general method for obtaining passive reduced order macromodels is presented in [44].

Model-order reduction techniques may only be applied to linear systems. They are only necessary if numerous simulation runs are required, since their numerical effort is comparable to or larger than one direct solution of the full system.

VII. Reliability

Reduced wire cross-sections imply higher current densities resulting in an increasing power-loss density and thus higher temperatures. Thermal simulation becomes necessary to find a limit for the maximum current in a wire [45]. This is especially important for low-k materials which have a smaller thermal conductivity than oxide and for Silicon-On-Insulator chips, since the heat transfer through the insulating oxide causes increased temperature [46]. Thermal simulations are of utmost importance for electrostatic discharge protection circuits [47].

To calculate the temperature profile the heat conduction equation has to be solved numerically. Adiabatic approximations are only possible for very short pulses ($t < 10$ ns) [48]. For accurate simulation of the steady state temperature the simulation area has to be rather large. If the chip is not mounted directly on a good thermal conductor it may be necessary to include package and pins [49].

Analytic thermal models can be developed for certain structures [50] but must be calibrated by numeric simulation.

To include thermal models in circuit simulation it is possible to simulate a thermal circuit, where temperature is replaced by a voltage and heat flow by an electric current. Similar to the calculation of electrical resistances and capacitances also thermal resistances and capacitances can be extracted [51].

Interconnects exposed to high current densities for a long time (e.g. power supply lines) are susceptible to electromigration. Electromigration is a complex directional diffusion process whose driving force is the current density, but depends on many other factors, e.g. temperature, mechanical stress [52], line length and cross-section. Simple electromigration models are based on Black's equation [53]. They have to be calibrated with experiments and are only reproducible for similar geometric structures. Atomistic models are computationally very expensive and depend on some poorly known factors (e.g. location of grain boundaries). Therefore, they cannot be used for layout verification purposes. Practical and accurate electromigration models are still an unsettled issue.

VIII. Design

Interconnect parasitics extraction is most important for post layout verification. Simple geometric models are sufficient in most cases. Only for "critical nets" highly accurate three-dimensional simulation is required. However, with higher clock frequencies and increasing total interconnect length also the number of critical nets increases and the need for highly accurate models will become more evident.

The correction of the errors detected during the post layout verification process may introduce new errors that have to be corrected again. As the number of critical nets rises it is more likely that errors occur and the rerouting/verification loop has to be repeated many times, which will make the design process inefficient and costly. Therefore the parasitics of the interconnects have to be considered during the design phase at the earliest possible stage, e.g. device placement and routing. Since at this stage the full topographic information of the interconnect stack is not yet available, the models have to make certain assumptions based on statistical information. These models should give an estimate of the delay caused by the interconnects and their impedance. Optimization should be performed on minimum signal delay during placement, and the driver sizes must also be tuned to minimize delay and to prevent ringing. For global interconnects the signal delay can also be reduced by the insertion of buffers [54–57].

IX. Software

Basic requirements for practically useful simulation software are stability and accuracy. The accuracy must be known and controllable (runtime/accuracy tradeoff).

Therefore the interconnect simulators should automatically identify critical nets and select appropriate models. To reduce the required CPU time the simulation domain can be divided into several regions applying models of different complexity according to the necessity on accuracy. The challenging task is to develop a general algorithm for automatizing this partitioning process and to find suitable models for the interfaces [58, 59],

because high frequencies cause complex interaction between structures, that traditionally could be analyzed separately.

Commercial TCAD vendors present a wide range of solutions for interconnect simulations. These tools (e.g. [60–63]) provide R(L)C extraction, SPICE netlist generation, Poisson equation solvers and furthermore some features as e.g. simple electromigration models [64] are also offered.

X. Application Examples

Simulations are performed with the program package Smart Analysis Programs [65]. We present the analysis of a double layered spiral inductor with the following dimensions: area = 226 x 262 μm, metal width = 18 μm, wirespacing = 18 μm, the height of the spiral inductor and the distance between the two layers amount 2.7 μm. The magnetic field of the spiral inductor (Fig. 1) was calculated with the magnetostatic vector potential. Additionally, the inductance was computed by evaluation of the Neumann formula resulting in 5.62 nH.

In Fig. 2 an example of a via structure with actual Cu-Ti layout is shown. The hottest spot (T = 367 K) is detected on the rightmost via, where the highest current density is observed, near the TiN-barrier. The high resistivity of the TiN barrier causes a large voltage drop at the bottom of the W-plug resulting in a high heat generation rate [66]. The bottom of the Si-substrate is kept at constant temperature of 24°C.

XI. Conclusion

In summary we can find three starting points for further reducing and controlling parasitic effects namely design, simulation, and materials.

During the design new routing strategies that better account for transmission line effects, the introduction of ground planes or shielding wires will help to control on-chip inductive effects.

New simulation methods are required that are more accurate, efficient, robust, and flexible.

The migration from Aluminum to Copper lowers the interconnect resistivity by 40 % [67]. Together with the introduction of low-k dielectrics the RC time constant can be reduced by a factor of 6. However, decreased resistance and capacitance will bring out inductive effects more intensively, thus increasing the importance of numerical inductance extraction methods.

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References

[1] A. Ringhandt and H. Wagemann, "An exact calculation of the two-dimensional capacitance of a wire and a new approximation formula", *IEEE Trans.Electron Devices*, vol. 40, no. 5, pp. 1028–1032, 1993.

[2] A. Ruehli and P. Brennan, "Capacitance models for integrated circuit metallization wires", *IEEE J.Solid-State Circuits*, vol. SC-10, no. 6, pp. 530–536, 1975.

[3] P. Wright and Y. Shih, "Capacitance of top leads metal–comparison between formula, simulation, and experiment", *IEEE Trans.Computer-Aided Design*, vol. 12, no. 12, pp. 1897–1902, 1993.

[4] U. Choudhury and A. Sangiovanni-Vincentelli, "Automatic generation of analytical models for interconnect capacitances", *IEEE Trans.Computer-Aided Design*, vol. 14, no. 4, pp. 470–480, 1995.

[5] N. Arora, K. Raol, R. Schumann, and L. Richardson, "Modeling and extraction of interconnect capacitances for multilayer VLSI circuits", *IEEE Trans.Computer-Aided Design*, vol. 15, no. 1, pp. 58–67, 1996.

[6] S.-C. Wong, P. S. Liu, J.-W. Ru, and S.-T. Lin, "Interconnect capacitance models for VLSI circuits", *Solid-State Electronics*, vol. 42, no. 6, pp. 696–977, 1998.

[7] K. Nabors and J. White, "Fastcap: A multipole accelerated 3-D capacitance extraction program", *IEEE Trans.Computer-Aided Design*, vol. 10, no. 11, pp. 1447–1459, 1991.

[8] F. Beeftink, A. J. van Genderen, N. P. van der Meijs, and J. Poltz, "Deep-submicron ULSI parasitics extraction using Space", in *Design, Automation and Test in Europe Confere, Designer Track*, 1998, pp. 81–86.

[9] M. W. Beattie and L. T. Pileggi, "Bounds for BEM capacitance extraction", in *Proc. 34rd Design Automation Conference*, Anaheim, CA, USA, 1997, pp. 133–136, ACM.

[10] J. Tausch and J. White, "Multipole accelerated capacitance calculation for structures with multiple dielectrics with high permittivity ratios", in *Proc. 33rd Design Automation Conference*, Las Vegas, NV, USA, 1996, ACM.

[11] U. Geigenmuller and N. P. van der Meijs, "Cartesian multipole based numerical integration for 3D capacitance extraction", in *Proc. European Design and Test Conf.*, 1997, pp. 256–259.

[12] M. Bächtold, J. G. Korvink, and H. Baltes, "Enhanced multipole acceleration technique for the solution of large Poisson computations", *IEEE Trans.Computer-Aided Design*, vol. 15, no. 12, pp. 1541–1546, 1996.

[13] A. Hieke, "Simple ADPL implementation of a 3D FEM simulator for mutual capacitances of arbitrary shaped objects like interconnects", in *Proc. 2nd Int. Conf. on Modeling and Simulation of Microsystems*, San Juan, Puerto Rico, USA, 1999, pp. 172–175.

[14] E. B. Nowacka and N. P. van der Meijs, "The hybrid element method for capacitance extraction in a VLSI layout verification system", in *Proc. Software for Electrical Engineering Analysis and Design*, P. P. Silvester, Ed., Pisa, Italy, 1996, pp. 125–134, Computational Mechanics Publications.

[15] W. Sun, W. W.-M. Dai, and W. Hong, "Fast parameters extraction of general three-dimension interconnects using geometry independent measured equation of invariance", in *Proc. 33rd Design Automation Conference*, Las Vegas, NV, USA, 1996, ACM.

[16] Y. Le Coz and R. Iverson, "A stochastic algorithm for high speed capacitance extraction in integrated circuits", *Solid-State Electron.*, vol. 35, no. 7, pp. 1005–1012, 1992.

[17] Y. Le Coz and R. Iverson, "A high-speed capacitance extraction algorithm for multi-level vlsi interconnects", in *VLSI Multilevel Interconnection Conf.*, Santa Clara, CA, 1991, pp. 364–366, IEEE.

[18] M. Horowitz and R. W. Dutton, "Resistance extraction from mask layout data", *IEEE Trans.Computer-Aided Design*, vol. CAD-2, no. 3, pp. 145–150, 1983.

[19] N. P. van der Meijs and A. J. van Genderen, "Delayed frontal solution for finite-element based resistance extraction", in *Proc. 32rd Design Automation Conference*, San Francisco, California, 1995, pp. 273–278, ACM.

[20] A. J. van Genderen and N. P. van der Meijs, "Using articulation nodes to improve the efficiency of finite-element based resistance extraction", in *Proc. 33rd Design Automation Conference*, Las Vegas, NV, USA, 1996, pp. 758–763, ACM.

[21] T. Smedes, "A boundary element method for substrate cross-talk analysis", in *Proc. ProRISC/IEEE Benelux Workshop on Circuits, Systems and Signal Processing*, Mierlo, The Netherlands, 1995, pp. 285–294.

[22] A. J. van Genderen, N. P. van der Meijs, and T. Smedes, "Fast computation of substrate resistances in large circuits", in *Proc. European Design and Test Conf.*, Paris, France, 1996, pp. 560–565.

[23] T. Li, C.-H. Tsai, E. Rosenbaum, and S.-M. Kang, "Substrate modeling and lumped substrate resistance extraction for CMOS ESD/latchup circuit simulation", in *Proc. 35th Design Automation Conference*, New Orleans, Louisiana, 1999, pp. 549–554, ACM.

[24] T. A. Johnson, R. W. Knepper, V. Marcello, and W. Wang, "Chip substrate resistance modeling technique for integrated circuit design", *IEEE Trans.Computer-Aided Design*, vol. 3, no. 2, pp. 126–134, 1984.

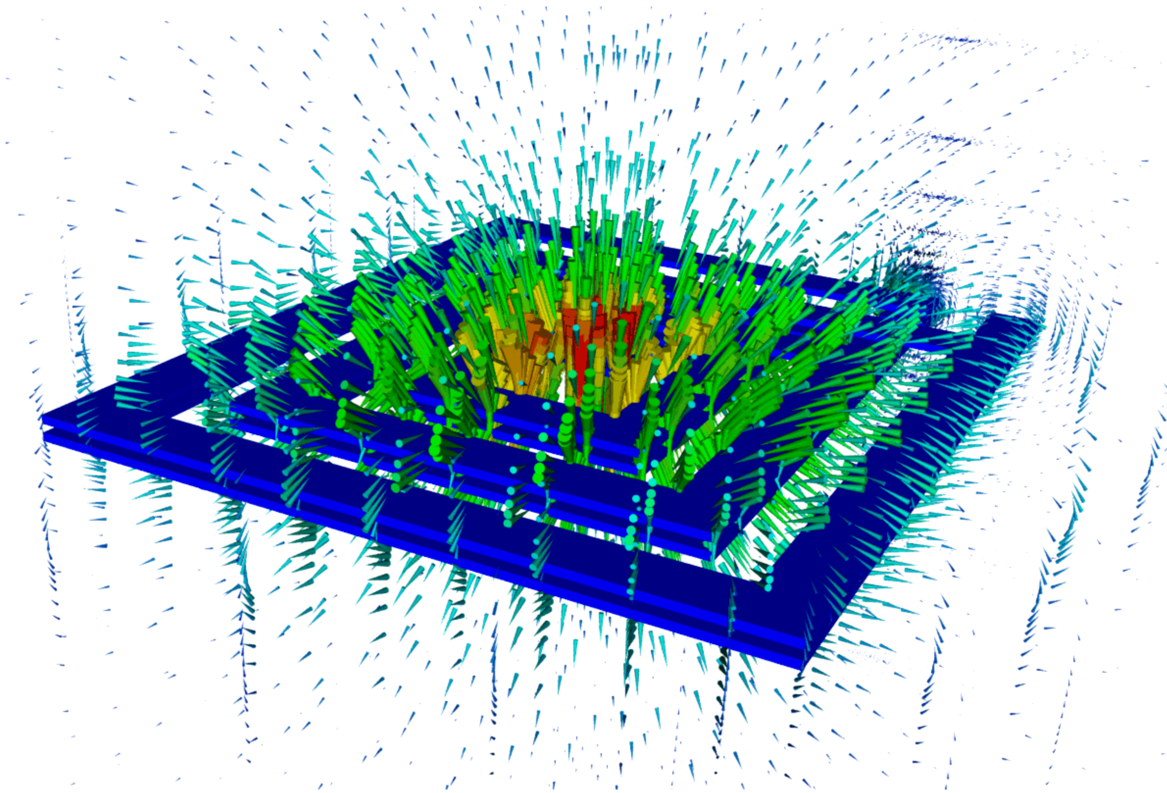

Fig. 1. Magnetic field around a spiral inductor.

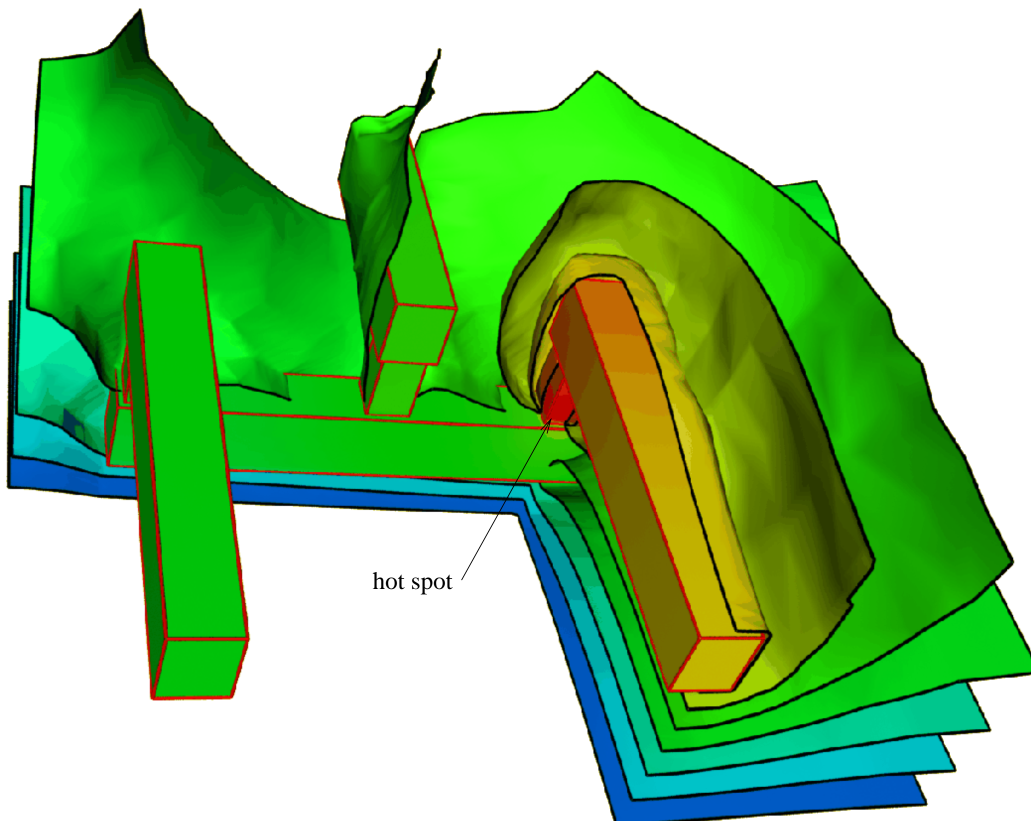

Fig. 2. Thermal analysis of a via structure. The temperature is shown on the surface of the interconnects and as contour faces in the dielectric.

[25] C. Harlander, R. Sabelka, and S. Selberherr, "Inductance calculation in interconnect structures", in *Proc. 3rd Int. Conf. on Modeling and Simulation of Microsystems*, San Diego, California, USA, 2000, pp. 416–419.

[26] G. Leonhardt and W. Fichtner, "Acceleration of inductance extraction by means of the monte carlo method", in *Proc. 2nd Int. Conf. on Modeling and Simulation of Microsystems*, San Juan, Puerto Rico, USA, 1999, pp. 147–150.

[27] P. Böhm and G. Wachutka, "Transient electromagnetic behvior of multiply contacted interconnect", in *Proc. 2nd Int. Conf. on Modeling and Simulation of Microsystems*, San Juan, Puerto Rico, USA, 1999, pp. 301–304.

[28] H. Heeb and A. E. Ruehli, "Three-dimensional interconnect analysis using partial element equivalent circuits", *IEEE Trans.Circuits and Systems–I: Fundamental Theory and Applications*, vol. 39, no. 11, pp. 974–982, 1992.

[29] P. Restle, A. Ruehli, and S. G. Walker, "Dealing with inductance in high-speed chip design", in *Proc. 35th Design Automation Conference*, New Orleans, Louisiana, 1999, pp. 904–909, ACM.

[30] Y. Cao, Z.-F. Li, J.-F. Mao, and J.-F. Mao, "A PEEC with a new capacitance model for circuit simulation of interconnects and packaging structure", *IEEE Trans.Microwave Theory and Techniques*, vol. 48, no. 2, pp. 281–287, 2000.

[31] J. Cullum, A. Ruehli, and T. Zhang, "A method for reduced-order modeling and simulation of large interconnect circuits and its application to PEEC models with retardation", *IEEE Trans.Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 47, no. 4, pp. 261–273, 2000.

[32] A. Deutsch, G. V. Kopcsay, V. A. Ranieri, J. K. Cataldo, E. A. Galligan, W. S. Graham, R. P. McGouey, S. L. Nunes, J. R. Paraszczak, J. J. Ritsko, R. J. Serino, C. Shih, and J. S. Wilczynski, "High-speed signal propagation on lossy transmission lines", *IBM J.Res.Dev.*, vol. 34, no. 4, 1990.

[33] A. Deutsch, G. V. Kopcsay, C. W. Surovic, B. J. Rubin, L. M. Terman, R. P. Dunne, Jr., T. A. Gallo, and R. H. Dennard, "Modeling and characterization of long on-chip interconnections for high performance microprocessors", *IBM J.Res.Dev.*, vol. 39, no. 5, pp. 547–567, 1995.

[34] L.-F. Chang, K.-J. Chang, and C. Bianchi, "A proposal for accurately modeling frequency-dependant on-chip", in *First International Symposium on Quality Electronic Design*, 2000, pp. 375–377.

[35] A. Deutsch, H. Smith, C. Surovic, G. Kopcasy, D. Webber, P. Coteus, G. Katopis, W. Becker, A. Dansky, G. Sai-Halasz, and P. Restle, "Frequency-dependent crosstalk simulation for on-chip interconnections", *IEEE Trans.Advanced Packaging*, vol. 22, no. 3, pp. 292–308, 1999.

[36] A. B. Kahng and S. Muddu, "Delay analysis of VLSI interconnections using the diffusion equation model", in *Proc. 31rd Design Automation Conference*. 1994, pp. 563–569, ACM.

[37] E. Tuncer and D. P. Neikirk, "Highly accurate quasi-static modeling of microstrip lines over lossy substrates", *IEEE Microwave and Guided Wave Lett.*, vol. 2, pp. 409–411, 1992.

[38] A. B. Kahng, K. Masuko, and S. Muddu, "Analytical delay models for VLSI interconnects under ramp input", in *Proc. Int. Conf. Computer Aided Design*, San Jose, CA, USA, 1996, IEEE.

[39] Q. Xu, Z.-F. Li, P. Mazumder, and J.-F. Mao, "Time-domain modeling of high-speed interconnects by modified method of characteristics", *IEEE Trans.Microwave Theory and Techniques*, vol. 48, no. 2, pp. 323–327, 2000.

[40] N. Lu and I. Hajj, "An exact analytical time-domain model of distributed rc interconnects for high speed nonlinear circuit applications", in *Proc. Ninth Great Lakes Symposium on VLSI*, 1999, pp. 68–71.

[41] T. Watanabe and H. Asai, "Synthesis of time-domain models for interconnnects having 3-D structure based on FDTD method", *IEEE Trans.Circuits and Systems–II: Analog and Digital Signal Processing*, vol. 47, no. 4, pp. 302–305, 2000.

[42] P. J. H. Elias, "Efficient moments extraction from VLSI interconnections", in *Proc. ProRISC/IEEE Benelux Workshop on Circuits, Systems and Signal Processing*, Mierlo, The Netherlands, 1995, pp. 83–90.

[43] P. J. H. Elias and N. P. van der Meijs, "Efficient moments extraction of large inductively coupled interconnection networks", in *Proc. Int. Symposium on Circuits and Systems*, Atlanta, Georgia, 1996, vol. 4, pp. 540–543, IEEE.

[44] A. Odabasioglu, M. Celik, and L. T. Pileggi, "PRIMA: passive reduced-order interconnect macromodeling algorithm", *IEEE Trans.Computer-Aided Design of Integrated Circuits and Systems*, vol. 17, no. 8, pp. 645–654, 1998.

[45] K. Banerjee, A. Mehrotra, A. Sangiovanni-Vincentelli, and C. HU, "On thermal effects in deep sub-micron VLSI interconnects", in *Proc. 35th Design Automation Conference*, New Orleans, Louisiana, 1999, pp. 885–891, ACM.

[46] Z. Kohári, V. Székely, M. Rencz, V. Dudek, and B. Höfflinger, "Studies on the heat removal features of stacked SOI structures with a dedicated field solver program (SUNRED)", in *27th European Solid-State Device Research Conference*, H. Grünbacher, Ed., Stuttgart, Germany, 1997, Editions Frontieres.

[47] K. Banerjee, A. Amerasekera, N. Cheung, and C. Hu, "High-current failure model for VLSI interconnects under short-pulse stress conditions", *IEEE Electron Device Lett.*, vol. 18, no. 9, pp. 405–407, 1997.

[48] X. Gui, S. Dew, and M. Brett, "Thermal simulation of thin-film interconnect failure caused by high current pulses", *IEEE Trans.Electron Devices*, vol. 42, no. 7, pp. 1386–1388, 1995.

[49] G. Digele, S. Lindenkreuz, and E. Kasper, "Electro-thermal interaction on circuit level under the influence of packaging", in *27th European Solid-State Device Research Conference*, H. Grünbacher, Ed., Stuttgart, Germany, 1997, Editions Frontieres.

[50] P. Waltz, G. Lormand, and L. Arnaud, "Thermal analytical model for analysis of pulsed DC electromigration results", in *27th European Solid-State Device Research Conference*, H. Grünbacher, Ed., Stuttgart, Germany, 1997, Editions Frontieres.

[51] B. Krabbenborg, A. Bosma, H. de Graaff, and A. Mouthaan, "Layout to circuit extraction for three-dimensional thermal-electrical circuit simulation of device structures", *IEEE Trans.Computer-Aided Design*, vol. 15, no. 7, pp. 765–774, 1996.

[52] J. Coughlan, S. Foley, and A. Mathewson, "Finite element analysis of stress distributions in interconnect structures", in *27th European Solid-State Device Research Conference*, H. Grünbacher, Ed., Stuttgart, Germany, 1997, Editions Frontieres.

[53] J. R. Black, "Electromigration—A brief study and some recent results", *IEEE Trans.Electron Devices*, vol. 16, pp. 338–347, 1969.

[54] J. Cong, L. He, C.-K. Koh, and Z. Pan, "Global interconnect sizing and spacing with consideration of coupling capacitance", in *Proc. Int. Conf. Computer Aided Design*. 1997, pp. 478–485, IEEE.

[55] S. S. Sapatnekar, "Wire sizing as a convex optimization problem: Exploring the area-delay tradeoff", *IEEE Trans.Computer-Aided Design*, vol. 15, no. 1, pp. 1001–1011, 1996.

[56] K. Rahmat, O. S. Nakagawa, S.-Y. Oh, and J. Moll, "A scaling scheme for interconnect in deep-submicron processes", in *Proc. IEDM*, 1995, pp. 245–248.

[57] K. D. Boese, J. Cong, K. S. Leung, A. B. Kahng, and D. Zhou, "On high-speed VLSI interconnects: Analysis and design", in *Proc. IEEE Asia-Pacific Conf. on Circuits and Systems*, 1992, pp. 35–40.

[58] R. W. Dutton, "The role of TCAD in parasitic analysis of IC's", in *23rd European Solid State Device Research Conference - ESSDERC'93*, J. Borel, P. Gentil, J. Noblanc, A. Nouailhat, and M. Verdone, Eds., Gif-sur-Yvette Cedex, France, 1993, pp. 75–81, Editions Frontieres.

[59] E. Chiprout, "Hierachical interconnect modeling", in *Int.Electron Devices Meeting*, 1997, pp. 125–128.

[60] ISE - Integrated Systems Engineering, "Solidis", `http://www.ise.com/products/index.htm`.

[61] OptEM Engineering Inc., "Inspector - Interconnect optimization and EM analysis", `http://www.optem.com/products/inspector.html`.

[62] Silvaco International, "Tempest - Interconnect parasitic extraction tools", `http://www.silvaco.com/products/tempest/tempest.html`.

[63] Cray Research Inc., "LC - An electromagnetic analysis tool", `http://lc.cray.com/lc/ug/`.

[64] Avant!, "Star-power", `http://www.avanticorp.com`.

[65] R. Sabelka, R. Martins, and S. Selberherr, "Accurate layout-based interconnect analysis", in *Simulation of Semiconductor Processes and Devices*, K. D. Meyer and S. Biesemans, Eds., pp. 336–339. Springer, Leuven, Belgium, 1998.

[66] C. Harlander, R. Sabelka, R. Minixhofer, and S. Selberherr, "Three-dimensional transient electro-thermal simulation", in *5th THERMINIC Workshop*, Rome, Italy, 1999, pp. 169–172.

[67] A. K. Stamper, M. B. Fuselier, and X. Tian, "Advanced wiring RC delay issues for sub-0.25-micron generation CMOS", in *Proc. Intl. Interconnect Technology Conference*, Burlingame, California, 1998, pp. 62–64.