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A finite element simulator for three-dimensional analysis of interconnect structures

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Abstract

We have developed a set of simulation programs for two- and three-dimensional transient analysis of ULSI interconnects. The program package is called "Smart Analysis Programs" (SAP) and it supports capacitance and resistance extraction, quasi-electrostatic simulation (calculation of delay times and crosstalk), and coupled electro-thermal simulations. For the numerical solution of the involved partial differential equations (Euler equation, Poisson equation, heat conduction equation), we apply the finite element method. Also available are a set of tools for construction of the input geometry, importing layout files, layout parameterization, automatic grid generation, postprocessing, and visualization of the simulated results. The simulators have been successfully used in various applications. Two representative examples are presented. In the first application, we calculate the resistance of a via in a copper dual damascene process and analyze the temperature and current density distributions. The second example is a matched polysilicon resistor pair. Here the delay time, crosstalk effects, and the mismatch in the resistances caused by self-heating due to high current is investigated. © 2001 Elsevier Science Ltd. All rights reserved.

Keywords: Partial differential equation solvers; Finite element method; Interconnect analysis; Capacitance; Resistance; Electro-thermal simulation

1. Introduction

In deep submicron ULSI designs the overall circuit behavior is significantly determined by the interconnect structure [1]. Due to the steady increase in device speed, clock frequencies reached the GHz regime. The delay caused by the parasitic resistance and capacitance of interconnect lines thus becomes one of the most critical design issues. Additionally, the reduced line width and line spacing make the local interconnects extremely sensitive to crosstalk since the capacitive coupling is increased. Crosstalk is also caused by the substrate resistance which is specifically severe for low-power and mixed-signal integrated circuits.

One possibility to reduce the parasitic interconnect effects is the introduction of new materials, i.e. materials with high conductivity and low dielectric constant are searched for. However, the physical limits will be reached soon [2,3]. An alternative is improved design strategies (like wave pipelining) that incorporate more aggressive design rules and reduced safety margins. For that, electrical models are essential to predict interconnection delay and circuit performance. Especially for designs close to the physical limits these models have to provide highly accurate results.

Careful investigations during the design phase are of utmost importance regarding circuit reliability. The knowledge of the current density and temperature distribution in the wiring structures is crucial to prevent electromigration. However, experimental measurements of these physical effects are expensive, time consuming, inaccurate, or simply impossible (especially on chip). For these reasons numerical calculations have become increasingly important and are nowadays a well-established aid in IC manufacturing.

Conventional ECAD tools supply geometrical models for capacitance and resistance extraction. Such models [4–9] are very fast and quite accurate for simple geometries. However, for more complex structures these models are often too inaccurate. Better results can be obtained with extraction methods based on the calculation of the three-dimensional (3D) electric field.

Various approaches were reported in the literature for accurate capacitance and resistance extraction. They include the *finite difference* method [10,11], the *boundary element* method [12–14], the *finite element* method (FEM) [15], a *hybrid element* method [16], a *stochastic* method [17], and the *measured equation of invariance* method [18].

There is also an increasing need for accurate chip

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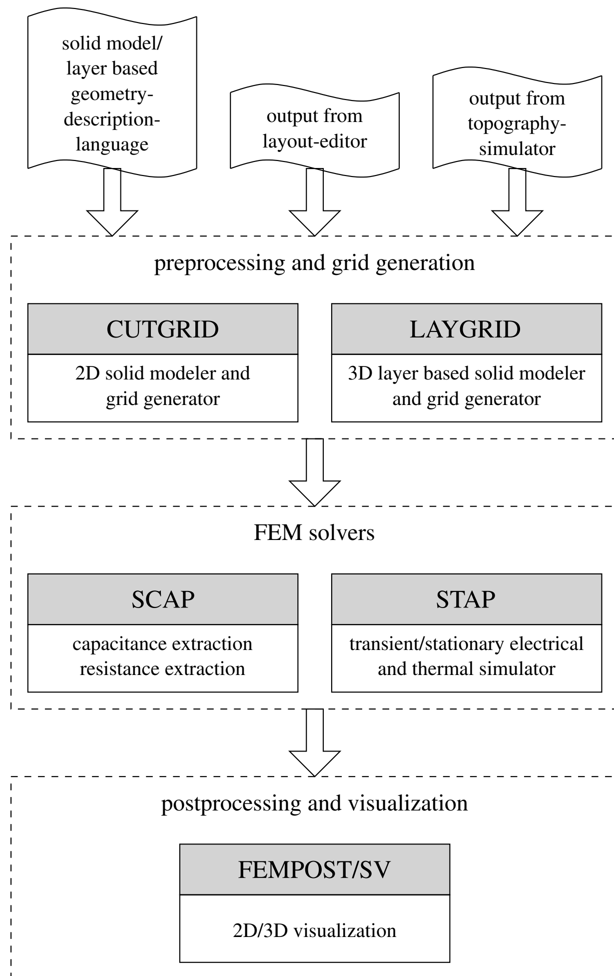

Fig. 1. Tools and data flow in the "Smart Analysis Programs".

substrate modeling. This topic is particularly important in densely packed ULSI designs, low-power, and mixed-signal circuits. For the calculation of the substrate resistance the boundary element method is very efficient [19,20].

Reduced wire cross-sections imply higher current densities resulting in an increasing power-loss density and thus higher temperatures. Thermal simulation becomes necessary to find a limit for the maximum current in a wire [21]. This is especially important for low-k materials, which have a smaller thermal conductivity than oxide and for Silicon-On-Insulator chips, since the heat transfer through the insulating oxide causes increased temperature [22]. Thermal simulations are of utmost importance for electrostatic discharge protection circuits [23]. For coupled electrical and thermal simulation the finite difference [22,24] and FEM [25,26] are well suited.

We introduce the program package SAP (Smart Analysis Programs) that is intended for highly accurate simulation of the most critical interconnect problems. The simulation tools of SAP support modes for

- resistance extraction;
- capacitance extraction;
- coupled electrical and thermal simulation (steady state and transient); and
- quasi-electrostatic simulation (for calculation of cross-talk and delay times).

For the numerical solution of the involved partial differential equations we use the FEM. The main advantages of the FEM over competitive methods like boundary integral techniques are its numerical robustness, the high accuracy obtained, the ability to solve nonlinear systems, and the general applicability to all of the above mentioned problem types.

Besides the finite element solvers, we have also developed tools for geometry preprocessing, solid modeling, automatic grid generation, and visualization. Fig. 1 gives an overview on the "Smart Analysis Programs".

2. Geometric modeling

A precise geometric representation of the "real" structure is essential for accurate simulation results. SAP supports for this reason a flexible geometry description language, which allows an easy layer-by-layer construction of the simulation structure. Additionally, with the tools presented in Refs. [27,28], it is possible to import layout files in CIF or GDSII format, or create them interactively with a graphical layout editor which is also used to select an "area of interest" or define cuts for 2D simulations. The geometric structure can then be either generated directly from the layout assuming constant layer thicknesses or by rigorous lithography [29], and topography simulation [30].

2.1. Input preprocessing

The two preprocessors CUTGRID (2D) and LAYGRID (3D) are used for specification of the simulation geometry and contacts (both electrical and thermal). In 2D the structure is constructed in terms of primitives (rectangles, circles, or general polygons) made of a specific material. The polygons may overlap, in this case, the area covered by other polygons is removed by a solid modeler.

3D structures are built with planar or non-planar layers. Each 2D layer is defined with the procedure described above. All geometric dimensions may be entered either as a constant value or as a variable expression, which is evaluated by the preprocessor previous to the solid modeling step. This allows us to parameterize certain features of the layout, which can be well utilized in automatic optimization environments [31].

2.2. Grid generation

The preprocessors are also responsible for the generation of the simulation grid. In two dimensions the mesher called Triangle [32] is used. For the 3D case the user can choose

between two different gridding methods. The first one is a layer-based method that works closely together with the 3D solid modeler. Basically, this method starts with a 2D grid which is generated by triangulating a merged structure (2D projection onto the *x*,*y*-plane) of all layers. The triangles are "extruded" into the *z*-direction and for each layer a prism is generated. Finally, each prism is split into three tetrahedrons.

The second implemented grid generator is the fully 3D unstructured Delaunay triangulator DELINK [33], that uses an advancing-front algorithm to "fill" solids (represented by their boundaries) with tetrahedrons.

3. Finite element simulation

Our simulator supports triangular (three- and six-node) and tetrahedral (four- and ten-node) grid elements, used for 2D and 3D simulations. The finite element discretization can be performed with linear and quadratic shape functions. For efficient utilization of computer memory, the sparsely occupied stiffness matrix is stored in a compressed format (MCSR). A preconditioned conjugate gradient solver (ICCG) that has been optimized specifically for the discretized Laplace operator is used to solve the large linear systems [34]. For highly accurate results a global grid refinement algorithm is implemented.

3.1. Capacitance extraction

A structure with n conductors has $n(n-1)/2$ (partial) capacitances across. For the capacitance extraction we calculate the electric potential φ inside the insulator domain by solving the Euler equation

$$\mathrm{div}(\bar{\varepsilon}(x, y, z)\mathrm{grad}\varphi) = 0, \tag{1}$$

where $\bar{\varepsilon}$ denotes the permittivity tensor.

For the finite element discretization of Eq. (1), we use the Ritz–Rayleigh method based on the formulation as a variational problem [35]. Conductor surfaces are represented by Dirichlet boundary conditions, the outer boundary of the simulation domain implicitly has a homogeneous Neumann boundary condition. Therefore, the simulation domain has to be chosen sufficiently large in a manner that the electric field is not distorted by the outer boundary. However, this effect can be exploited to reduce the computational effort for geometric structures with symmetries.

$n-1$ simulation runs are performed with different conductor potentials applied, and the electrostatic field energy is calculated. From the energy values the partial capacitance matrix is extracted.

The main advantage of our implementation over other simulation tools based on the boundary element method, geometric or stochastic methods is that it is not limited to stratified structures and can deal with anisotropic dielectrics. The cost is a higher memory consumption, which makes full-chip calculations impracticable. However, the method is well suited for highly accurate simulations of smaller parts of the chip.

3.2. Resistance extraction

The calculation of resistances is performed in a similar manner by solving

$$\mathrm{div}(\gamma(x, y, z)\mathrm{grad}\varphi) = 0 \tag{2}$$

in the domains of conducting material, where γ is the conductivity. At the ends of the wires Dirichlet boundary conditions are applied. Each conductor (net) is calculated in a separate run.

3.3. Quasi-electrostatic simulation

Usually delay times or crosstalk on interconnect lines are calculated analytically based on extracted resistances and capacitances using lumped or distributed (transmission line) models. This approach is only valid for configurations where the electrical field is perpendicular to the direction of signal propagation. For general structures more accurate results can be achieved by solving the potential distribution function in an electro quasi-static regime

$$\mathrm{div}(\gamma\mathrm{grad}\varphi + \bar{\varepsilon}\mathrm{grad}(\partial\varphi/\partial t)) = 0 \tag{3}$$

again using the FEM. For the time discretization, we use the Backward-Euler and the Crank–Nicholson methods.

3.4. Coupled electro-thermal simulation

For the numerical calculation of Joule self-heating effects, two partial differential equations have to be solved. The first one describes the electric sub-problem,

$$\mathrm{div}(\gamma_{\mathrm{E}}\mathrm{grad}\varphi) = 0. \tag{4}$$

The electric potential φ needs to be solved only inside domains composed of electrically conducting material (γ_{E} represents the electrical conductivity). On the surface of the conductors three types of boundary conditions are allowed:

- Dirichlet — a constant potential is specified;
- Neumann — a constant current density is specified; and
- floating potential — the total current is specified and the potential is forced to be the same all over the boundary area.

The next step is to calculate the power loss density p,

$$p = \gamma_{\mathrm{E}}(\mathrm{grad}\varphi)^2. \tag{5}$$

Then, the heat conduction equation has to be solved to obtain the distribution of the temperature T,

$$\mathrm{div}(\gamma_{\mathrm{T}}\mathrm{grad}\, T) = p - c_{\mathrm{p}}\rho_{\mathrm{m}}(\partial T/\partial t) \tag{6}$$

γ_{T} represents the thermal conductivity, c_{p} the specific heat and ρ_{m} the mass density.

Heat sinks are modeled by Dirichlet boundary conditions (constant temperature). To simulate additional heat emitting

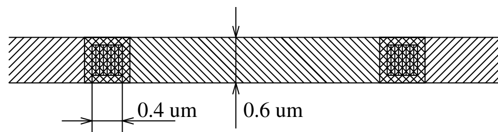

Fig. 2. Layout of the Cu via.

devices, the user can arrange flat or voluminous heat sources with a constant power dissipation rate.

Both, the electrical and thermal conductivities of certain materials depend on temperature. Therefore, we use a second-order approximation:

$$\gamma(T) = \gamma_0 \frac{1}{1 + \alpha(T - T_0) + \beta(T - T_0)^2}. \tag{7}$$

γ_0 is the (electrical or thermal) conductivity at the temperature T_0 of 300 K, α and β are constant (linear and quadratic) temperature coefficients.

This makes the problem nonlinear. Since this nonlinearity is relatively weak, a simple iterative relaxation method is used which quickly converges upon the solution, usually after 3–6 iterations.

For accurate simulation results it is important to specify a sufficiently large simulation domain. We found that the lateral width of the simulation area should be chosen at least 1.2–1.5 times the thickness of the thickest layer (usually the silicon substrate). It is possible to omit small geometric features in areas where accuracy is not critical. A reduction of the simulation domain causes predominantly an error in the calculated temperature whereas current densities and temperature gradients are less affected.

Areas of the chip surface exposed to air are difficult to model with the heat flow equation since the heat transport mechanism in gases is dominated by convection, not conduction. The total thermal resistance for the boundary to air is nonlinear and depends on some poorly known factors (e.g. airspeed). Fortunately, the thermal conductivity of air is very low compared to other materials. However, in most cases the air-boundary cannot be totally neglected because it covers a major part of the chip and a considerable amount of the generated heat is dissipated thereby. We tackle this problem with a very simple model, namely a 1 μm thick layer of "air" with a thermal conductivity of 0.015–0.03 W/mK and constant temperature (ambient temperature) on the top. This model has been found to be sufficient for most applications since the obtained results compare well to measurements [36].

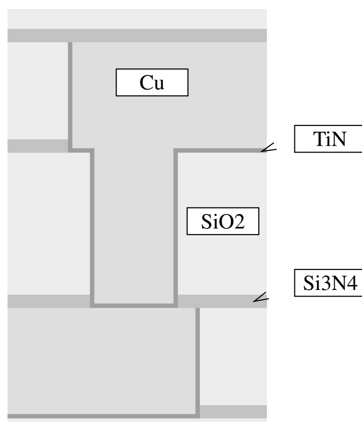

Fig. 3. Cross-sectional view of the via structure in a dual-damascene process.

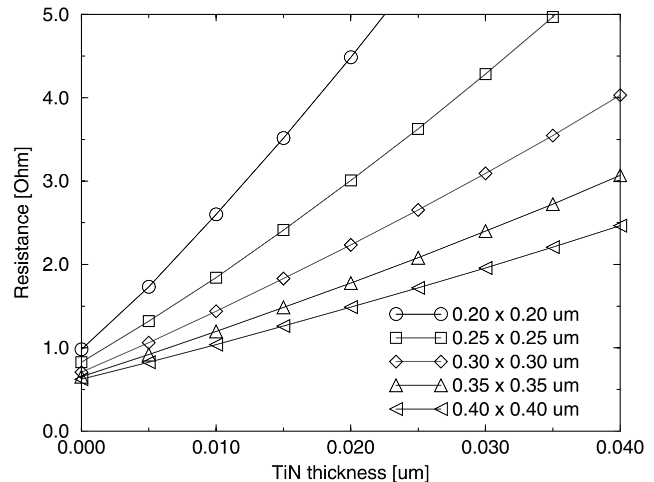

Fig. 4. Via resistance of various sized Cu vias at room temperature. For small thicknesses of the TiN barrier layer the dependence is almost linear.

4. Visualization

The package SAP contains a visualization program that can be used to display the distributions of the calculated attributes like potential, current density, power loss density, field strength, electric displacement, temperature, and heat flow. The program is based on VTK [37], a flexible and powerful visualization library. Scalar attributes can be visualized as surface color or by displaying iso-lines or iso-surfaces. For vector attributes cones pointing in the direction of the field are displayed in every point of the grid.

A special mode exists for locating quickly hot spots and areas with high current densities, where an iso-surface at a value of 90% of the maximum temperature or current density is displayed.

The visualization program can be operated interactively with a menu driven graphical user interface as well as in batch mode without user interaction.

5. Application examples

5.1. Via-chain structure

The resistance of an interconnection path not only depend on the line width and length but also contacts and vias contribute a significant amount to the total resistance. In

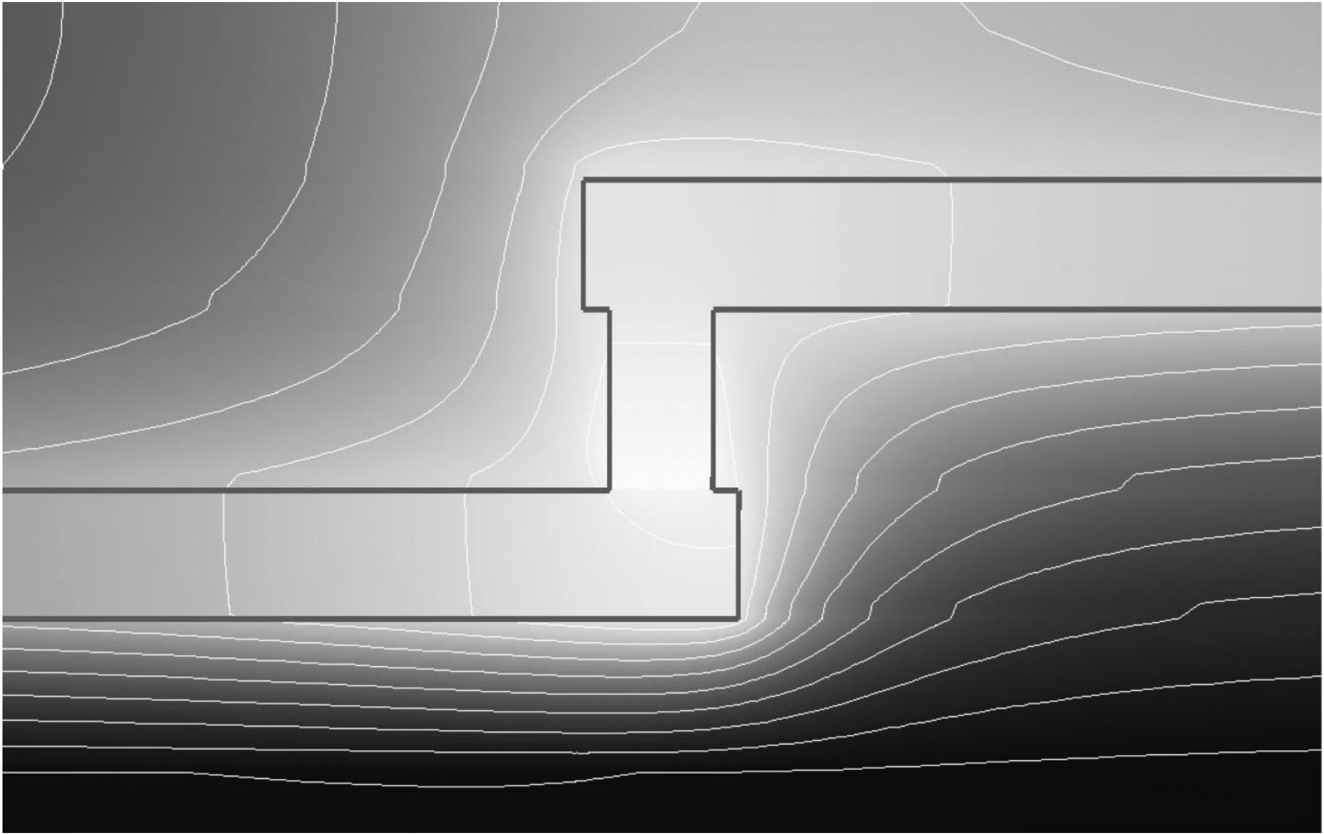

Fig. 5. Temperature profile on the cross-sectional view of the test structure. The maximum temperature of 91°C is reached at the bottom of the via. The substrate surface under the via has a temperature of 47°C. The isothermal lines are 4.4°C apart.

this example, we simulate a chain of vias in a copper dual-damascene process architecture [38].

Fig. 2 shows a part of the layout of a chain of $0.4 \times 0.4\ \mu m^2$ vias, in Fig. 3 the cross-section of a single via is displayed. Since the structure repeats periodically only a single via needs to be simulated and the simulation area is bounded by symmetry planes. The via resistance strongly depends on the thickness of the TiN barrier layer due to its low conductivity. Fig. 4 shows the results of the resistance calculations as a function of the TiN thickness for via sizes from $0.2 \times 0.2\ \mu m^2$ to $0.4 \times 0.4\ \mu m^2$.

A comparison with measured data [38] shows a resistance of about 30% higher than the calculated value for the case with 20 nm TiN barrier, which can be explained by a contact resistance of TiN/Cu transitions. For zero barrier thickness, the simulated and measured data perfectly match.

We simulated also the thermal behavior of the $0.4 \times 0.4\ \mu m^2$ via chain structure with 20 nm TiN (as displayed in Fig. 3). For that application a high current (13.4 mA) was applied to the ends of the via chain structure, which is equivalent to a current density of approximately 8.5 MA/cm^2 in the center of the via. The bottom of the Si-substrate is kept at constant temperature of 24°C.

Fig. 5 shows the temperature profile cross-section. The maximum temperature of 91°C is reached at the bottom of the via and coincides well with the maximum in the heat generation rate. Fig. 6 shows the current density on the half via structure. The high resistance of the TiN barrier causes an almost equal distribution of the current at the bottom of the via. The highest current density is observed at the top of the via in the corner on the right-hand side. Since this spot also has an increased temperature it will be most vulnerable to electromigration.

5.2. Polysilicon resistor

In this example we analyze a matched polysilicon resistor pair. Both lines are 1 μm wide, and have a total length of 171 μm. The polysilicon layer is 0.5 μm thick and has a resistance of 2000 Ω/□. The structure was converted from a layout file (see Fig. 7) to the SAP data representation.

In the first step we extracted the resistances and capacitances ($R_1 = R_2 = 3.34\ k\Omega$, $C_{1,gnd} = 19.0\ fF$, $C_{2,gnd} = 19.4\ fF$, $C_{1,2} = 5.0\ fF$). Transient electric simulation is applied to calculate delay times and crosstalk between the resistors. Therefore, a voltage step of 1 V is applied on the left terminal of the first resistor, the second resistor is connected to ground and the Si-substrate has been assumed as an ideal conductor connected to ground. A delay time of 106 ps is observed until the output voltage of the first resistor reaches 90% of the input. Crosstalk occurs on the output

Fig. 6. Distribution of the current density in a (half) via in A/m^2.

of the second resistor, its maximum of 0.1 V is reached after 40 ps (see Fig. 8).

The computed output voltages are in very good accordance with the results obtained from a calculation of a 5-stage lumped model based on the extracted R and C values.

In the second transient simulation we assumed a substrate with a lightly doped EPI layer with a resistivity of 10 Ωcm. The output voltages of the active and the grounded line (with respect to the potential of the substrate surface on the right side below the contacts) are shown in Fig. 9 (solid lines). Note, that these results differ significantly from the previous simulation. Now the delay time on the active line is much longer (600 ps) and the crosstalk is negative (maximum −0.31 V after 133 ps). For the comparison of the simulation results with a lumped model, we extracted the resistance of the substrate between the contacts below the left and right ends of the lines (14.9 kΩ). The results of the extended five stage lumped model (dashed lines in Fig. 9) are not as accurate as in the previous simulation for the first 300 ps, but after this period the error vanishes.

Thermally induced mismatch in the resistances is calculated in a coupled electro-thermal simulation run. Here, one line is loaded with a current of 3 mA, and the bottom of the Si-substrate is kept constantly at 300 K. This causes a difference of 2% in the resistances due to joule self-heating.

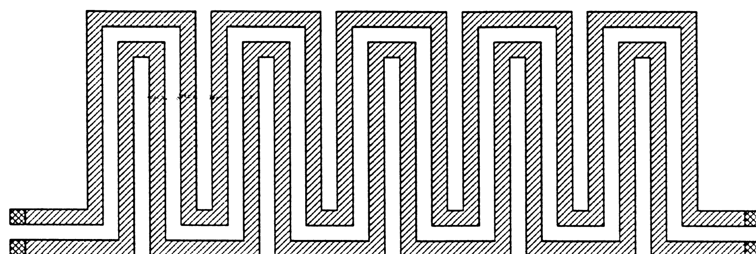

Fig. 7. Polyresistor layout.

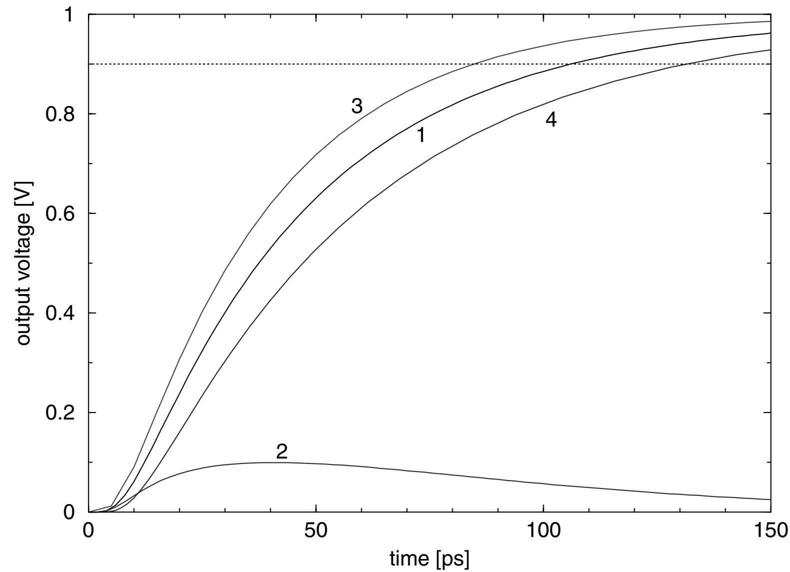

Fig. 8. Output voltages of the polysilicon resistor pair: 1 and 2: one resistor gets a voltage step of 1 V, the other is connected to 0 V; curve 1 shows the output voltage on the active line, the delay is 106 ps; 2: crosstalk on the second line, maximum 0.1 V; 3: voltage step is applied to both resistors: delay 84 ps; 4: output for a straight polysilicon line with the same length, delay 132 ps.

6. Memory and CPU time consumption

The dynamically allocated memory and CPU time consumption of the SAP simulators has been measured by simulating about 30 different two-contact capacitance and resistance extraction problems in two and three dimensions. The simulations have been carried out on a DEC AlphaStation 600 with 512 MByte main memory and a 21164 CPU at 333 MHz running Digital Unix 4.0. Fig. 10 shows the dependence on the total number of grid nodes.

7. Conclusion

We introduced the interconnect analysis program package SAP and demonstrated its usefulness for highly accurate interconnect simulation by a polysilicon resistor and a Cu via example. The obtained results agree well with measurements and are more accurate than simple geometrical models. Another advantage of our method is that the calculated properties are known at every point of the simulation domain, not only at the contacts, but it requires more memory and CPU time. The program is freely

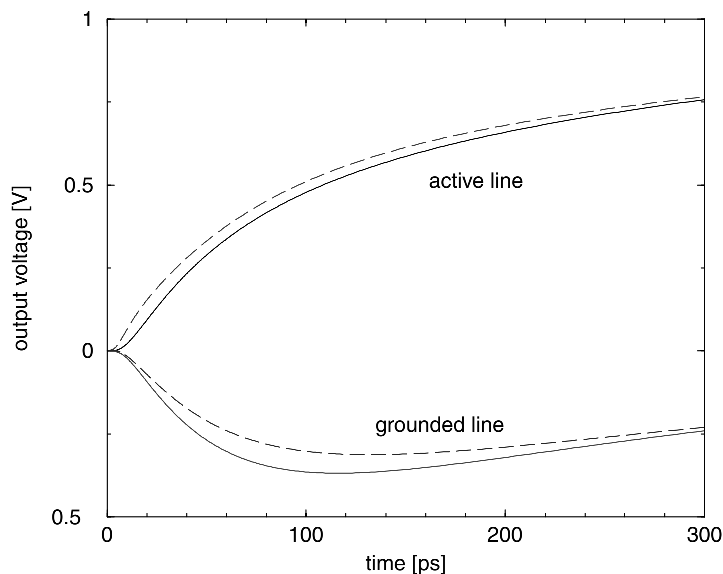

Fig. 9. Simulated output voltages of the polysilicon resistor over lossy substrate.

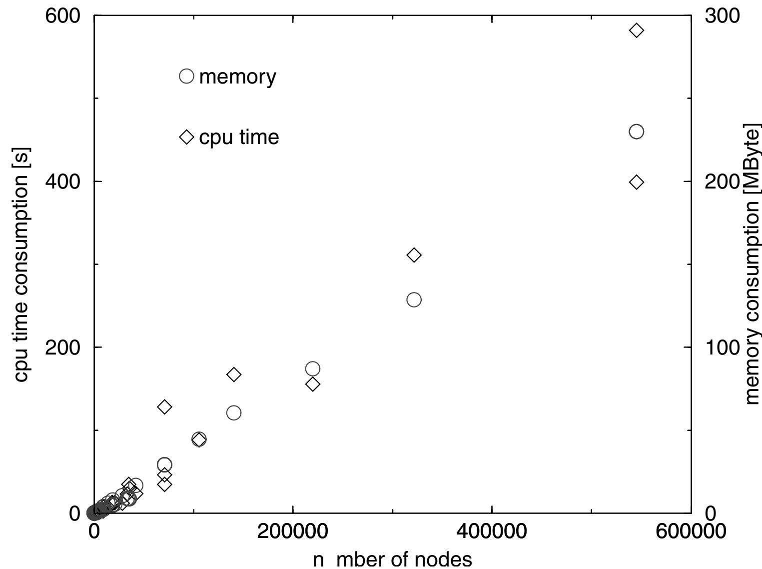

Fig. 10. Memory and CPU time consumption measured on an AlphaStation 600.

available, for information on obtaining SAP see http://www.iue.tuwien.ac.at/software/software.html.

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