MACRO-MODELING FOR MOS DEVICE SIMULATION

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Abstract - By making use of the MOS diode theory, the carrier, and current distribution, as well as the mobility in a MOS device is evaluated. Simple analytical expressions are used for parameters like mobility, carrier concentration, and transversal electric field. Agreement between experimental and simulated results from an LDD MOSFET and an n-well resistance is in agreement, probing this approach is suitable as a plug-in model tester for quick model evaluation.

I INTRODUCTION

Nano-meter devices are key devices for designing high-performance low-power systems. Whereas device simulators are focused on device optimization referred to the technology parameters of a given fabrication process, electric simulators make use of the device electric properties to build up an electronic system. However, the physics-based device model is not well suited for such a task due to its mathematical complexity. Novel and miniaturized devices make the conventional formulations inadequate, because the new physical effects are not incorporated.

The development of mathematical models that predict the electric behavior of nano-devices is a cumbersome task. Either complex expressions are generated, or some physical aspects are neglected in the general formulation. Device simulators are programmed in such a way that the device designer gets a better match between experiments and theory. Unfortunately, devices simulators are no the right choice for circuit designers, where simple analytical expressions are needed to rapidly evaluate circuits with thousands or millions of transistors.

This paper gives a new general strategy for simulating the electric behavior of MOS devices. Although it has been developed for unipolar devices, it can be extended to bipolar devices. Simple mathematical expressions were used, minimizing the number of fitting parameters, and by taking into account the technology-dependence of the most representative electric parameters, such as; threshold voltage, carrier mobility, etc.

II GENERAL ANALYSIS

Figure 1 shows a metal-oxide-semiconductor device. It is a conventional MOS structure, where the carrier conduction takes place in the n-well.

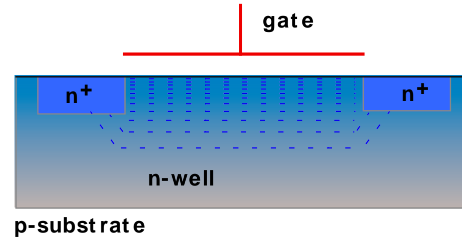

Figure 1: MOS device structure

There are two (n^+) contacts at the edges, where the resistor current is injected and collected. The resistance of the structure is controlled by the gate. For positive gate voltages electrons accumulate at the surface reducing the resistance, while at negative voltages the surface gets inverted increasing the resistance. The structure becomes a pMOS transistor when the n^+ diffusion is replaced by p^+ diffusions.

The conductivity of the region under the gate terminal is computed according to Ohm's law.

$$\sigma = \left(q \cdot n \cdot \mu\right) \tag{1}$$

where q is the magnitude of the electronic charge, n the carrier concentration, and μ the carrier mobility.

The conductivity σ is gate voltage dependent through n and μ that are modulated by the gate. From the MOS diode theory [1] the electron concentration n is computed as follows

$$n(y) = n_o e^{-\psi(y)/\phi_t} \tag{2}$$

where y is the coordinate towards the substrate direction, n_o the thermal equilibrium electron concentration, $\psi(y)$ the surface potential, and ϕ_t is the thermal voltage. The hole concentration reads

$$p(y) = p_o e^{\psi(y)/\phi_t} \tag{3}$$

The surface potential is computed according to the following formulation

$$\psi(y) = \psi\left(1 - y/W\right)^2 \tag{4}$$

where W is the maximum width of the depletion layer under the gate, which is computed as follows

$$W = \sqrt{\frac{2\varepsilon_{Si}\phi_F}{qN}} \tag{5}$$

ϕ_F is the Fermi potential and N is the doping concentration.
In general the current driven by the device can be calculated with the following formulation

$$I = \sigma \frac{W}{L} t_S V \tag{6}$$

where W, L, and t_S are the width, length, and thickness of the sample respectively. V is the potential between the electrodes.
The influence of the gate voltage on the carrier concentration takes place in a very narrow film under the gate, therefore the semiconductor under the gate oxide is split up into different layers, with the current being calculated for each of these layers. The total current is computed as the addition of all these layer contributions (see Fig. 1). The total current, in a gate-controlled resistor, is then calculated as the current flowing through the portion of the semiconductor controlled by the gate, plus the current flowing through the neutral region, where the gate voltage does not exert any influence.
The mobility parameter is crucial in computing appropriate values for the current. In inversion layers the carrier mobility is computed as follows

$$\mu_{n,p}^{LIC} = \mu_{n,p}^{\min} + \frac{\mu_{n,p}^{0}\left(\frac{T}{300\,K}\right)^{-\gamma_{n,p}} - \mu_{n,p}^{\min}}{1 + \left(\frac{CI}{C_{n,p}^{ref}}\right)^{\alpha_{n,p}} + \left(\frac{\sqrt{n \cdot p}}{k_{n,p} \cdot C_{n,p}^{ref}}\right)^{\alpha_{n,p}}} \tag{7}$$

Equation (7) computes the mobility due to lattice (L), incomplete ionization (I), and carrier to carrier scattering (C). It combines the formulations of Arora [3], Caughey and Thomas [4], and Adler [5]. The constants used in the model are defined as follows

$$\mu_{n,p}^{\min} = \begin{cases} \alpha_{n,p}\left(\frac{T}{300\,K}\right)^{b_{n,p}} & T \geq T_{crit} \\ \alpha_{n,p}\left(C_{n,p}\right)^{b_{n,p}} \bullet \left(\frac{T}{200\,K}\right)^{d_{n,p}} & T \geq T_{crit} \end{cases} \tag{8a}$$

$$C_{n,p}^{ref} = f_{n,p}\left(\frac{T}{300\,K}\right)^{g_{n,p}}$$

$$\alpha_{n,p}^{ref} = h_{n,p}\left(\frac{T}{300\,K}\right)^{j_{n,p}} \tag{8b}$$

The surface scattering mobility is computed with the expression found in [6]

$$\mu_{n,p}^{LICS} = \frac{\mu_{n,p}^{ref} + \left(\mu_{n,p}^{LICNE} - \mu_{n,p}^{ref}\right)\left(1 - F(y)\right)}{1 + F(y)\left(\frac{E_{n,p}^{\perp}}{\alpha_{n,p}}\right)^{b_{n,p}}} \tag{9}$$

where the reference mobility is a temperature dependent coefficient.

$$\mu_{n,p}^{ref} = c_{n,p} \left(\frac{T}{300\,K} \right)^{-d_{n,p}} \tag{10}$$

and the *F(y)* function reads as

$$F(y) = \frac{2\,e^{-\left(\frac{y}{e_{n,p}}\right)^2}}{1 + e^{-\left(\frac{y}{e_{n,p}}\right)^2}} \tag{11}$$

Finally, a saturation velocity reduction is computed with the conventional formulation [7].

$$\mu_{n,p}^{LICSE} = \frac{\mu_{n,p}^{LICS}}{\left(1 + \left(\frac{E_{n,p}}{E_{n,p}^{crit}}\right)^{\beta_{n,p}}\right)^{1/\beta_{n,p}}} \tag{12}$$

These models were implemented into the Matlab and Maple [8] code together with the layer-split algorithm. Taking advantage of the Maple symbolic capability, one saves hundreds of code lines to implement the MOSFET and gate-controlled resistor simulator. The values for the different constants used here, and the various physical factors were taken from literature [1, 2, 9]. As a result, the number of parameters is drastically reduced making this a friendly approach to investigate the impact of technology parameters on the electric behavior of MOS devices.

III RESULTS

Figure 2 shows the Ids-Vds experimental and simulated characteristics of a (W/L)=(20/0.5) LDD nMOSFET with a gate oxide thickness of 10 nm and a bulk substrate doping concentration of 10^{17} cm^{-3}. The match between experimental and simulated results is quite good. The distribution current for different gate voltages (Vds=3.4 V) is shown in Figure 3. The variation of the electron concentration towards the substrate is shown in Figure 4 for different values of the gate voltage.
The computed mobility is shown in Figure 5. From these two previous figures one can see the carrier concentration decreases towards the substrate direction and the carrier mobility increases due to the reduction of the lattice scattering mechanism.

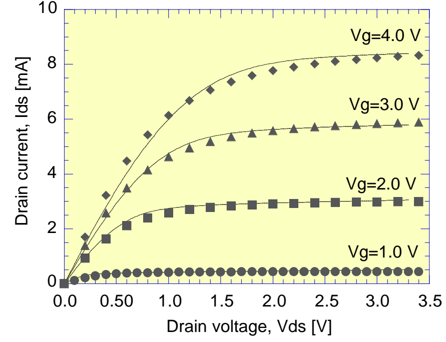

Figure 2: Experimental and simulated (symbols) Ids-Vds characteristics.

We emphasize that this match was obtained only by adjusting the carrier mobility parameters, which on its turns, depend on technology parameters.

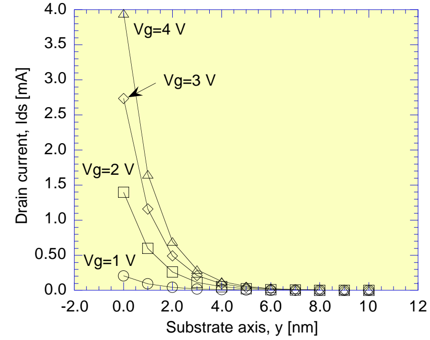

Figure 3: Simulated results for Ids as a function of y, with Vg as a parameter.

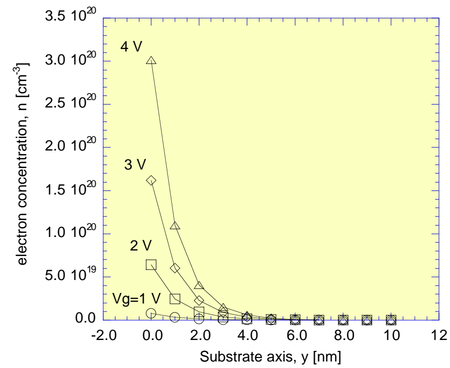

Figure 4: Simulated results for the electron concentration as a function of y.

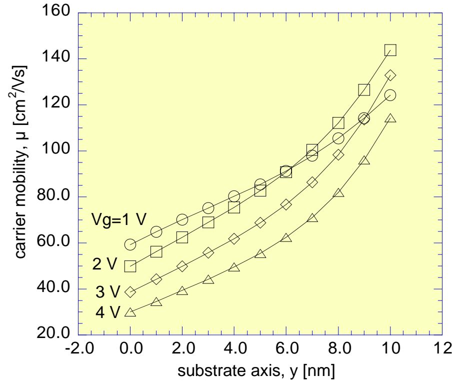

Figure 5: Simulated results for the carrier mobility using ten layers.

To be sure that this approach has a wide validity, the n-well gated-resistor, where carrier conduction takes place through an accumulation layer, was also simulated. In this case the sample device has an n-well concentration of 10^{17} cm^{-3}, with a (W/L) relation of (2/200), and an n-well junction depth of 1.8 μm.

Whereas in the case of inversion layers (MOSFET) the device was split up into ten layers, the gated resistor requires a different layer-split approach. The current is not only computed in the accumulation region, but also in the neutral region under the accumulation layer. When the gated-resistor is operated in inversion, the electrons do not flow near the surface, where the inversion layer forms, but under it, where the n-well is neutral.

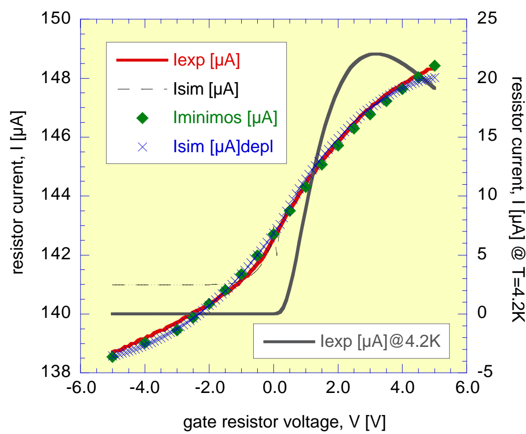

Figure 6: Experimental and simulation results for the gated current.

In the gate-voltage sensitive region the device was split into 30 layers, while a split into 10 layers was used for the neutral region. The results are shown in Figure 6.

IV DISCUSSION

The simulation results of the gated resistor show that for positive gate voltages, the current increases due to the accumulation electrons near the surface. For negative values of the gate voltage, the surface gets depleted of electrons, forcing the current to flow under the surface, where the n-well is neutral. This effect causes the reduction of the current.

A Minimos-NT simulation is included in the results shown in Figure 6. An optional simulation without considering the depletion region is also shown in this figure, which shows that charge current can get blocked if there were no option to flow below the depletion region. This is confirmed by the experimental curve measured at the liquid-helium temperature (T=4.2 K), where the freeze-out effect blocks any chances for the current to flow through the neutral n-well portion [10].

The current distribution and carrier concentration as a function of the substrate axis, for different values of the gate voltage is shown in Figure 7 and Figure 8.

The current in the body of the gated resistor is uniformly distributed in comparison to a MOSFET where most of the current flows in a very narrow surface sheet.

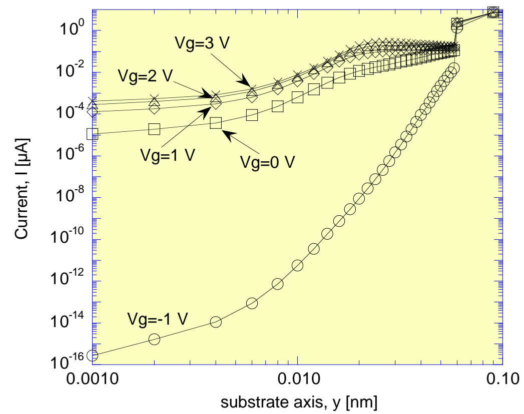

Figure 7: Simulated current distribution under the gate region.

V CONCLUSIONS

A different approach for computing the electric response of MOS devices, as well as some of their physical parameters, like carrier mobility, carrier concentration, etc., has been

presented. By splitting the device into different layers, local effects can be studied, and the contribution to the whole current can be examined. This approach reduces to the minimum possible use of fitting parameters and complex formulations. The physical parameters are exclusively computed based on values for the technology parameters. The tool has been validated by comparing its results with experiments, and by making reference to a rigorous two-dimensional device simulator. Besides, this tool has the ability to reduce the CPU time by 50 percent compared to Minimos-NT. This tool is available in the Maple and Matlab source code, which gives it a multi-platform portable capability.

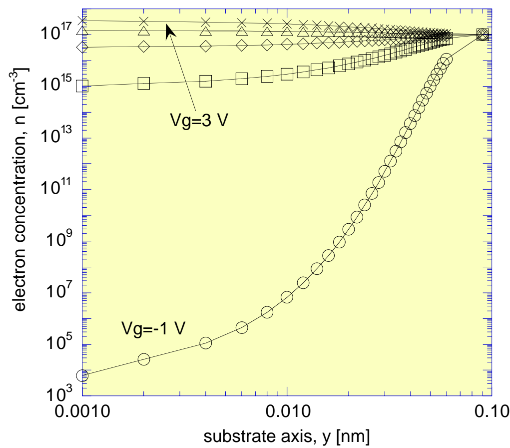

Figure 8: Simulated electron concentration for the gated resistor for differente gate voltages.

VI ACKNOWLEDGMENTS

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